PAPER Special Section on Analog Circuit and Device Technologies

Ultralow-Power Current Reference Circuit with Low Temperature Dependence

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SUMMARY An ultralow power constant reference current circuit with low temperature dependence for micropower electronic applications is proposed in this paper. This circuit consists of a constant-current subcircuit and a bias-voltage subcircuits, and it compensates for the temperature characteristics of mobility μ, thermal voltage V_T, and threshold voltage V_{TH} in such a way that the reference current has small temperature dependence. A SPICE simulation demonstrated that reference current and total power dissipation is 97.7 nA, 1.1 μW, respectively, and the variation in the reference current can be kept very small within ±4% in a temperature range from −20 to 100°C.

key words: *CMOS, reference, subthreshold, weak inversion, low power, temperature dependence*

1. Introduction

One of the promising areas of research in microelectronics is the development of ultralow power analog LSIs that consist of subthreshold MOSFETs, or MOSFETs that are operated in the region of weak inversion. To construct such LSIs, we must first develop voltage and current references that can operate with low-power dissipation of a few micro watts or less. We herein describe one such low power reference, a current reference that uses a subthreshold MOSFET circuit and that generates a constant current independent of temperature and supply voltage.

In the near future, "ubiquitous" network systems will be created. Such systems require many sensing LSIs, or smart sensors, that measure various physical data in surroundings, that store the measured data, and that output the data on demand. These sensing LSIs must operate with a low-power supply because they will probably be placed under conditions where they have to get the necessary energy from microbatteries or from less-than-ideal surroundings such as ones with poor sunshine, weak electric waves, and slight differences in temperature between day and night. To create an ultralow power LSIs, we designed a circuit in the subthreshold region. In such an LSI operated in the subthreshold region, we need to develop a constant voltage supply circuit and a constant current reference circuit that has ultralow power dissipation for these LSIs.

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Many current reference circuits operating with strong inversion has been reported [1]. A Beta Multiplier Self Biasing circuit is widely used as a current reference circuit using MOSFET. However, this circuit requires a very large value of the resistor to generate a small output current, and moreover, has a problem in which the output current increases linearly as the temperature increases. A current reference circuit reported by Oguey and Aebischer [2] generates a small output current using strong inversion transistors that operate in the linear and saturation regions. Resistors are not used. However, the circuit is not enough for the discussion on the temperature dependence on its output reference current. The circuit is not enough to use as a reference current under an environment where the temperature changes because the output current that they proposed increases proportionally as the temperature increases (see Appendix).

There are few reports on the premise of operating in the subthreshold region. The purpose of this work is to offer a design method for a constant current reference circuit that works at the subthreshold region over a large temperature range. This paper is organized as follows: circuit configurations and operation principles are described in Sect. 2, simulation results are presented in Sect. 3, and we conclude the paper in Sect. 4. Note that all the simulations were performed using SPICE BSIM3 level 49 model and 0.25 μm TSMC-CMOS parameters.

2. Circuit Configuration

The current reference circuit we describe consists of a constant-current subcircuit and a bias-voltage subcircuit. The latter supplies a bias voltage to the former.

2.1 Constant-Current Subcircuit

Figure 1(a) shows the constant current subcircuit. It is based on the β-multiplier self biasing circuit (Fig. 1(b)) and uses a MOS resistor M_R instead of an ordinary resistor R. We operate all MOSFETs in this circuit in the weak-inversion region except for the MOS resistor in the strong-inversion and triode region. This circuit has two advantages compared with the basic β multiplier: the first is that it needs no resistor of high resistance that occupies a large area on an LSI chip, and the second is that it can achieve a zero temperature coefficient of current for an appropriate bias voltage V_{BIAS} for the MOS resistor. This circuit works as follows.

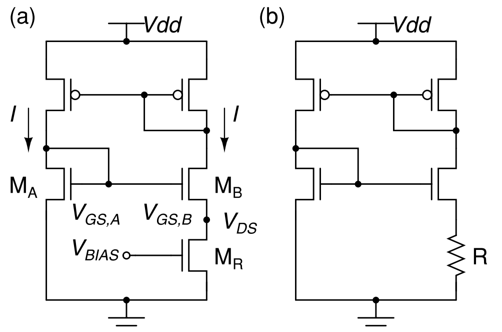

Fig. 1 Constant-current subcircuit (a) configuration of the circuit we use, and (b) basic β-multiplier self biasing circuit.

The subthreshold MOS current [3], [4] for a drain-source voltage V_{DS} higher than 0.1 V is given by

$$I = KI_0 \exp\left(\frac{V_{GS} - V_{TH} - V_{OFF}}{\eta V_T}\right) \tag{1}$$
$$I_0 = \mu C_{OX} V_T^2 (\eta - 1),$$

where K is the aspect ratio (=channel width/channel length), μ is the mobility, C_{OX} is the gate-oxide capacitance, V_T is the thermal voltage ($V_T = k_B T/q$), η is the subthreshold swing parameter, V_{TH} is the threshold voltage, V_{OFF} is the offset voltage difference between the threshold voltage in the strong inversion and that in the subthreshold region, and I_0 is called the pre-exponential factor. Voltage V_{OFF} depends on the channel width and can be given by

$$V_{OFF} = V_{OFF,0} + \frac{V_{OFF,W}}{W}, \tag{2}$$

where $V_{OFF,0}$ is the large-channel-width offset voltage, $V_{OFF,W}$ is a positive coefficient, and W is the channel width.

In the circuit in Fig. 1(a), the gate-source voltage $V_{GS,A}$ in transistor M_A must be equal to the sum of the gate-source voltage $V_{GS,B}$ in M_B and the drain-source voltage V_{DS} in M_R, or

$$V_{GS,A} = V_{GS,B} + V_{DS}. \tag{3}$$

Because the currents I through the transistors M_A and M_B are the same, Eq. (3) can be rewritten as

$$V_{DS} = \alpha_{A,B} + \eta V_T \ln\left(\frac{K_B}{K_A}\right), \tag{4}$$

where $\alpha_{A,B}(= V_{OFF,A} - V_{OFF,B})$ is the difference in the offset voltages, and K_A and K_B are the aspect ratios of transistors M_A and M_B. The resistance R_{M_R} of MOSFET M_R operated in the triode region is given by

$$R_{M_R} = \frac{1}{\mu C_{OX}\left(\frac{W}{L}\right)(V_{BIAS} - V_{TH})}. \tag{5}$$

We find from Eqs. (1),(2),(4), and (5) that the current I through M_A and M_B is given by

$$I = \frac{V_{DS}}{R_{M_R}} = \left(\alpha_{A,B} + \eta V_T \ln\left(\frac{K_B}{K_A}\right)\right) \times \mu C_{OX}\left(\frac{W}{L}\right)(V_{BIAS} - V_{TH}). \tag{6}$$

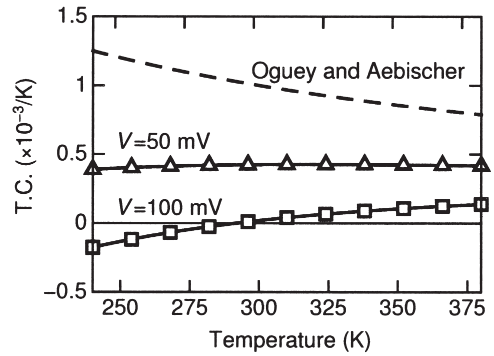

Fig. 2 Value of TC as a function of temperature, calculated from Eq. (10), with the overdriving voltage V as a parameter. The dashed curve shows the TC of Oguey and Aebischer's circuit.

2.2 Temperature Dependence of the Circuit Current

Equation (6) shows that the temperature coefficient (TC) of current I is

$$TC_I = \frac{1}{I}\frac{\partial I}{\partial T} = \frac{1}{\alpha_{A,B} + \eta V_T \ln\left(\frac{K_B}{K_A}\right)} \frac{\partial\left(\alpha_{A,B} + \eta V_T \ln\left(\frac{K_B}{K_A}\right)\right)}{\partial T} + \frac{1}{\mu}\frac{\partial \mu}{\partial T} + \frac{1}{V_{BIAS} - V_{TH}} \frac{\partial (V_{BIAS} - V_{TH})}{\partial T}. \tag{7}$$

The temperature dependence on the mobility and threshold voltage are

$$\mu = \mu(T_0)\left(\frac{T}{T_0}\right)^{-m}, \tag{8}$$
$$V_{TH} = V_{TH0} - \kappa T, \tag{9}$$

where $\mu(T_0)$ is the mobility at room temperature (T_0), V_{TH0} is the threshold voltage at absolute zero, and κ is the temperature dependence parameter. For a fixed reference voltage V_{BIAS}, TC can be expressed by equation

$$TC_I = \frac{\eta V_T \ln\left(\frac{K_B}{K_A}\right)}{T\left(\alpha_{A,B} + \eta V_T \ln\left(\frac{K_B}{K_A}\right)\right)} - \frac{m}{T} + \frac{\kappa}{V + \kappa T}, \tag{10}$$

where $V(= V_{BIAS} - V_{TH0})$ is the overdriving voltage. The first term on the right is almost equal to $1/T$ for small $\alpha_{A,B}$ values, the second term is about $-1.5/T$ for ordinary MOSFETs, and the third term changes from $1/T$ to 0 as a function of V. Therefore, TC can be set to 0 at room temperature by adjusting V to an appropriate value. Figure 2 shows the calculated value of TC as a function of temperature. In this example, a zero TC can be obtained at $V = 100$ mV at room temperature. The value of TC for Oguey and Aebischer's circuit, calculated from Eq. (A·3), is also depicted for comparison.

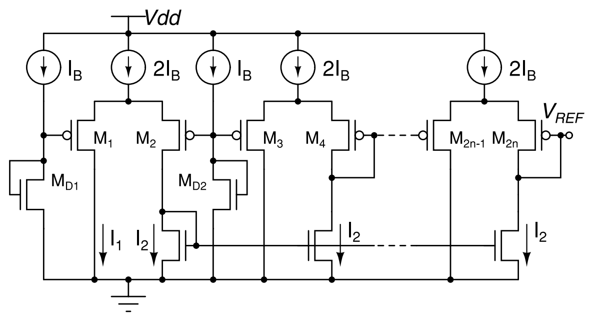

Fig. 3 Bias voltage circuit. It consists of two diode-connected transistors and n differential pairs.

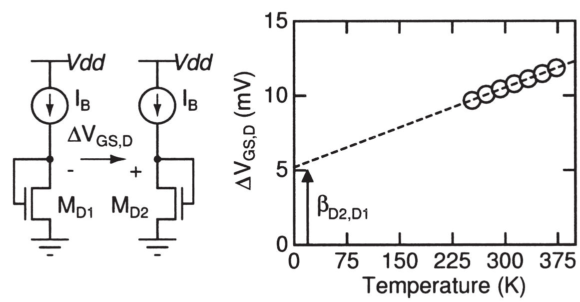

Fig. 4 Difference in gate-source voltage in two diode-connected transistors. The left portion is the schematic, and the right portion is the simulation results. The bias current I_B and the ratio of K_{D1}/K_{D2} are set to 100 nA and 1.25.

2.3 Bias-Voltage Subcircuit

The next part is to construct a subcircuit that supplies bias voltage V_{BIAS} to the constant-current subcircuit. This bias-voltage subcircuit must generate a constant voltage that is independent of temperature. Although a bandgap reference circuit [5] is widely used to obtain a constant voltage, it is not suitable for our purpose because, for low-current operation in the subthreshold region, it needs large resistors of high resistance. However, Buck and others proposed a new CMOS bandgap reference circuit without resistors [6]. We modified their circuit to operate in the subthreshold region and to generate a bias voltage for the constant-current subcircuit.

Figure 3 shows the circuit configuration. The circuit consists of two diode-connected transistors (M_{D1}, M_{D2}) and n differential pairs (M_1-M_2, M_3-M_4, $\cdots$,M_{2n-1}-M_{2n}) connected in a cascade. We set the aspect ratios of transistors such that

$$\begin{aligned} &K_{D1} > K_{D2}, \\ &K_1 > K_2, \\ &\text{and } \; K_{2i} > K_{2i-1} \quad (i = 2, 3, \cdots, n). \end{aligned} \tag{11}$$

The circuit produces a constant voltage on the output terminal V_{REF}. The output voltage is equal to the sum of the voltage across M_{D2} and the gate-to-gate voltages of the differential pairs. As shown later, the M_{D2} voltage shows a negative TC, whereas the gate-to-gate voltages show a positive TC; this enables us to generate a zero-TC voltage. The details of the circuit operation are as follows.

The diode-connected MOSFETs M_{D1} and M_{D2} are operated in the subthreshold region, and their gate-source voltages $V_{GS,D1}$ and $V_{GS,D2}$ are given by

$$V_{GS,Di} = V_{TH} + V_{OFF,Di} + \eta V_T \ln\left(\frac{I_B}{K_{Di} I_0}\right) \quad (i = 1, 2), \tag{12}$$

where I_B is the current through the MOSFETs. The temperature coefficient of this gate-source voltage is given by

$$\begin{aligned} \frac{\partial V_{GS,Di}}{\partial T} &= \frac{\partial V_{TH}}{\partial T} + \frac{\eta V_T}{T} \ln\left(\frac{I_B}{K_{Di} I_0}\right) \\ &\quad - \eta V_T \left(\frac{1}{\mu}\frac{\partial \mu}{\partial T} + \frac{1}{V_T^2}\frac{\partial V_T^2}{\partial T}\right) \\ &= -\kappa + \frac{\eta k_B}{q}\left(\ln\left(\frac{I_B}{K_{Di} I_0}\right) - (2 - m)\right). \end{aligned} \tag{13}$$

This equation includes I_0, but the temperature dependence of I_0 can be ignored because I_0 is contained in a logarithmic function. For ordinary MOSFET parameters, the gate-source voltage across M_{D2} shows a negative TC.

The difference $\Delta V_{GS,D}$ of the gate-source voltages in M_{D1} and M_{D2} can be expressed as

$$\begin{aligned} \Delta V_{GS,D} &= V_{GS,D2} - V_{GS,D1} \\ &= \beta_{D2,D1} + \eta V_T \ln\left(\frac{K_{D1}}{K_{D2}}\right), \end{aligned} \tag{14}$$

where $\beta_{D2,D1} (= V_{OFF,D2} - V_{OFF,D1})$ is the positive offset voltage as shown in Fig. 4. This voltage difference is applied to the left differential pair M_1-M_2. The resultant currents I_1 and I_2 in the differential pair are given by

$$I_i = K_1 I_0 \exp\left(\frac{V_{GS,Di} - V_S - V_{OFF,i} - V_{TH}}{\eta V_T}\right), \quad (i = 1, 2) \tag{15}$$

where V_S is the common source node voltage of the differential pair. Current I_2 is copied into M_4 of the next differential pair. Because the currents in transistors M_3 and M_4 are I_1 and I_2, the gate-source voltages $V_{GS,3}$ and $V_{GS,4}$ are given by

$$V_{GS,3} = V_{TH} + V_{OFF,3} + \eta V_T \ln\left(\frac{I_1}{K_3 I_0}\right) \tag{16}$$

and

$$V_{GS,4} = V_{TH} + V_{OFF,4} + \eta V_T \ln\left(\frac{I_2}{K_4 I_0}\right). \tag{17}$$

The gate-to-gate voltage ΔV_{GG}, or the difference of the gate-source voltages ($\Delta V_{GG} = V_{GS,3} - V_{GS,4}$) in the differential pair M_3-M_4 is given by

$$\begin{aligned} \Delta V_{GG} &= \beta_{3,4} + \eta V_T \ln\left(\frac{K_4 I_1}{K_3 I_2}\right) \\ &= \beta + \eta V_T \ln\left(\frac{K_4 K_1 K_{D2}}{K_3 K_2 K_{D1}}\right), \end{aligned} \tag{18}$$

where

$$\beta = \beta_{D2,D1} + \beta_{2,1} + \beta_{3,4}. \tag{19}$$

We set the aspect ratios such that

$$K_4 K_1 K_{D2} > K_3 K_2 K_{D1}, \tag{20}$$

then ΔV_{GG} shows a positive TC. In the same way, the successive differential pairs generate their gate-to-gate voltages. These voltages are added together in the array of the differential pairs. The output of the circuit is the sum of $V_{GS,D2}$ and the total of the gate-to-gate voltages. To produce enough output voltage to drive the MOS resistor in the strong-inversion region, we used a number of differential pairs. The output voltage of the circuit can be given by

$$V_{REF} = V_{GS,D2} + (n-1)\Delta V_{GG}. \tag{21}$$

We can obtain a constant voltage with a zero TC, adjusting the size of transistors and the number of differential pairs.

Figure 5 shows the simulated results for the output voltage of the circuit. In the simulation, the ratio of each of the transistor pairs shown in Table 1 was assumed, and the number of differential pairs was set to 5 (i.e., $n = 5$). An almost

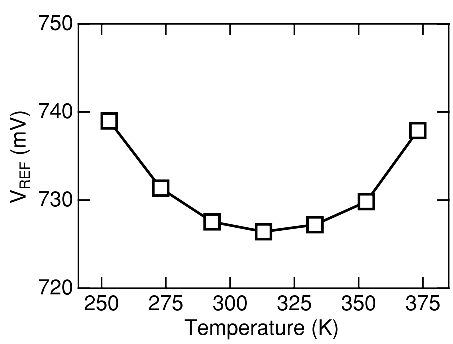

Fig. 5 Output of bias-voltage circuit as a function of temperature, simulated with parameters given in Table 1.

Table 1 Example of MOSFET's ratios.

$\frac{K_B}{K_A}$	$\frac{K_{D1}}{K_{D2}}$	$\frac{K_1}{K_2}$	$\frac{K_{i+1}}{K_i}$ (i=3,5,7,9)
1.06	1.25	3	3

constant voltage can be obtained in the temperature range, and the TC of the voltage is zero at room temperature. The voltage variation with the temperature can be suppressed within ± 1%. This variation is mainly ascribed to the nonlinearity of the gate-source voltages of the diode-connected transistors. Though both voltages of $V_{GS,D2}$ and ΔV_{GG} in Eq. (21), where $V_{GS,D2}$ is negative and ΔV_{GG} is positive, are nearly proportional to the temperature, they still have little nonlinear temperature dependence. Therefore, the output voltage changes nonlinearly as shown in Fig. 5.

3. Constructing the Current Reference Circuit

The current reference circuit we describe can be constructed by combining the constant current subcircuit and the constant voltage subcircuit. Figure 6 shows the entire configuration of the circuit. We modified the configuration of the constant-current subcircuit and added a source-coupled amplifier, to ensure the same current flowing in M_A and M_B. To use the source-coupled amplifier, we adapted a cascode configuration of nMOSFETs in the constant-current subcircuit. The source-coupled amplifier and the constant-current subcircuit construct the unity gain configuration. The voltage of V_A is monitored by the non-inverting terminal of the unity gain circuit, and then the output voltage of V_B is set at the same voltage with V_A. This ensures the same current value in transistors M_A and M_B. AC analysis of this unity gain circuit shows that the phase margin at the unity gain frequency is 45 degree, and the circuit is stable.

Figure 7 shows the simulated results for the output current I_{REF}. In this simulation, the ratio of K_B/K_A was set to 1.06. The variation in the current can be suppressed within ± 4% in the temperature range from −20 to 100°C.

The circuit is insensitive to a change in power supply voltage because of the feedback control with the source-coupled amplifier. Figure 8 shows the bias voltage V_{REF} and the output current as a function of the supply voltage. The circuit can operate at a low power voltage of 1.2 V. The variation in the bias voltage and the output current can be suppressed within ± 0.19% and ± 0.60%, respectively, in the supply voltage range from 1.2 to 3 V. Table 2 summarizes the performance of this current reference.

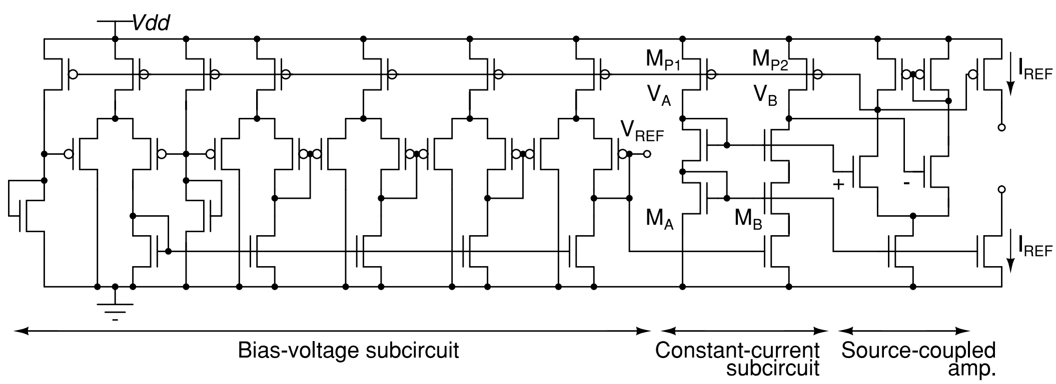

Fig. 6 Current reference circuit consisting of bias voltage subcircuit and constant-current subcircuit.

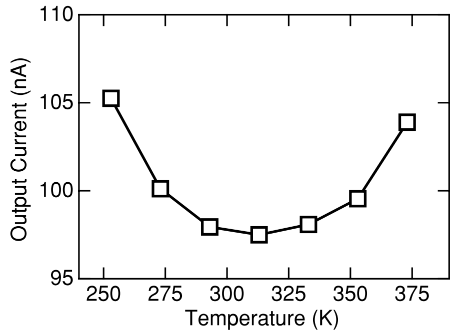

Fig. 7 Output of current reference circuit as a function of temperature, simulated with parameters given in Table 1.

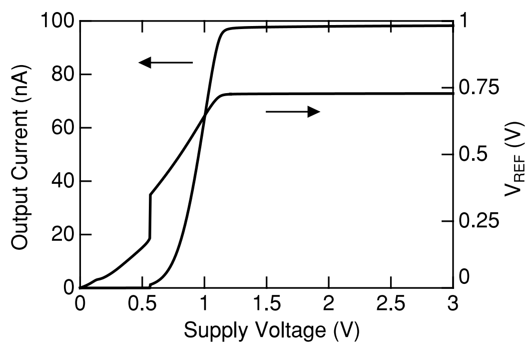

Fig. 8 Bias-voltage and output current as a function of supply voltage.

Table 2 Performance summary.

Technology	0.25 μm, 1-poly 5-metal CMOS
V_{DD}	1.5 V
I_{REF}	97.7 nA (T = 25°C)
V_{REF}	727 mV (T = 25°C)
Power	1.1 μW (T = 25°C)
$\Delta I_{REF}/I_{REF}$	± 4% (T = −20 – 100°C)
	± 0.60% (V_{DD} = 1.2 – 3 V)
$\Delta V_{REF}/V_{REF}$	± 1% (T = −20 – 100°C)
	± 0.19% (V_{DD} = 1.2 – 3 V)

The temperature dependence on the output current is somewhat larger than expected from Eq. (10). This was mainly caused by the variation in the bias-voltage with temperature that is shown in Fig. 5. Further improvements will be made possible by modifying the bias-voltage subcircuit. Equation (10) shows that the temperature that gives a zero TC increases as overdriving voltage V increases (see Fig. 2). Therefore, if we can construct a bias-voltage circuit that produces a voltage with an appropriate positive TC, then we will be able to create an improved current-reference circuit that shows a zero TC over a wide temperate range. We are now developing such a modified bias-voltage circuit.

4. Conclusion

We described an ultralow power constant current reference circuit with little temperature dependence. This circuit consists of a constant-current subcircuit and a bias-voltage subcircuit. and is useful as a reference current for a micropower application in an environment where the temperature changes. This circuit compensates for the temperature characteristics of mobility μ, thermal voltage V_T, and threshold voltage V_{TH} in such a way that the reference current has small temperature dependence. A SPICE simulation demonstrated that the reference current is 97.7 nA, and the variation in the reference current and the bias voltage can be kept very small within ± 4% and ± 1% in a temperature range from −20 to 100°C. The total power dissipation is extremely low, 1.1 μW. Standard CMOS technology can be used without a resistor.

Acknowledgment

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Appendix: Temperature Coefficient of Oguey and Aebicher’s Current Reference

The output current in their circuit [2] is given by

$$I = n^2 \mu C_{OX} K V_T^2 K_{eff}, \qquad \text{(A· 1)}$$

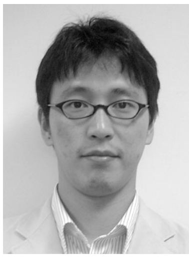
where n is a correction factor of low drain-source voltage ($n = \beta_{lin}/\beta_{sat}$), and K_{eff} is a function of the geometrical ratios of transistors. The TC is given by

$$TC_I = \frac{1}{I}\frac{dI}{dT} = \frac{1}{\mu}\frac{d\mu}{dT} + \frac{1}{V_T^2}\frac{dV_T^2}{dT} \qquad \text{(A· 2)}$$

and is reduced to

$$TC_I = -\frac{m}{T} + \frac{2}{T}. \qquad \text{(A· 3)}$$

Because the value of m is about 1.5 for ordinary MOSFETs, the temperature coefficient is always positive, and the current will increase as the temperature increases.



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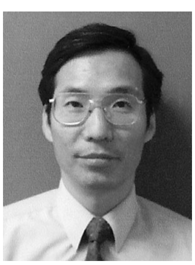

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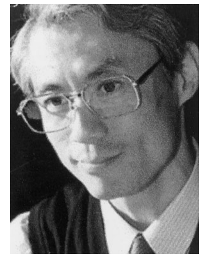

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