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Gate-Extension Overlap Control by Sb Tilt Implantation

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SUMMARY Antimony tilt implantation has been utilized for source and drain extension formation of n-MOSFETs. The tilt implantation is a very convenient method to provide adequate overlap between the extensions and a gate electrode. MOSFET drive current was effectively improved by the tilt implantation without degrading short channel effects. *key words:* MOSFET, extension, gate, overlap, tilt implantation, Sb

1. Introduction

Development of shallow junction formation techniques has been repeated in the history of MOSFET scaling for suppressing short channel effects. Reduction of junction depth sometimes results in higher sheet resistance and increase in parasitic resistance that reduces MOSFET drive current. There is another parameter of parasitic resistance, that is, gate-source/drain overlap length. From a device fabrication point of view, control of overlap between the extensions and gates is also a critical issue. Adequate overlap length is necessary to prevent a current crowding effect and obtain sufficient drain current. However, excess overlap length gives rise to increase in overlap capacitance, gate leakage current due to direct tunneling at off state and GIDL (Gate Induced Drain Leakage) current. These problems increase gate propagation delay or power dissipation.

Thompson et al. [1] utilized the offset spacer for extension implantation to obtain various overlap length and to investigate the influences on device characteristics. They indicated that adjustment of overlap length was a trade-off issue between drive current and parasitic capacitance. Offset spacer is the most popular method to optimize p⁺ extension overlap for leading-edge devices [2], [3]. Since combination of B⁺ implantation and RTA or spike annealing gives rise to relatively large lateral diffusion, the offset spacer is suitable for p-MOSFETs fabrication. In the case of As for n-MOSFET, lateral diffusion is not so large compaerd with B. This makes overlap length adjustment difficult instead of relieving the problem, since the side wall spacer technique needs moderate lateral diffusion. Currently integration of milliseconds annealing, such as non-melt laser annealing [4], [5] and flash lamp annealing [5], for MOSFET fabrication is extensively investigated. These new annealing

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methods can provide nearly-zero diffusion dopant activation even for B. That may result in too short overlap length to keep parasitic resistance low enough. To avoid this situation, annealing condition is sometimes tuned to enlarge diffusion during annealing. However, this increases not only overlap length but also junction depth.

In this work, we have used Sb⁺ tilt implantation for n^+/p source/drain extension formation. In this technique, overlap length is modified by implantation angle. If the lateral diffusion during annealing process is large, the tilt implantation will not be effective to modify the overlap length. Therefore, tilt implantation is suitable for low diffusive dopants or the nearly-zero diffusion annealing. Since Sb has low diffusive nature, it is suitable for extension formation by tilt implantation.

Antimony implantation technique that has significant features as a shallow junction formation method was utilized in this work. Antimony is suitable for n⁺ extension formation because of its heavy mass and low diffusive nature. We have reported 20 nm junction formations with Sb⁺ implantation and conventional RTA method [6]-[8]. Very low sheet resistance, $260 \Omega/sq$. was obtained for such ultrashallow junctions. We have also reported combination with melt-laser annealing for 10 nm junction formation [9], [10]. Different from B and As that are popularly used for extension formation, Sb junction depth is not dominantly defined by diffusion during activation annealing but by implanted depth. Hence, the overlap length of Sb extensions can be modified simply by implantation angle with good controllability. Effectiveness of the tilt implantation will be shown with fabricated MOSFETs characteristics. Relationships between overlap length and device characteristics are also discussed with SIMS depth profiles and process and device simulation.

2. MOSFET Fabrication and Dopant Profiles

We have fabricated n-MOSFETs with the Sb extensions to evaluate the influence of overlap length. Figure 1 shows the process flow for fabricated n-MOSFETs and major process parameters. Gate oxide thickness was 2 nm and gate lengths were in the range of 50 nm to 20 μ m. Sb implantation energy was 10 keV that realizes 20 nm junctions, as described later. The most heavy thermal treatment process after the extension implantation was the second annealing for Ti salicidation at 850°C for 60 s.

Prior to real fabrication, two-dimensional Sb profiles

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- Gate oxidation: 2nm
- Gate formation
- Screen oxide deposition: HTO 5nm
- Sb⁺ Extension implantation: 0°, 30° 10 keV, 3x10¹⁴ cm⁻²
- Sidewall spacer formation
- Deep S/D implantation
- Recrystallization RTA: 800°C, 3s
 Annealing for Ti salicidation and
- dopant activation 1st anneal: 650°C, 60s 2nd anneal: 850°C, 60s

Fig. 1 Fabrication process flow of MOSFETs.



Fig. 2 Simulated two dimensional Sb profiles for (a) vertical (0°) and (b) tilt (30°) implantation. Implantation energy and dose were 10 keV and 3×10^{14} cm⁻³, respectively.

around the gate edge just after the implantation were obtained with the process simulator TSUPREM4. Figures 2(a) and (b) represent simulated two-dimensional Sb profiles for vertical (0°) and tilt (30°) implantation, respectively. Screen oxide thickness, implantation energy and implantation dose were 5 nm, 10 keV and 3×10^{14} cm⁻³, respectively. As shown in Fig. 2(b), the 30° tilt implantation leads to 15 nm overlap, while only 2.5 nm overlap is obtained in the vertical case as shown in Fig. 2(a). Here, overlap length was obtained at the Si surface assuming that substrate doping concentration was 1×10^{18} cm⁻³. Improvement in surface Sb concentrations at the gate edge by the tilt implantation from less than 1×10^{19} cm⁻³ to 1×10^{20} cm⁻³ is also noteworthy. These results indicate that the vertical Sb implantation leads to nearly zero-overlap extension formation as long as its diffusion is negligible. Figure 3(a) shows Sb SIMS depth profiles for as implanted and after annealing. Sb was vertically implanted into Si with the same conditions as Fig. 2(a) case. The junction depth defined at $1 \times 10^{18} \text{ cm}^{-3}$ for after annealing at 850°C for 60 s is almost same as that for the asimplanted. The simulated as-implanted profile in Fig. 2(a) agrees well with that for the SIMS profile. Redistribution of Sb by RTA is mainly observed at high concentration region where Sb concentration is larger than 10^{19} cm^{-3} . A profile peak shows shift towards the surface by the annealing. This is due to the pileup formation [6]-[8] that gives rise to reduction in electrically active dopant at the surface. The influence of pileup formation is discussed later. Figure 3(b)



Fig.3 Sb SIMS depth profiles. (a) as implanted and after annealing for 0° implantation. (b) after annealing for 0° and 30° implantation.

shows Sb SIMS depth profiles for 0° and 30° implantation after 850°C 60 s annealing. Profile for 30° is very similar to 0° except for small change in effective projection range due to the angle difference. So we can expect the overlap length is controlled by the tilt angle without changing the junction depth.

3. Device Characteristics

Figure 4(a) shows I_D-V_G characteristics of fabricated MOS-FETs. The poly-Si gate lengths (L_{Poly}) for 0° and 30° are 125 nm and 150 nm, respectively. In the case of the 30° tilt implantation, Sb was implanted from both source and drain side with a half dose. Tilt implantation results in reduction in effective gate length. Metallurgical distance between source and drain, L_{met} , was obtained using the following formula, to avoid confusion due to device characteristics



Fig. 4 I_D-V_G characteristics of fabricated nMOSFETs for (a) short channel ($L_{met} = 120 \text{ nm}$) and (b) long channel ($L_{met} = 945 \text{ nm}$).

dependence on the effective gate length:

$$L_{met} = L_{poly} - 2L_{ovi}$$

where L_{poly} was experimentally evaluated patterned gate length and Lovl was the overlap length of source/drain and gate obtained with 2D simulation. L_{met} for the both devices whose $I_D - V_G$ characteristics are shown in Fig. 4 was calculated to be 120 nm. Figure 4(b) shows $I_D - V_G$ characteristics for long channel ($L_{met} \sim 945 \text{ nm}$) MOSFETs. In the case of the short channel devices in Fig. 4(a), FET on-current I_{on} (I_D @ $V_G = V_D = 1.5$ V) is much improved by the tilt implantation. On the other hand, in the case of the long channel devices in Fig. 4(b), I_{on} for 30° and 0° are almost same. As L_{met} is reduced, channel resistance, in general, decreases. On the other hand, overlap resistance is independent of gate length. Therefore, current reduction due to overlap resistance is large in the short channel devices. Threshold voltage roll-off due to drain induced barrier lowering in the short channel devices is about 70 mV for both 0° and 30° devices. Figure 5 shows relationship between threshold voltage and L_{met} . Threshold voltage roll-off curves for 0° and 30° were almost identical to each other. As described with Fig. 3(b),



Fig. 5 Comparison of threshold voltage roll-off characteristics for 30° and 0° implantation.



Fig. 6 Comparison of I_D-V_D characteristics of source/drain asymmetric devices. (a) source-overlap and (b) drain-overlap devices.

junction depth was not affected by the implantation tilt angle. Since device parameters other than the tilt implantation angle are common for both 0° and 30° devices, coincidence in DIBL and roll-off characteristics shown in Fig. 5 is understood to be natural. Increase in L_{ovl} sometimes leads to increase in GIDL. However, GIDL for the fabricated devices was sufficiently low under the practical gate bias condition regardless of the tilt angle, as shown in Fig. 4. Figure 6 shows $I_D - V_D$ characteristics of an asymmetrical extension device fabricated with single side Sb implantation with the full dose. Since parasitic resistance at source side gives rise to large current reduction by the body effect due to the potential drop at the parasitic resistance, drain current for a drain-side-overlap condition is lower than that for a sourceside-overlap condition. The source-side-overlap device has another merit that gate-drain overlap capacitance can be reduced without degrading drain current [11].

4. Comparison with Simulated Data

Figure 7 shows comparison of current drive performance between device simulator MEDICI and fabricated MOSFETs. In this simulation, L_{met} was fixed to be 95 nm and overlap length was modified in the range of -25 nm to 25 nm. Reduction in I_{on} due to small overlap is more significant in fabricated MOSFETs than simulated results. To explain this discrepancy, the Sb concentration at the Si surface after activation annealing was considered. Figure 8 shows simulated Sb depth profile after annealing based on fitting between simulated and SIMS profiles [8]. Implantation energy and dose were 10 keV and 3×10^{14} cm⁻³. Annealing temperature and time were 850°C and 30 min, respectively. Sb forms pileup at the Si surface, in other words, at the SiO₂/Si interface. We have assumed that Sb atoms are trapped at the surface in the simulation. The trapped Sb is observed as a pileup in SIMS profiles with finite spreading due to SIMS depth resolution. The pileup is not clearly observed in Fig. 3. However, profile peak shift towards the surface by



Fig.7 Comparison of simulated and measured current drive performance as a function of overlap length.

annealing is attributed to the pileup formation. In the previous work, we showed that piled-up Sb atom works as the seed for precipitation growth. Once precipitation or cluster was formed. Sb atoms included them are considered to be electrically inactive [6]. Therefore, the trapped Sb should be subtracted from SIMS profiles to estimate profile for electrically active Sb, as shown in Fig. 8. As a result, Sb concentration underneath the surface reduces. Since the annealing time for Fig. 8 was longer than that for the fabricated MOS-FETs, the influence of reduction in the surface Sb concentration is qualitatively explained with Fig. 9. In this figure, electrically active Sb concentration underneath the Si surface is assumed to reduce to 1/4 by annealing. The lateral shift of concentration contour due to the surface concentration reduction is illustrated by broken lines in Fig.9. Reduction in L_{ovl} for the 0° implantation is larger than the 30° case. The as-implanted profile for the 0° implantation is



Fig. 8 Simulated Sb depth profile after annealing. Electrically inactive pileup atoms were subtracted from the entire SIMS profile.



Fig. 9 Schematic explanation of influence caused by reduction in the surface Sb concentration. Sb concentration underneath the Si surface was assumed to reduce to 1/4 by annealing. The shift of concentration contour for 1×10^{19} cm⁻³ are illustrated by broken lines.

Gaussian-like, that for the 30° implantation has a plateaulike peak as shown in Fig. 2. This difference leads to the larger lateral shift for the 0° case, in other words, larger reduction in L_{ovl} and increase in larger drain current reduction shown in Fig. 4.

5. Conclusions

In this work, the extension formation by Sb tilt implantation was demonstrated as an effective gate-extension overlapcontrol method. By this technique, ultra shallow junction with moderate overlap length can be formed with no complicated additional processes, such as the side wall spacer formation. Current drive performance was improved by the tilt extension implantation. Low diffusion dopant such as Sb, needs the tilt implantation to obtain the sufficient overlap length. Comparison of FET characteristics between fabrication and simulation indicated that active dopant reduction by pileup formation at the Si surface was an important factor that affects drain current.

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