IEICE TRANS. INF. & SYST., VOL.E91–D, NO.3 MARCH 2008

PAPER Special Section on Test and Verification of VLSIs

Ramp Voltage Testing for Detecting Interconnect Open Faults

Yukiya MIURA[†a)], *Member*

SUMMARY A method for detecting interconnect open faults of CMOS combinational circuits by applying a ramp voltage to the power supply terminal is proposed. The method can assign a known logic value to a fault location automatically by applying a ramp voltage and as a result, it requires only one test vector to detect a fault as a delay fault or an erroneous logic value at primary outputs. In this paper, we show fault detectability and effectiveness of the proposed method by simulation-based and theoretical analysis. We also expose that the method can be applicable to every fault location in a circuit and open faults with any value. Finally, we show ATPG results that are suitable to the proposed method.

key words: *CMOS circuits, defect oriented testing, open faults, ramp voltage*

1. Introduction

As the present deep-submicron VLSI operates under a low voltage supply and a high frequency, the influence caused by open faults becomes noticeable. Since present VLSIs are fabricated by using copper process technologies and multiple metal layers, via open defects and contact open defects often occur [1], [2]. As a result, interconnect open faults occur, which means breaks of signal lines between gates. Therefore, detecting open faults is important for obtaining high reliable products. Note that it is said that the open fault in the source/drain terminal of a transistor (e.g. the stuck-open fault) can be detected by traditional two-pattern test [3], [4].

Application of logic testing (e.g., stuck-at faults testing) to detect open faults is reported [5]–[8]. Especially, it is said that n-detection testing is useful for detecting open faults because it can apply n different test vectors for exciting a fault and propagating its effect [9]. However, voltages of signal lines around the fault location depend on applied test vectors, and the voltage at the fault location depends on the balance of wire capacitances between the VDD and GND sides, and as a result, open fault detection by logic testing is difficult even if we use n-detection testing [10]. Thus, the open fault cannot be necessarily detected by traditional logic testing.

If a known voltage (logic value) can be compulsorily set to the fault location, fault detection by logic testing can be realized easily. Based on this motivation, we have proposed a new method for detecting interconnect open faults by applying ramp voltage to power supply terminals, where an initial voltage (initial logic value) at a fault location is automatically assigned when the ramp voltage is applied [11]. Note that Gyvez et. al. proposed a ramp voltage method for detecting faults in analog circuits by IDDQ testing [12]. The objective of their method is to change the states of transistors and to obtain a current signature. In this sense, their situation for the ramp voltage application is different with us.

In this paper, we show fault detectability and effectiveness of the proposed method by using simulation and theoretical analysis. We also expose that the method is applicable for detecting interconnect open faults with any value. Finally, we show ATPG results that are suitable to our testing method, where test generation is done so that the number of signal lines assigned logical values by a test vector is as smaller possible. Note that this paper does not target complete interconnect open (floating gate) faults.

This paper is organized as follows. Section 2 describes a method for detecting interconnect open faults. Section 3 shows effectiveness of the proposed method by using simulation results and theoretical analysis. We also show ATPG results that are suitable to the proposed method in Sect. 4. Section 5 concludes this paper.

2. Preliminary

2.1 Interconnect Open Faults

In this paper, we consider interconnect open faults between two gates as shown in Fig. 1. In general, interconnect open faults are modeled by a RC circuit [13], [14], where Rf is an open resistance and Cw1 (Cw2) is a total wire capacitance between the signal line having an open fault and signal lines having the VDD (VSS) voltage. The value of Rf originates in a fault itself and values of Cw1 and Cw2 originate in design and technology. We call values of these Rf, Cw1 and

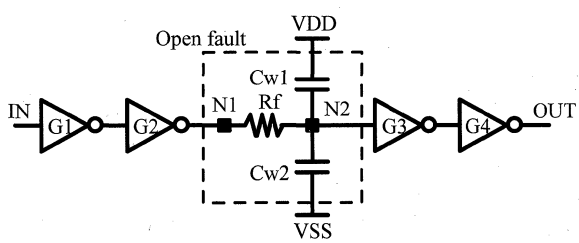

Fig. 1 Open fault model and simulation circuit.

Manuscript received April 6, 2007.
Manuscript revised August 3, 2007.

[†]The author is with the Faculty of System Design, Tokyo Metropolitan University, Hino-shi, 191–0065 Japan.
a) E-mail: miura@tmu.ac.jp

DOI: 10.1093/ietisy/e91–d.3.700

Cw2 open fault values generically. In this paper, we show that our method is applicable to the open fault value of wide range. We use the circuit of Fig. 1 for simulation; however, we show that the proposed method is applicable to general CMOS combinational circuits by using an equivalent circuit. Here, based on the fault location, G2 is called a diving gate and G3 is called a driven gate. The inversion gate located in the odd (even) number counting from a primary input is called an odd (even) inversion gate.

Open faults may exist in the gate terminal of either nMOS or pMOS transistors, which result in a transistor-interconnect open fault. We do not consider them in this paper; however, we obtained similar results for them if we used the proposed method [15].

2.2 Principle of Open Fault Detection

The difficultness of open fault detection by logic testing comes from assignment of a known voltage to the open fault location. In order to improve this problem, we have proposed the following testing method (Fig. 2 (a)) [11].

(1) All input terminals including power supply terminals of the circuit are set to the GND level (0 V) at time 0 [t0] so that all internal nodes in the circuit can be set to the GND level.
(2) A positive ramp voltage with a certain slope is applied to the VDD terminal during the interval [t1, t2]. Logic 0 is automatically applied to the fault location since primary inputs are still the GND level. This approach prevents to change rapidly the voltage of the open fault location. Determination of the slope of a ramp voltage is described in Sect. 3.2.
(3) After the node voltage fully settles down [t3], apply one test vector from primary inputs to change the logic value at the open fault location, propagate it to the primary output, and observe an output value at a predetermined time [t4]. We can set time t3 to arbitrary time if we use a ramp voltage with an enough gentle slope as the VDD signal. We call the interval [t0, t3] an initializing interval. ATPG for the proposed method is described in Sect. 4.1.
(4) If the output value does not change within a specific time interval [t4], we find there is an open fault and finally, we can judge the CUT is faulty. Note that the specific interval usually corresponds to one clock period of the at-speed of the circuit under test. We call the interval staring from [t3] a testing interval.

In the above procedure, if we apply a negative ramp voltage to the VSS terminal in the above step (2) as shown in Fig. 2 (b), the initial value at the fault location is logic 1 and logic 0 for the testing interval. Therefore, our testing method can set both logic values as the initial value.

Considering the above procedure, the equivalent circuit of Fig. 1 is represented by the RC differential circuit of Fig. 3 (a) when N1 = VSS = GND and $V_i(t)$ = (positive voltage). Here, if we apply the negative voltage to the VSS terminal (i.e., N1 = VDD = GND, $V_i(t)$ = (negative voltage)), the equivalent circuit becomes one of Fig. 3 (b).

In the RC differential circuit of Fig. 3 (a), the voltage of the N2 node, V_{N2}, is expressed as follows if the ramp voltage, $V_i(t) = kt$ and $V_i(0) = 0$, is applied [16]:

$$V_{N2}(t) = k \cdot Cw1 \cdot Rf \cdot \left(1 - e^{-\frac{t}{Rf(Cw1+Cw2)}}\right) \quad (1)$$

If the initial voltage of $V_i(0)$ is V_0, the V_{N2} voltage is given

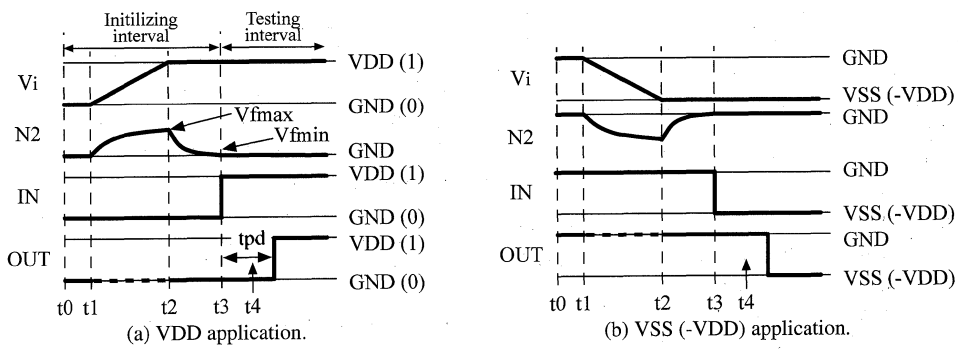

Fig. 2 Testing method.

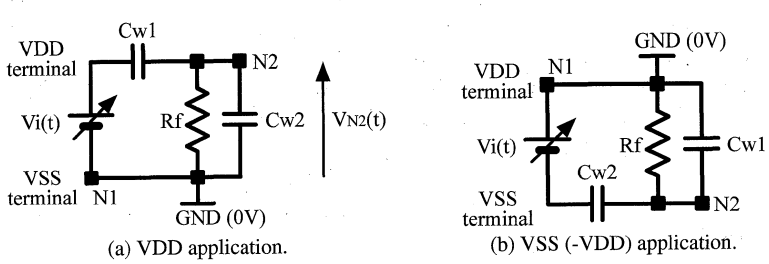

Fig. 3 Equivalent circuit during [t1, t2].

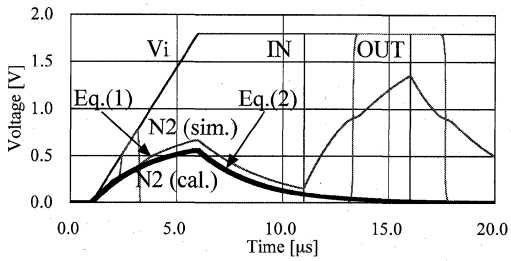

Fig. 4 Simulation results.

as follows:

$$V_{N2}(t) = \frac{Cw1}{Cw1 + Cw2} \cdot V_0 \cdot e^{-\frac{t}{Rf(Cw1+Cw2)}} \quad (2)$$

Note that coefficient $(Cw1/(Cw1 + Cw2))V_0$ of the right-hand side of Eq. (2) results in V_{N2}(t2) obtained from Eq. (1) because $V_{N2}(t)$ at t2 is given by Eq. (1) when t = t2. Here, the time constant τ of the differential circuits of Figs. 3 (a) and 3 (b) is $Rf(Cw1 + Cw2)$.

Figure 4 shows simulation results of the faulty circuit of Fig. 1 whose simulation conditions are as follows: (CMOS process) = TSMC-0.18 μm (MOSIS), Rf = 100 MΩ, $Cw1$ = 16 fF, $Cw2$ = 8 fF. During the ramp voltage application [t1, t2], the voltage of the node N2 that is the fault location is relatively stable because all of internal nodes are set to the GND voltage. The bold line shows the result of theoretical analysis by using the circuit of Fig. 3 (a) (i.e., result by Eqs. (1) and (2)), which agrees with that of the fault circuit. Then, this equivalent differential circuit is a reasonable model of the circuit with the open fault. In this simulation, although the circuit has approximately 2 μs delay times, it functions normally.

The equivalent circuit of VDD (VSS) application for faults at even inversion gates corresponds to one of VSS (VDD) application for faults at odd inversion gates. Therefore, the proposed method is applicable to open faults at every location of CMOS combinational circuits.

3. Effectiveness of the Proposed Method

To verify the proposed method, we show results of circuit simulation and theoretical analysis of equivalent circuits, and expose that we can estimate electrical behaviors by a local circuit analysis. Table 1 shows simulation conditions, where we use the TSMC 0.18 μm technology [17]. Here, the wire capacitance of 8 fF corresponds to a total wire capacitance between metal 6 of 20 μm-length and 0.5 μm-width and all other layers. In the following sections, we evaluate voltages of the open fault location, Vfmax (the maximum voltage of N2 at t2) and Vfmin (the minimum voltage of N2 at t3), and the delay time for fault detection, tpd (the interval between 50% transition points of nodes IN and OUT) (see Fig. 2 (a)).

3.1 Theoretical Analysis for Open Faults

Table 2 shows the relationship between the voltage application and the wire capacitance for several Rf values. A test that makes the voltage of the fault location stable is suitable in the proposed method. From Eq. (1) and simulation results, we find that the N2 voltage is proportional to Cw1 if the slope is constant for the positive power supply application. For the negative power supply application, the opposite phenomena occur because the equivalent circuit is denoted by the circuit of Fig. 3 (b) (i.e., the role of Cw1 and Cw2 is exchanged). In addition, results of Table 2 also correspond to those of the VSS application for faults at odd inversion gates because of the relationship between equivalent circuits of Fig. 3. From these facts, the following test is proper to achieve our objective.

Table 1 Simulation conditions.

Technology	TSMC 0.18μm (MOSIS)
VDD	1.8V
Vtp, Vtn	-0.52V, 0.51V
Typical gate	L=0.18μm, Wp/Wn=3.3μm/1.0μm
Gate threshold	(1/2)VDD
Rf	1kΩ ~ 100MΩ
Cw1, Cw2	8fF ~ 80fF
t0, t1, t2, t3	0μs, 5μs, 25μs, 45μs
Vi(t)	(1.8V/20μs)t, (-1.8V/20μs)t

(a) For the fault at the even inversion gate, we need to use the positive (negative) power supply application if $Cw1 < Cw2$ ($Cw1 > Cw2$) (e.g., simulation no. S1).
(b) For the fault at the odd inversion gate, we need to use the negative (positive) power supply application if $Cw1 < Cw2$ ($Cw1 > Cw2$).

If load capacitances of the driven gate have an enough impact for wire capacitances at the fault location, their effects appear for the voltage at the fault location and the delay time at the primary output. In the simulation S2 (S3), transistor sizes of the driven gate G3 are 5 (10) times of those of the typical gate. From these results (i.e., the column of "Theory of w/o CL"), N2 voltages and propagation delays depend on not only open fault values but also driven gate sizes. In the rest of the paper, we take the load capacitance of the driven gate into account in theoretical circuit analysis. Since a faulty circuit can be modeled by the RC circuit of Fig. 3 (a), wire capacitances of $Cw1$ and $Cw2$ can be rewritten as follows:

$$Cw1 \leftarrow Cw1 + CLp, \quad Cw2 \leftarrow Cw2 + CLn$$

Here, the load capacitance of a transistor consists of the diffusion capacitance and the gate capacitance whose values depend on a transistor's operation. For the simple discussion, we consider worst values of load capacitances; for instance, CLp = 7.73 fF and CLn = 2.50 fF for the typical gate size. Therefore, theoretical V_{N2} values obtained from the equivalent circuit show worst values compared with those of simulation results (i.e., actual values are within the safety side). As shown in the column of "Theory with CL" on Table 2, results of the theoretical analysis considering the load capacitance agree well with those of the SPICE simulation even if the value of Rf is small (simulation no. S4

Table 2 Results of circuit simulation and theoretical analysis.

Sim. No.	Test & Circuit types	Rf, Cw1,Cw2 [MΩ] [fF]	Simulation Vfmax [mV]	Simulation Vfmin [mV]	Simulation tpd [μs]	Theory w/o CL Vfmax [mV]	Theory w/o CL Vfmin [mV]	Theory w/o CL tpd [μs]	Theory with CL Vfmax [mV]	Theory with CL Vfmin [mV]	Theory with CL tpd [μs]
S1	Typical gates VDD application	100, 80, 8	698.9	90.2	6.76	645.8	66.5	6.10	686.5	89.6	6.81
		100, 8, 8	146.0	0.042	2.05	72.0	0.0	1.11	141.5	0.069	1.82
		100, 8, 80	127.1	16.2	6.72	64.6	6.7	6.10	123.1	16.1	6.81
S2	G2=typ, G3=5*typical VDD application	100, 80, 8	816.2	182.4	8.91	645.8	66.5	6.10	788.7	172.9	9.13
		100, 8, 8	375.3	11.4	5.53	72.0	0.0	1.11	349.4	12.3	4.14
		100, 8, 80	299.9	63.8	9.91	64.6	6.7	6.10	282.8	62.0	9.13
S3	G2=typ, G3=10*typical VDD application	100, 80, 8	879.8	304.4	11.26	645.8	66.5	6.10	876.3	275.5	11.98
		100, 8, 8	577.8	74.2	8.87	72.0	0.0	1.11	543.4	74.8	6.99
		100, 8, 80	458.9	140.1	12.88	64.6	6.7	6.10	432.0	135.8	11.98
S4	Typical gates VDD application	100k, 80, 8	0.80	0.0	6.87n	0.72	0.0	6.10n	0.79	0.0	6.81n
		100k, 8, 8	0.15	0.0	1.70n	0.072	0.0	1.11n	0.14	0.0	1.82n
		100k, 8, 80	0.15	0.0	7.04n	0.072	0.0	6.10n	0.14	0.0	6.81n
S5	Typical gates VDD application	1k, 80, 8	13.43μ	0.0	0.64n	7.20μ	0.0	0.061n	7.90μ	0.0	0.068n
		1k, 8, 8	2.75μ	0.0	0.34n	0.72μ	0.0	0.011n	1.42μ	0.0	0.018n
		1k, 8, 80	2.75μ	0.0	0.64n	0.72μ	0.0	0.061n	1.42μ	0.0	0.068n

and S5), where their differences are within 3.3% for Vfmax and Vfmin.

By using our testing method, the delay time caused by a fault is proportion in the time constant because the interconnect open fault is modeled by the RC difference circuit and its time constant is $Rf(Cw1+Cw2)$. Then, in the theoretical analysis by the RC difference circuit, the delay time is proportion in the time to reach the voltage of 50% of VDD at the fault location. We can also estimate that the delay time is 0.69τ where the fault has the time constant τ. The tpd column of "Theory" in Table 2 shows calculation results, where those values are almost consistent with simulation results (Their differences are within 8.4%).

3.2 Application to Various Open Fault Value

According to Eq. (1), since the voltage of N2 is mainly in proportion to both k and $Cw1Rf$, we can estimate the voltage change of the fault location N2 as follows: Since the N2 voltage is easy to rise as $Cw1Rf$ becomes larger, to prevent the voltage rising of N2, it is necessary to apply a ramp voltage with a small k (i.e., a ramp voltage with a gentle slope). If we can determine the maximum value of $Cw1Rf$ to be detected in advance, we can set the slope k to prevent voltage rising at the fault location. Therefore, determination of k depends on the maximum value of the open fault to be detected.

For instance, if we assume that Vfmax is almost the same even if an open fault value is changed, we can calculate the slope k of a fault with $(Rf, Cw1, Cw2)$ for the given standard values $(k_0, t_0, Rf_0, Cw1_0, Cw2_0)$ as follows:

$$k = \frac{m \cdot n}{m+n} \tag{3}$$

$$m = \frac{Cw1_0 \cdot Rf_0 \cdot \left(1 - e^{-\frac{t_0}{Rf_0(Cw1_0+Cw2_0)}}\right)}{Cw1+Rf} \cdot k_0 \tag{4}$$

$$n = -\frac{VDD}{Rf(Cw1+Cw2)} \tag{5}$$

Table 3 shows those calculation and simulation results

Table 3 Calculation of ramp voltage slope.

#	Rf, Cw1,Cw2 [MΩ] [fF]	k [mV/μs]	Simulation Vfmax [mV]	Simulation Vfmax/VDD [%]	Theory Vfmax [mV]	Theory Vfmax/VDD [%]
#	100, 80, 8	90	698.9	38.8	686.5	38.1
	0.1, 80, 8	78251	653.6	36.1	620.5	34.5
	1, 80, 8	7825	645.6	35.9	620.5	34.5
	10, 80, 8	783	638.3	35.5	620.5	34.5
	100, 80, 40	78	575.3	32.0	569.1	31.6
	100, 80, 80	78	514.0	28.6	508.8	28.3
	100, 8, 8	436	563.5	31.3	544.0	30.2
	100, 8, 40	436	356.4	19.8	348.4	19.4
	100, 8, 80	401	237.9	13.2	231.3	12.9

for the standard Vfmax (indicated by #), where we can obtain almost the same Vfmax value for several parameters. Note that calculation results obtained from the above equations give approximate estimates because Eq. (1) represents the response of the equivalent circuit and load capacitances of the driven gate vary with transistor's operation. Since the value of the exp function of Eq. (1) becomes larger as the $Cw2$ value becomes larger, Vfmax becomes smaller. Then, we can set the V_{N2} value to a safety side.

On the other hand, if an open fault value is small, the delay time tpd by the fault is also small because the time constant of the fault is $Rf(Cw1+Cw2)$. If we wish to detect a fault with a small fault value, we need to set the observation time at the primary output to the minimum estimated delay time caused by an assuming fault and the minimum measurable value by an instrument. Therefore, the observation time at the primary output corresponds to the minimum value of a fault to be detected.

From these discussions, our testing method can apply to interconnect open faults with values of wide range by adjusting the slope k of the ramp voltage and observation time t4 at the primary output.

4. Test Vectors and Related Phenomena

4.1 ATPG Results

In the proposed method, an initial logic value at a fault location is automatically assigned when a ramp voltage is ap-

plied. Then, only one test vector is needed, which has to assign a complementally logical value to the fault location and propagate it to the primary output. Therefore, test generation algorithm is just the same as that for stuck-at faults. For the proposed testing method, it is desirable that wire capacitances, $Cw1$ and $Cw2$, around a fault location are almost constant during the testing interval. In order to achieve this purpose, we generate test vectors so that the number of signal lines whose logical values are assigned by a test vector is as small as possible (i.e., the number of signal lines with don't care (X) values is as larger as possible).

Table 4 shows results of such test generation based on the PODEM algorithm where we can obtain the fault efficiency of 100% for every circuit. The column "PODEM" shows ATPG results by the original PODEM algorithm. From the most left column, the table shows the number of test vectors and the average value, maximum value, and minimum value of the number of signal lines with specified logical values. The column "Proposed" shows ATPG results by the proposed method (modified PODEM algorithm). For both methods, don't care at primary inputs (unspecified PIs) after generating a test vector remains. In addition to this, for the proposed method, a path selection in the backward/propagation operation is carried out so that the number of signal lines that is assigned logical values by a test vectors is much smaller than possible.

We use the following heuristic measurement for the path selection. Assume that a present tracing gate during the backward/propagation operation is Gp. Let $\{G1, G2, \ldots, Gn\}$ be a set of gates feeding/connecting to the gate Gp. $Lv(G)$ denotes a level of a gate G (i.e., the maximum number of stages from PI to G (from G to PO for the propagation operation)), and In(G) denotes the number of input lines of G that we must assign logical values for the backward/propagation operation. We select a gate to minimize the value $S(Gi)$ of the following equation.

$$S(Gi) = \frac{In(Gi)}{Lv(Gp) - Lv(Gi)}, \quad (1 \leq i \leq n) \tag{6}$$

By using the equation, we can select a partial path that can minimize the number of lines with specified logical values.

Although the number of test vectors by the proposed ATPG method increases by approximately 46.5% than that of the original PODEM on the average, the number of lines with don't care increases by approximately 27.3%. Therefore, we can stabilize the wire capacitances around the fault location if we use the test vectors generated by the proposed method.

We compared our ATPG results with those of Ref. [18] that regenerates test vectors with don't care primary inputs as many as possible for a given uncompacted test set. Although the number of tests is small, the number of lines with signal values is large. There is the trade-off between the number of test vectors and the number of signal lines with specified values. Therefore, we need to find optimum their values from the viewpoint of a testing cost.

4.2 Effect of Change in Wire Capacitances

Even if we use test vectors described the above, signal values around the fault location will change after a test vector is applied. In this situation, we can consider the following condition for applying a test vector at time t3 (see. Fig. 2). Note that the total wire capacitance, $Cw1 + Cw2$, around any signal line never changes because circuit design does not change.

$$Cw1 \leftarrow Cw1 \pm \Delta Cw, \quad Cw2 \leftarrow Cw2 \mp \Delta Cw,$$
$$Cw1 + Cw2 = \text{constant}$$

When a test vector is applied and voltages of signal lines around a fault location change, the faulty circuit behaves like a step-voltage application. According to Eq. (2), the voltage at the fault location is in proportion to $Cw1/(Cw1 + Cw2)$ mainly. Therefore, the voltage at the fault location becomes higher (lower) for the VDD application as $Cw1$ ($Cw2$) is larger, and as a result, the delay time caused by the fault becomes shorter (longer) compared with unchanged wire capacitances. We can obtain the opposite relationship for the VSS application.

Table 5 shows simulation results when wire capacitances change at time t3. The VDD (VSS) application is better for $Cw1 < Cw2$ ($Cw1 > Cw2$) (indicated by # in Table 5). However, if the wire capacitances, $Cw1$ and $Cw2$, change when the test vector is applied, and the delay time decrease, then the other test type is appropriate for

Table 4 Evaluation of the number of signal limes with specified values.

Circuits	PODEM *				Proposed *				Ref. [18] *			
	# Tests	Ave. (%)	Max.	Min.	# Tests	Ave. (%)	Max.	Min.	# Tests	Ave. (%)	Max.	Min.
c432	155	234 (54.2)	422	49	223	150 (34.7)	347	28	53	294 (68.1)	404	166
c499	125	309 (61.9)	499	92	165	254 (50.9)	499	55	65	417 (83.6)	499	287
c880	363	398 (45.2)	745	90	512	310 (35.2)	627	50	76	650 (73.9)	866	406
c1355	204	504 (37.2)	1355	148	304	412 (30.4)	1355	74	94	1010 (74.5)	1355	625
c1908	258	645 (33.8)	1782	377	385	466 (24.4)	1412	120	131	1337 (70.1)	1749	288
c2670	701	1204 (45.1)	2557	278	1109	734 (27.5)	1839	138	137	1344 (50.3)	2189	312
c3540	831	1820 (51.4)	3284	505	1137	1303 (36.8)	3034	227	188	2447 (69.1)	3458	1677
c5315	1134	1917 (36.1)	5199	620	1867	1452 (27.3)	4149	405	178	3192 (60.1)	5121	1375
c6288	172	5447 (86.6)	6288	5602	210	3028 (48.2)	6288	825	34	6012 (95.6)	6288	5515
c7552	1037	3186 (42.2)	6946	2046	1743	2564 (34.0)	5398	500	276	6009 (79.6)	7449	1883
Average	498	1566 (49.4)	2908	981	766	1067 (34.9)	2495	242	123	2271 (72.5)	2938	1253

* Fault efficiency=100%

Table 5 Results in change of wire capacitance.

Sim. No.	Test & Circuit types	Cw1 [fF]	Cw2 [fF]	Vfmax [mV]	tpd [μs]	
S6	Typical gates VDD application	80	8	698.9	6.76	
		80 –> 44	8 –> 44	698.9	9.38	
		80 –> 8	8 –> 80	698.9	12.45	
S7		8	80	127.1	6.72	#
		8 –> 44	80 –> 44	127.1	2.67	
		8 –> 80	80 –> 8	127.1	0.022	
S8	Typical gates VSS application	80	8	-102.0	6.65	#
		80 –> 44	8 –> 44	-102.0	2.54	
		80 –> 8	8 –> 80	-102.0	0.023	
S9		8	80	-675.7	6.65	
		8 –> 44	80 –> 44	-675.7	9.88	
		8 –> 80	80 –> 8	-675.7	11.79	

such a case. For example, the VDD application is better for $(Cw1, Cw2) = (8\,\text{fF}, 80\,\text{fF})$. If $(Cw1, Cw2)$ changes to (80 fF, 8 fF) for applying the test vector, the delay time, tpd, becomes shorter from $6.72\,\mu s$ to $0.022\,\mu s$. In this case, the VSS application is better because the final values of wire capacitances after the test vector application are (80 fF, 8 fF). From the above discussion, two methods of the voltage application, VDD application and VSS application, give good results even if the wire capacitances around the fault location change.

5. Conclusion

We proposed ramp voltage testing to detect interconnect open faults. It can detect the open faults as a logic error (or a signal delay) and requires only one test vector. This paper showed that the proposed method could apply to every fault location and to open faults with any value. Since the behavior of the faulty circuit can be modeled by the RC differential circuit if we use the proposed method, we can estimate electrical behaviors by using a local circuitry around a fault location. Finally, we showed test generation results that are suitable for the proposed method and are achieved by the ATPG algorithm similar with stuck-at faults. The proposed method may be costly since it requires ramp voltage application. However, we consider that application to specific locations, for instance, where we surely guarantee fault-free function, is possible and realistic. Besides, the proposed method can be used for fault analysis and fault diagnosis that are inherently costly. In order to show practicality, we further apply the proposed method to a real chip and examine it for other open fault models.

References

[1] R. Rodríuez-Montañés, P. Volf, and J. Pineda de Gyvez, "Resistance characterization for weak open defects," IEEE Des. Test Comput., vol.19, no.5, pp.18–26, 2002.

[2] J. Segura, A. Keshavarzi, J. Soden, and C. Hawkins, "Parametric failures in CMOS ICs – A defect-based analysis," Proc. Int. Test Conf., pp.90–99, 2002.

[3] R.L. Wadsac, "Fault modeling and logic simulation of CMOS and MOS integrated circuits," Bell Syst. Tech. J., vol.57, no.5, pp.1449–1474, May-June 1978.

[4] W. Moore, G. Gronthoud, K. Baker, and M. Lousberg, "Delay-fault testing and defects in deep sub-micron ICs – Does critical resistance really mean anything?," Proc. Int. Test Conf., pp.95–104, 2000.

[5] M. Renovell, A. Ivanov, Y. Bertrand, F. Azais, and S. Rafiq, "Optimal conditions for Boolean and current detection of floating gate faults," Proc. Int. Test Conf., pp.477–486, 1999

[6] V.H. Champac and A. Zenteno, "Detectability conditions for interconnection open defect," Proc. VLSI Test Symp., pp.305–311, 2000.

[7] B. Kruseman, "Comparison of defect detection capabilities of current-based and voltage-based test methods," Proc. European Test Workshop, pp.175–180, 2000.

[8] J.C.-M. Li, C.-W. Tseng, and E.J. McCluskey, "Testing for resistive opens and stuck opens," Proc. Int. Test Conf., pp.1049–1058, 2001.

[9] C.-W. Tseng and E.J. McCluskey, "Multiple-output propagation transition fault test," Proc. Int. Test Conf., pp.358–366, 2001.

[10] S. Ghosh and F.J. Ferguson, "Estimating detection probability of interconnect opens using stuck-at tests," Proc. Great Lakes Symp. VLSI, pp.254–259, 2004.

[11] Y. Miura, "A simple logic testing for interconnect opens in CMOS combinational circuits," European Test Symp., 2004.

[12] J.P. de Gyvez, G. Gronthoud, and R. Amine, "VDD ramp testing for RF circuits," Proc. Int. Test Conf., pp.651–658, 2003.

[13] J.M. Rabaey, Digital Integrated Circuits: A Design Perspective, Prentice-Hall, NJ, 1996.

[14] Z. Li, X. Lu, W. Qiu, W. Shi, and D.M.H. Walker, "A circuit level fault model for resistive opens and bridges," Proc. VLSI Test Symp., pp.379–384, 2003.

[15] Y. Miura, "Open fault detection in CMOS combinational circuits by logic testing with precharge," Information Technology Letters, Forum on Information Technology, LC-005, pp.39–42, 2004.

[16] W.H. Hayt, Jr. and J.E. Kemmerly, Engineering Circuit Analysis, Fifth ed., McGraw-Hill, NY, 1993.

[17] The MOSIS Service, http://www.mosis.org/

[18] K. Miyase and S. Kajihara, "XID: Don't care identification of test patterns for combinational circuits," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol.23, no.2, pp.321–326, Feb. 2004.

Yukiya Miura received the B.E. and M.E. degrees from Akita University, Akita, Japan, in 1985 and 1987 respectively, and the Ph.D. degree from Osaka University, Osaka, Japan, in 1992. From 1987 to 1989 he joined NEC Corporation where he had been engaged in the development of CMOS LSIs. In 1992 he jointed Tokyo Metropolitan University where he is currently an Associate Professor in the Faculty of System Design. In 1998 he was a Visiting Associate Professor of Universitat Politècnica de Catalunya, Spain. His current research interests are design for testability, current testing, analog and mixed signal circuits testing and defect-oriented testing.