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Study on Test Data Reduction Combining Illinois Scan and Bit Flipping

Masayuki ARAI[†a)], Satoshi FUKUMOTO[†], *and* Kazuhiko IWASAKI[†], *Members*

SUMMARY In this paper, we propose a scheme for test data reduction which uses broadcaster along with bit-flipping circuit. The proposed scheme can reduce test data without degrading the fault coverage of ATPG, and without requiring or modifying the arrangement of CUT. We theoretically analyze the test data size by the proposed scheme. The numerical examples obtained by the analysis and experimental results show that our scheme can effectively reduce test data if the care-bit rate is not so much low according to the number of scan chains. We also discuss the hybrid scheme of random-pattern-based flipping and single-input-based flipping.

key words: *test data reduction, Illinois scan, bit flipping, BIST-aided scan test*

1. Introduction

With the rapid advances in semiconductor technology, scales of VLSI chips are increasing dramatically. This makes test design more difficult, leading to requirements of larger test data and testing time [1]. Various designs for testability (DFT) techniques have been proposed and evaluated to overcome this problem. Among them, scan-based test has been proposed, which applies automatic test pattern generator (ATPG) test patterns. ATPG test patterns are derived algorithmically, and they can detect faults effectively. One of the drawbacks is the requirement of enormous test data for large circuits, resulting in increase of test cost.

As traditional built-in self-test (BIST) techniques [2] have difficulty achieving a high fault coverage of ATPG, many hybrid BIST schemes have been proposed [3]–[6]. Circuits with hybrid BIST architectures use broadcasters or bit flipping circuits to compress ATPG vectors by taking advantage of their characteristics of having much less care-bits.

The Illinois Scan Architecture proposed by Hamzaoglu et. al. [7] is simple but effective approach to reduce test data by using broadcasters. The Illinois scan operates in two modes: *serial scan mode* where the scan chain is arranged as long single one, and *broadcast mode* which broadcasts data input from single scan-in into divided shorter scan chains in parallel. As the scan cells on the same depth receive the same data in the broadcast mode, the Illinois Scan has the constraints on the fault coverage. Thus, many schemes have been studied, including rearrangement of scan cells [7], suitable test generation algorithm [8], and use of multiple scan inputs [9].

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[†]The authors are with the Faculty of System Design, Tokyo Metropolitan University, Hino-shi, 191–0065 Japan.

a) E-mail: arai@eei.metro-u.ac.jp

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On the other hand, from the bit flipping circuits point of view, early techniques which appeared as deterministic BIST implanted the information of flipping in CUT in the form of combinational logic so-called Bit Flipping Function [5], [6]. As the number of ATPG vectors applied increased, bit-flipping circuits have become to be used under the control of ATE. In BIST-Aided Scan Test (BAST) proposed by Hiraide et. al. [10], pseudo-random patten is generated by the additional built-in circuit, and the appropriate bits of the pattern are flipped not to conflict to the care bits of an assigned ATPG vector. The BAST architecture can compress test data 100 times of ATPG when the care-bit rate is very low. The care-bit rate, however, varies depending on the position of ATPG because of compaction during ATPG generation, and a fraction of ATPGs sometimes much higher care-bit rates than the others. Also, even under low care-bit rate, increasing the number of scan chains would gain the probability that at least one care bit exists on a given clock cycle, reducing the effectivenes of random-pattern-based flipping.

In this paper, we propose a scheme for test data reduction which uses Illinois-scan-like broadcaster along with bit-flipping circuit. Because the bit-flipping circuit is controlled by ATE to flip the broadcasted data on the appropriate scan chain, the proposed scheme can reduce test data without degrading the fault coverage of ATPG. Also, the proposed scheme does not modify the arrangement of CUT or scan chains. We theoretically analyze the test data size for the proposed scheme. The numerical examples obtained by the analysis and experimental results show that our scheme can effectively reduce test data if the care-bit rate is not so much low according to the number of scan chains. We also discuss that the hybrid scheme of random-pattern-based flipping and single-input-based flipping.

2. Combination of Illinois Scan and Bit Flipping

Figure 1 illustrates the basic architecture of the proposed scheme. Let F denote the number of flip-flops (FFs) in the CUT, N denote the number of scan chains, and L denote the maximum length of scan chains. In the proposed scheme, data input from single scan-in bit is propagated in parallel to all scan chains via the inverter block. Controlled by B-bit width of instructions input to the decoder block, the inverter block flips the bit for the given scan chain. Thus, in the proposed scheme, we can input arbitrary ATPG vector to CUT.

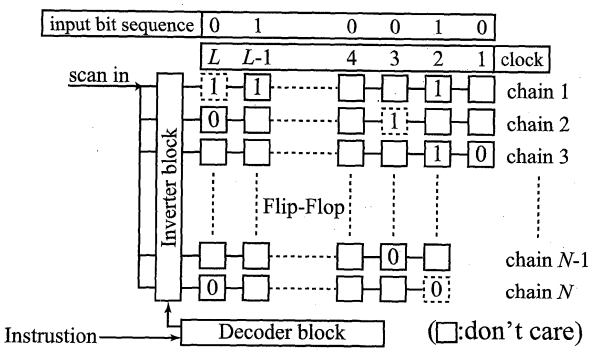


Fig. 1 Basic architecture of the proposed scheme.

ATPG vectors often contain many don't-care bits. We choose the scan-in data for each clock cycle as the majority of the care bits (0 or 1), and the minority of the care bits are flipped by the inverter block. For example, in Fig. 1, the first clock cycle contains only one care bit of 0 on the scan chain 3, and thus data 0 is input and no flips are needed. In the second clock cycle, there are two care bit 1s and one care bit 0. Then, scan-in data is determined as 1, and the scan chain N which has the conflicting care bit needs to be flipped. To the clock with no care bits, the random value is assigned.

Because the number of the flipped bits on each clock cycle may vary in the range of 0 to $N/2$, the decoder block has to control the scan-shift operation. Also, while omitted in Fig. 1, the scan chains might be connected to any response compactors. Therefore, in case of handling the unknown values in the responses, we assume $B = \log_2 N + 2$ in the following.

3. Analysis of Test Data Size

Here we analyze the amount of the test data for an ATPG vector by the proposed scheme, under the assumption that the care bit in the ATPG vector appears independently, according to the care-bit rate r.

The test data size for an ATPG vector by the proposed scheme, $D_{proposed}$, can be estimated as follows.

$$D_{proposed} = L + BL + BEL. \tag{1}$$

The first term L is for the data input from scan-in, and the second one BL is for the instructions of scan-shift. The third one BEL describes the test data for bit-flip, where E denotes the expected number of flipped bits for each clock, and it is derived as

$$E = \sum_{n=1}^{N/2} n \cdot P_n. \tag{2}$$

In Eq. (2), P_n represents the probability that n bits are flipped for a given clock. It is derived as follows.

$$\begin{aligned} P_n &= \binom{N}{n}\left(\frac{r}{2}\right)^n \binom{N-n}{n}\left(\frac{r}{2}\right)^n (1-r)^{N-2n} \\ &\quad + 2\binom{N}{n}\left(\frac{r}{2}\right)^n \binom{N-n}{n+1}\left(\frac{r}{2}\right)^{n+1} \cdot (1-r)^{N-(2n+1)} \\ &\quad \vdots \\ &\quad + 2\binom{N}{n}\left(\frac{r}{2}\right)^n \binom{N-n}{N-n}\left(\frac{r}{2}\right)^{N-n} (1-r)^0 \\ &= 2\left\{\sum_{k=1}^{N-2n+1} \binom{N}{n}\binom{N-n}{n+k-1}\left(\frac{r}{2}\right)^{2n+k-1} \cdot (1-r)^{N-(2n+k-1)}\right\} \\ &\quad - \binom{N}{n}\binom{N-n}{n}\left(\frac{r}{2}\right)^{2n}(1-r)^{N-2n}. \end{aligned} \tag{3}$$

The probability that there is at least one bit flipped, P_{flip} is derived as

$$P_{flip} = 1 - P_0^L. \tag{4}$$

For the original Illinois Scan architecture, broadcast cannot be applied for the ATPG vectors which contains conflicting care bits on one clock.

4. Experimental Results

We applied the proposed scheme to four circuits to evaluate the test data size. Table 1 shows the information about the circuits evaluated. The first two circuits, b17 and b19 are taken from ITC'99 benchmark circuits. The other two circuits, pat1 and pat2, are larger real VLSI chips. The circuits pat1 and pat2 have much less care bits. According to the constraints on the number of FFs, we set the number of scan chains up to 128 for b17 and b19, and up to 1024 for pat1 and pat2.

Figures 2, 3, 4, and 5 plot the results of analysis of test data size for one ATPG vector for b17, b19, pat1, pat2, respectively. The number of scan chain, N, is set to 32, 64, and 128. The X-axis is the care-bit rate r, and the Y-axis is the test data volume in bits which is calculated by Eq. (1) under given N and the number of FFs, F. As shown in the figures, the test data size exponentially increases as the care-bit rate increases. When the care-bit rate is low, increasing the number of scan chains reduce the test data size.

The figures also plot the relation of data size and care-bit rate, which are calculated based on simulations on the actual ATPG. For example, as shown in Fig. 2, the care-bit rate of each ATPG vector distributes in range of 0.08 to 0.22 for b17. For b17, the actual ATPG shows less data size than those obtained by analysis. This is because b17 has much more care bits and the care bits shows stronger correlations. For the other circuits, the results of analysis seem to fit to the simulation results.

For all conditions on the number of the scan chains and care-bit rates shown in the figures, P_{flip} is larger than 0.5, that is, it is not practical to apply Illinois scan with broadcast mode.

Figure 6 shows the result of analysis of test data size for each ATPG vector by the proposed scheme and BAST, fot $F = 52274$, which is equal to the setting of pat2, with up to 1024 scan chains. The BAST architecture uses pseudo-random pattern instead of single scan-in. Therefore, from the test stimuli point of view, the data input from ATE is

Table 1 Information about CUT and ATPGs used for evaluation.

CUT	#FF	#ATPG	avg. care-bit rate
b17	1414	722	13.20%
b19	6543	924	9.04%
pat1	21281	2755	0.35%
pat2	52274	6811	0.23%

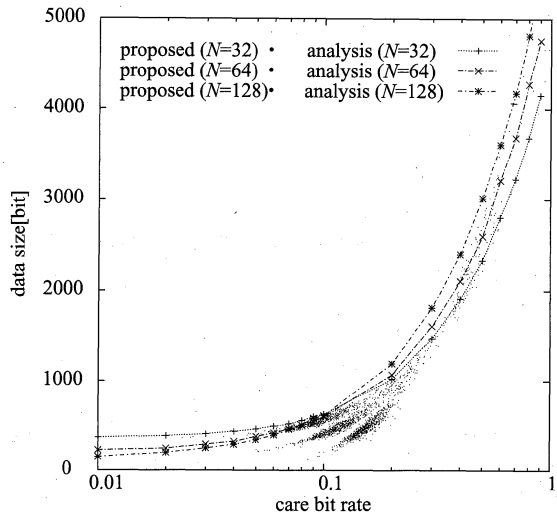


Fig. 2 Test data size for each ATPG vector by the proposed scheme for b17. (N = 32, 64, 128)

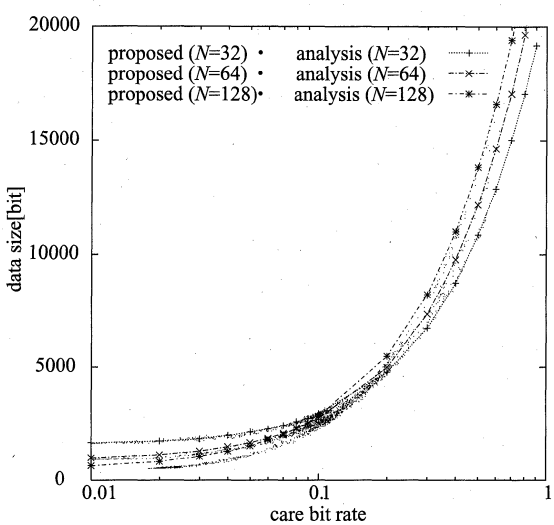


Fig. 3 Test data size for each ATPG vector by the proposed scheme for b19. (N = 32, 64, 128)

only the instructions for flipping and scan-shift, and thus the data size for one ATPG by BAST can be estimated as

$$D_{BAST} = BL + \frac{Lr}{2}. \quad (5)$$

As shown in Fig. 6 (a), for 32 scan chains, the test data size of the proposed scheme is always larger than those of BAST if the care-bit rate is less than 0.01.

As the number of the scan chains increased, test data sizes for both the proposed scheme and BAST are improved,

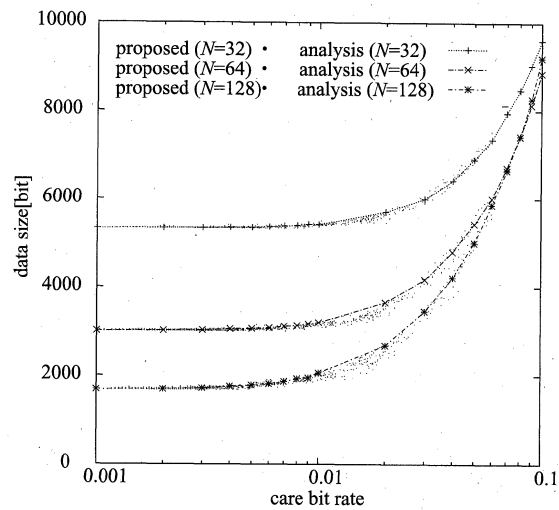


Fig. 4 Test data size for each ATPG vector by the proposed scheme for pat1. (N = 32, 64, 128)

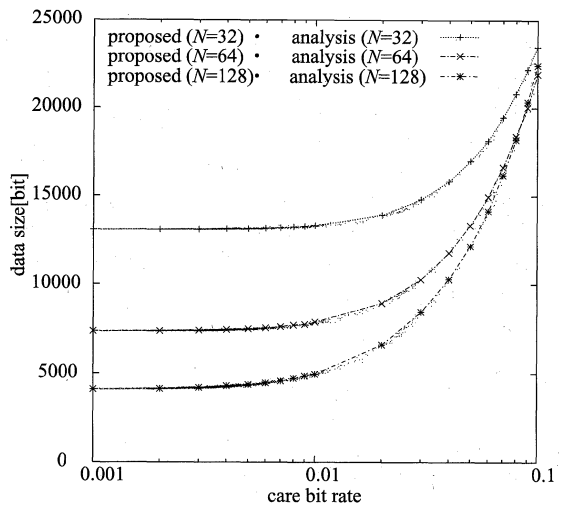
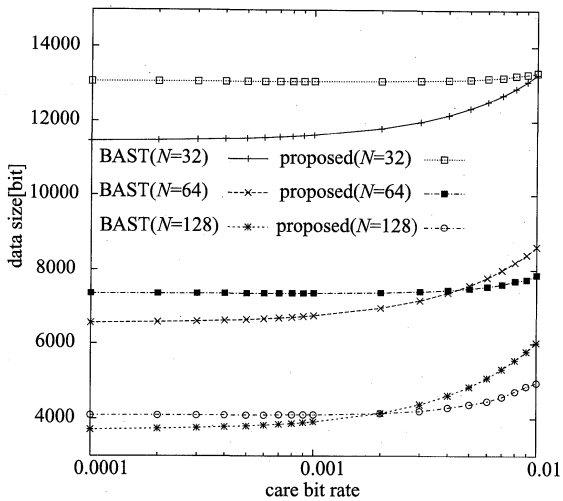


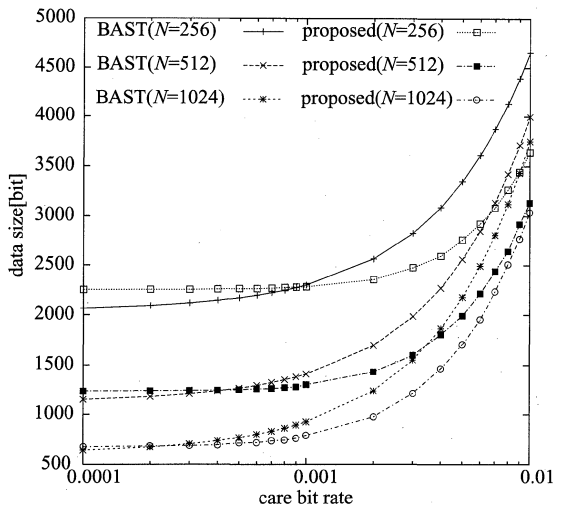
Fig. 5 Test data size for each ATPG vector by the proposed scheme for pat2. (N = 32, 64, 128)

but the difference between them in the low care-bit rate becomes smaller. While the proposed scheme always requires L-bit of scan-in data, scan length L becomes large when the number of the scan chains is small. Furthermore, larger number of the scan chains increases the chances of flips on BAST, even under low care-bit rate. For 1024 scan chains, as shown in Fig. 6 (a), the test data for the proposed scheme is about 5% larger than those of BAST when the care-bit rate is 0.0001, and becomes smaller than BAST when the care-bit rate is larger than 0.0003.

Table 2 summarizes the test data size of the proposed scheme for total set of ATPG vectors. The compression rate is calculated as the relative value to BAST. For b17 and b19, the proposed scheme shows improved test data size for all settings on the numbers of the scan chains. The relative compression rate was 49.31% at the best case for b17. For pat1 and pat2, when the number of scan chains is small,



(a) $F = 52274$, $N = 32, 64, 128$.



(b) $F = 52274$, $N = 256, 512, 1024$.

Fig. 6 Calculation resutls of test data size for one ATPG by the proposed scheme and BAST.

Table 2 Test data size for total ATPG of the proposed scheme. Compression rate is calculated by the relative one to BAST.

CUT	#SC	data size[bit]		compression rate
		BAST	proposal(1)	
b17	32	695850	506845	72.84[%]
	64	751842	467587	62.19[%]
	128	986152	486264	49.31[%]
b19	32	3204110	2685500	83.81[%]
	64	2847220	2228150	78.26[%]
	128	3223710	2348320	72.85[%]
pat1	32	13541100	14792200	109.2[%]
	64	8146940	8437770	103.6[%]
	128	5042940	4906540	97.30[%]
	256	3313070	2957780	89.28[%]
	512	2384760	1944260	81.53[%]
	1024	1914500	1468840	76.72[%]
pat2	32	80756100	89449700	110.8[%]
	64	47787900	50752300	106.2[%]
	128	28727500	28904000	100.6[%]
	256	18011700	16903500	93.85[%]
	512	12163600	10578800	86.97[%]
	1024	9097080	7503030	82.48[%]

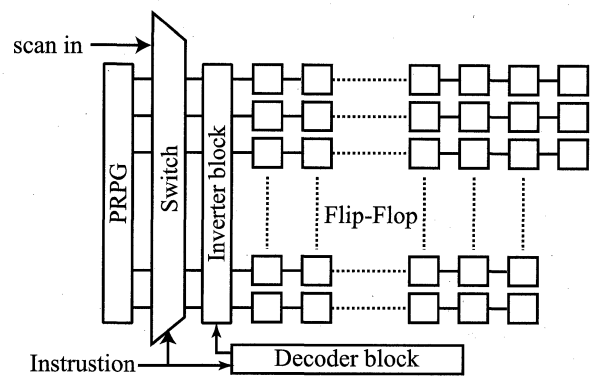


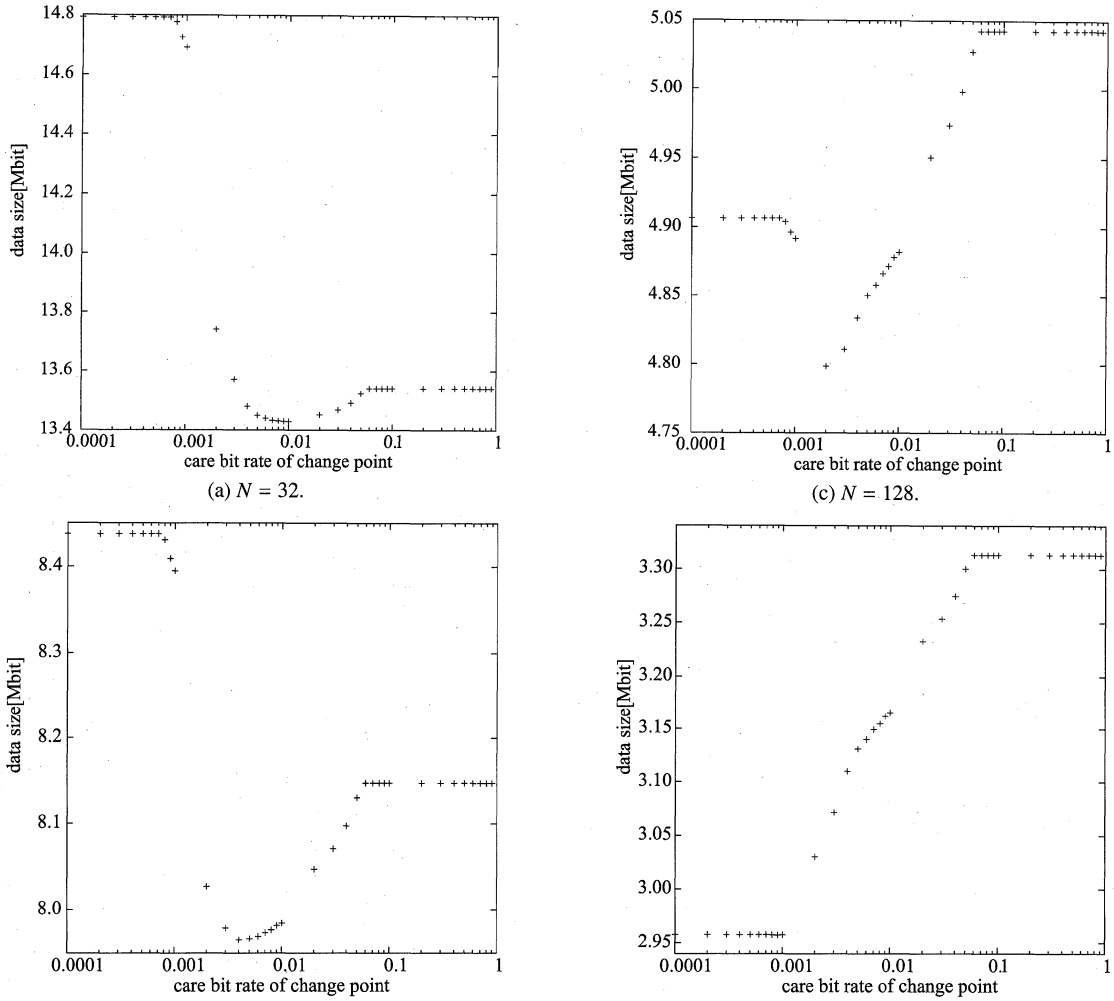
Fig. 7 The hybrid scheme which can flip data from single scan-in or random pattern.

the proposed scheme needs larger amount of test data. It, however, shows more improved test data size as the number of the scan chains become larger. For pat2 with 1024 scan chains, test data size is compressed to 82.48% of BAST.

As shown in Fig. 6, there are the threshold on the care-bit rate of ATPG vectors. For higher range of the care-bit rate than the threshhold, the proposed scheme that is single-scan-in-based flipping shows superior test data compression, and contrary, lower range of the care-bit rate presents the superiority of random-pattern-based flipping. Let us then finally discuss the effectiveness of the hybrid scheme of these two concepts. Figure 7 shows an example of the arrangement of the hybrid scheme. In addition to single scan-in shown in Fig. 1, the hybrid scheme supplies pseudo-random pattern generator (PRPG), as well as the switch choosing the input, which is controlled by the decoder block. Here we simply assume that the hybrid scheme has two modes: single scan-in mode and random-pattern mode. The ATPG vectors with more care bits are first applied by single scan-in mode. After that, a special instruction code is input to the decoder block and the circuit starts to operate in random-pattern mode. In this case, we can implement the instruction for mode transmition without increasing the bit width of the instruction codes.

Figure 8 shows the total test data size by the hybrid scheme for pat1. The X-axis is the change point of the care-bit rate to determine the operation mode. That is, ATPG vectors which have higher care-bit rates than change point are applied by single-scan-in mode, and the others are applied by random-pattern mode. If the change point is higher than the maximum care-bit rate of the ATPG vectors, all of the vectors are applied by random-pattern mode, as indicated as the flat lines on the right side of the figures. Contrary, too low change point forces all ATPG vectors to be applied by single-scan-in mode, shown as the flat lines on the left side of the figures.

When the number of the scan chains is 32, 64, and 128, the optimal change point that minimizes the test data size exists in the range of 0.001 to 0.1. When the number of the



(a) $N = 32$. (c) $N = 128$.

(b) $N = 64$. (d) $N = 256$.

Fig. 8 Total test data size by the hybrid scheme for pat1. In the hybrid scheme, ATPG vectors which have higher care-bit rates than change point (X-axis) are applied by single-scan-in mode, and the others are applied by random-pattern mode.

scan chains is larger than 256, the minimum test data size is observed on the left sides of the figure, that is, obtained by the use of single-scan-in mode, because of the high probability that at least one care-bit exists on each clock cycle.

While we have investigated on the single-scan-in arrangement, our scheme can easily be extended to multiple-scan-in. The effectiveness would depend on care-bit rate.

5. Conclusions

In this paper, we proposed a scheme for test data reduction which uses broadcaster along with bit-flipping circuit. We theoretically analyzed the test data by the proposed scheme. The numerical examples obtained by the analysis and experimental results showed that our scheme can effectively reduce test data if the care-bit rate is not so much low according to the number of scan chains. We also discussed the hybrid scheme of random-pattern-based flipping and single-input-based flipping.

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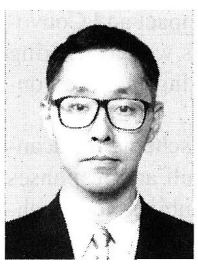
Masayuki Arai received B. E., M. E. and Ph.D. degrees from Tokyo Metropolitan University in 1999, 2001, and 2005, respectively. He is currently an assistant professor in Faculty of System Design, Tokyo Metropolitan University. His research interests include dependable networks and VLSI testing. He is a member of IEEE.



Satoshi Fukumoto received the B. S. E., M. S. and Ph.D. degrees from Hiroshima University, Japan, in 1987, 1989 and 1992, respectively. From 1992 to 2000 he worked at the Department of Information Network Engineering, Aichi Institute of Technology, Japan. Since 2000 he has been working at Tokyo Metropolitan University, where he is now an associate professor of Faculty of System Design. His research areas include fault-tolerant computing, dependable networks, distributed systems and VLSI testing. He is a member of the Information Processing Society of Japan, IEEE, and ACM.

Kazuhiko Iwasaki received B. E. degree in 1977, M. E. degree in 1979, and Ph. D. degree in 1988, all in information and computer sciences from Osaka University. He joined Hitachi's Central Research Laboratory in 1979, where he was engaged in the research and development of VLSI processors. From 1990 to 1995 he was an associate professor at Chiba University. Presently, he is a professor of Tokyo Metropolitan University. His research interests include dependable networking and VLSI testing. He is a senior member of the IEEE, and a member of the ACM and the IPSJ.