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Fabrication of Microchannel with Thin Cover Layer for an Optical Waveguide MEMS Switch Based on Microfluidics

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SUMMARY We propose and demonstrate a new fabrication process of a microchannel using the Damascene process. This process aims to integrate photonic circuits with microchannels fabricated in a glass film. The microchannel is fabricated by the removal of the sacrificial layer after a sacrificial layer is formed by the Damascene process and the cover is formed by sputter deposition. A thin cover layer can be formed by the sacrificial method, because the cover layer is supported by the sacrificial layer during film formation. The cover layer is hermetically sealed, since it is formed by radio frequency (RF) sputtering deposition. The thickness is 1 μm and the width ranges from 3.5 to 8 μm. Using the proposed microchannel fabrication method, we prepared a microelectromechanical system (MEMS) optical switch using microfluidics, and we confirmed its functional operation. This optical switch actuates a minute droplet of liquid injected into the microchannel using Maxwell's stresses. Light propagates straight through the waveguide so that the light passes through the microchannel when the droplet is in the microchannel, but the light rays are completely reflected into a crossed waveguide when the droplet is not in the microchannel. Since this fabrication method uses techniques common to those in the formation of copper wiring in an IC chip, it can be used in the microchannel process.
key words: *optical switch, microelectromechanical system, microchannel, Damascene process, thin cover layer*

1. Introduction

Microchannels are promising as a building block for many applications such as micro total analysis systems (μ-TAS), microreactive chambers, low-k materials in an integrated circuit (IC) chip, low-refractive-index materials in an optical integrated circuit, and dead-air space for controlling thermal flow.

We studied the fabrication process for a microchannel orientated toward optical switches, using a silica-based optical waveguide and the movement of a matching oil droplet, which is injected into the microchannel [1]. The characteristics of the microchannel are: 1) the microchannel is formed in silica-based optical waveguides. 2) The sidewall is formed perpendicular to the waveguide, since one of the sidewalls is used as a mirror. 3) The cover layer is thin because we want to minimize the distance between the upper electrode on top of the cover layer and the substrate that is used as the lower electrode. 4) The clearance between the cover layer and the substrate is not apparent. 5) The surface of the cover layer must be flat, because the electrode is formed on the cover layer. If the surface is not flat, the electrode cannot be formed on the cover layer, and the driving voltage cannot be applied to the droplet injected into the microchannel.

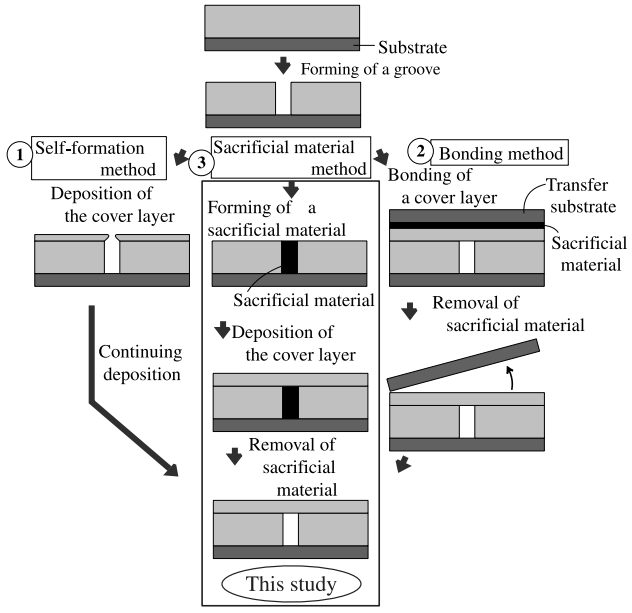

Fig. 1 Generalized fabrication process for microchannel.

In practice, the separation of the fabrication processes of the microchannel and IC or the integrated photonic circuit is important so as to avoid interference with or influence on fabrication conditions. To achieve this separation we considered the following three methods: 1) the self-formation method, 2) the bonding method 3) and the sacrificial-layer method. An outline of these methods is shown in Fig. 1. In the self-formation method, a microchannel is formed by the etching of a groove and the deposition of a cover layer in the horizontal direction. Norlin et al. [2] demonstrated a multisensor system by a self-formation method. In the bonding method, a groove is also formed by etching, and the other planar substrate is bonded to it. A sensor array was demonstrated by Schmidt et al. using an SOI wafer [3]. A micromachined micropump was demonstrated by Harrison and Bao [4]. In the sacrificial-layer method, a groove is first formed by etching and is buried by a sacrificial layer. Next, a microchannel is formed by the removal of the sacrificial layer. Phosphosilicate glass is usually used as the sacrificial layer. Kohl et al. demonstrated an air channel using a sacrificial photosensitive polycarbonate [5].

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When using the self-formation method, the width of the trench is limited. This is because the cover layer material is deposited not only on the cover layer, but also on the sidewalls of the trench. To realize a wide microchannel, a narrow trench is first formed, and the sidewall is etched selectively to increase the width of the trench. In this process, the perpendicularity of the sidewall usually deteriorates. In the bonding method, a perfectly smooth, clean surface is required. The condition of the surface, and the temperature and pressure of the bonding environment are very important [6]. When substrates that have an imperfect surface are bonded, a clearance gap is formed between the substrates. Compared with other methods, the sacrificial-layer method is well suited to the fabrication of an occlusive microchannel.

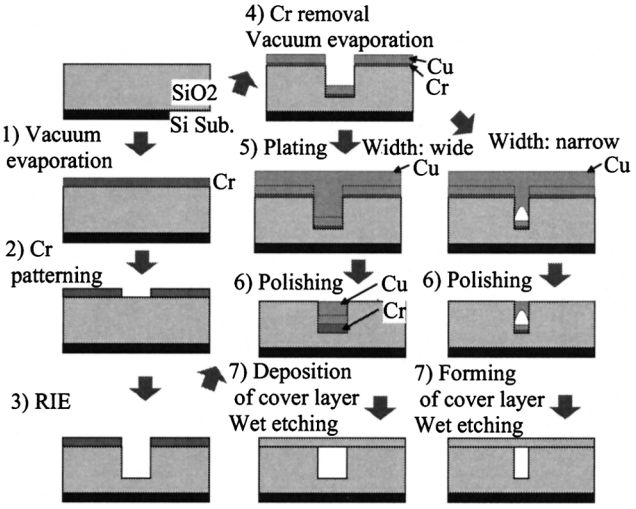
Copper is the most common material used in the plating technique and is promising for the interconnection to the IC chip owing to its high electrical conductivity. The dual Damascene process, which is a modified Damascene process, is a well-known technique used to create copper wiring [7].

The bonding method is often used to form a microchannel in a glass substrate [8], [9]. However, the sacrificial-layer method has advantages regarding the desired characteristics described in Sect. 1. Hence, we developed the fabrication technology of a microchannel using the Damascene process, which is suitable for integration with optical integrated circuits. This fabrication technology is suitable for the monolithic integration of microfluidic circuits and photonic circuits because of its large fabrication tolerance of the copper layer and the thin cover layer.

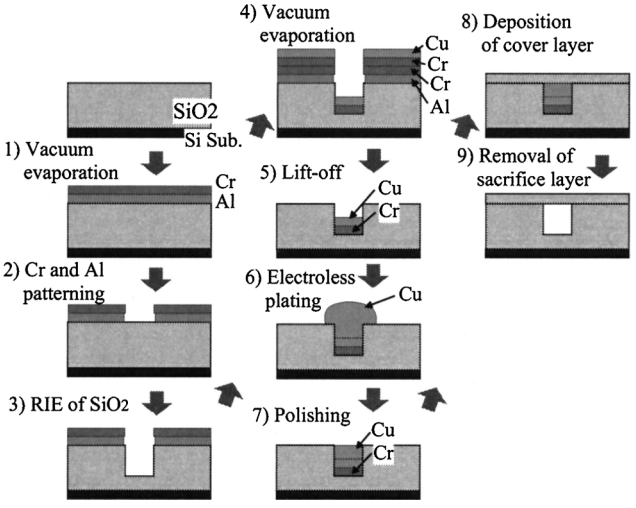
2. Fabrication Process

Figure 2 shows the fabrication process for the microchannel developed in this study. Figure 2(a) shows the fabrication process for the microchannel using the conventional Damascene process. 1) Chromium, as the mask for reactive ion etching (RIE), is deposited. 2) The chromium mask is patterned by photolithography. 3) A trench is formed by RIE. 4) After removal of the chromium, chromium and then copper are deposited. Chromium is used as an adhesive layer between the substrate and the copper layer which is used as the seed layer of plating. 5) A thick copper layer is then formed by electroless plating so that the trench is completely covered. 6) The copper layer formed on the land area is polished, and the sacrificial copper layer formed in the trench is planarized. 7) The cover layer is deposited. Finally, the copper and chromium layers are removed by wet etching.

When the trench width is narrow, and depending on the plating conditions in the trench, voids sometimes appear in the sacrificial layer. The cover layer is deposited on the sacrificial layer. Therefore, the surface profile of this cover layer is a copy of that of the sacrificial layer, but somewhat smoother. Even when a void is formed in the sacrificial layer, the succeeding process can be continued, unless large cracks form that cannot be covered up by deposition after smoothing the extra sacrificial layer by polishing.



(a) Without lift-off process.



(b) With lift-off process.

Fig. 2 Fabrication process.

Figure 2(b) shows the improved fabrication process of the microchannel developed in this study. Using the lift-off technique and the Damascene process, we can form the sacrificial layer selectively in the trench. Since the sacrificial layer starts forming from the bottom of the trench, voids are less likely to form in the sacrificial layer, even if the trench width is narrow. Therefore, a dense and mechanically strong sacrificial layer can be formed. 1) Aluminum as the lift-off material and chromium as the RIE mask material are deposited in sequence. 2) The chromium mask is patterned by photolithography. 3) A trench is formed by RIE. 4) Chromium and copper are deposited by vacuum evaporation. Chromium is used as an adhesive layer between the substrate and the copper layer, which is used as the seed layer of plating. 5) The plating seed layer remains on only the bottom of the trench because of a lift-off using sodium hydroxide solution. 6) The sacrificial layer is selectively formed by electroless plating. 7) The sacrificial layer is

planarized by polishing the excess sacrificial layer. 8) The cover layer is deposited. 9) The copper and chromium are removed by wet etching.

The number of steps in the processes is increased, because the deposition of aluminum and the lift-off technique is added to the process. This process has three advantages: 1) it produces a dense sacrificial layer, 2) the deposition area is reduced, and 3) the polishing time is shortened.

3. Process Conditions

3.1 Formation of Groove

SiO_2 was deposited on a thermally oxidized 3 inch silicon wafer by RF sputtering to prevent the undesired plating of copper on the reverse side of the substrate. Aluminum and chromium were deposited by vacuum evaporation and patterned by conventional photolithography and wet etching. The silicon dioxide layer was etched by RIE. These techniques are conventional fabrication methods for photonic circuits.

3.2 Electroless Plating

Electroless copper plating was performed in 5 liter of solution with air which is used to agitate the substrate, which suppresses the self-decomposition of the plating bath. The agitation of the substrate peels off the bubble generated during the plating. A summary of the plating conditions is shown in Table 1. EDTA·2NA is complexing agent that is suitable for thick plating. Sodium hydroxide is a pH regulator, formalin is a reducing agent, and 2,2' bipyridyl is a stabilizing agent.

Plating seed (copper) was formed by vacuum deposition. To improve the adhesion between copper and SiO_2, a 100-nm-thick chromium layer was deposited on the SiO_2 layer. Because the adhesion between copper and SiO_2 is poor [6], the plating seed (copper) easily becomes unstuck when no chromium buffer layer is formed between the copper and SiO_2 layers. As the pretreatment for electroless plating, the substrate was cleaned using organic solvents (methanol, acetone, trichloroethylene) and dilute (0.5 mol/l) nitric acid. To plate selectively on only the copper plating seed, no catalyst was added.

3.3 Polishing

Figure 3 shows a photograph of the polishing machine. A substrate adhered to a ceramic plate is rotated on a turntable (40 cm diameter used in this study) with a polishing pad stuck on its center axis.

The polishing can be classified into chemical mechanical polishing (CMP) and mechanical polishing (MP) according to the choice of slurry, whose pH is adjusted for the material. The slurry should be adjusted to acidic for the CMP of copper. If the slurry is adjusted to alkaline, the copper is polished mechanically. In contrast, the slurry should be adjusted to alkaline for the CMP of SiO_2. ICue5003 (supplied by Cabot Inc.) and NANOX#200 (supplied by Nano Factor Co., Ltd) are slurries for the copper and SiO_2, respectively. In this study, we used ICue5003 for the CMP of copper, which was mixed with 1mol/l nitric acid to adjust to pH=4, and NANOX#200 for the MP of copper. Table 2 shows the polishing conditions [10].

3.4 Formation of Cover Layer

After the polishing, the substrate was cleaned with pure water and organic solvents. The cover layer was then deposited by RF sputtering. Table 3 shows the deposition conditions of the cover layer. The thickness of the cover layer was 1 μm.

Table 1 Plating condition.

Copper(II) sulfate pentahydrate	10 [g/l]
EDTA·2NA	30 [g/l]
Sodium hydroxide	8.5 [g/l]
Formalin 37%	10 [ml/l]
2,2' bipyridyl	5 [mg/l]
Bath temperature:65 [deg]	
With air agitation	
Agitation of the substrate:35 rpm	

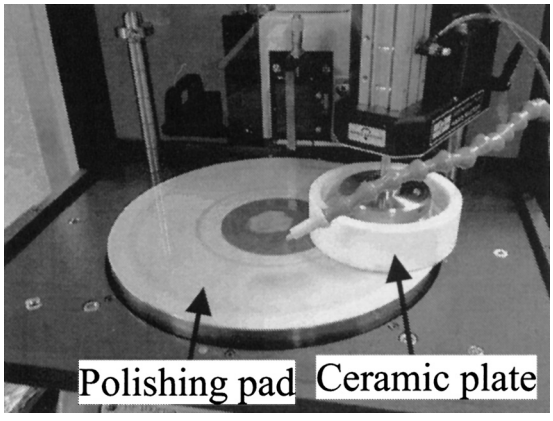


Fig. 3 Polishing machine.

Table 2 Polishing conditions.

	CMP	MP
Slurry	ICue 5003 (Cabot) pH=4 (ADJ by nictric acid)	NANOX #200 (Nano Factor) pH=9.94
	Instillment speed: 3.5 [ml/min]	
Pressure	0.1 [MPa]	
Rotation speed	Table: 30 [rpm]	
	Substrate: 10 [rpm]	

Table 3 Deposition conditions of cover layer.

Material	Silicon dioxide
Target size	4 inch
Gases	Ar:O_2=1.1:1.9 [sccm]
Temperature	300 [°C]
RF power	500 [W]
Deposition rate	0.79 [μm/h]

4. Results and Discussion

4.1 Electroless Plating

Figure 4 shows the change in pH of the electroless plating bath for two cases. One is for the plating on a 3 inch wafer with a full surface area, and the other is for a reduced deposition area obtained by the lift-off technique (Fig. 2(b)). The plating conditions are the same as those shown in Table 1. The decrease in pH was suppressed owing to the reduction in the deposition area.

The plating rate decreases as the pH of the plating bath decreases. This is because the pH is a measure of electric potential, which supplies energy to the electroless plating. Other factors affecting the deposition rate are the plating bath temperature, the agitation speed, the concentration of metal salt, the concentration of reducing agent, and the material and concentration of plating additives. To stabilize the plating rate, these factors must be kept constant. The temperature and the agitation speed were controlled to be constant using the plating apparatus. Other factors seem to be suppressed by reducing the deposition area, as shown in Fig. 2(b), and by suppressing the change in pH as shown in Fig. 4. The thickness of the sacrificial layer can be controlled more precisely by the process shown in Fig. 2(b) than by the process shown in Fig. 2(a).

The deposition on the reverse side of the substrate was negligible, because the substrate was thermally oxidized prior to the plating. Note that the copper was plated not only on the trench, but also on the liquid reserve at both ends of the trench, the marking pattern to align the mask surrounding the device, and the holding assembly in the plating bath. Here, the liquid receiver and the marking pattern are drawn on the same patterning mask as the trenches, and are plated as on the trenches. Note that part of the holding assembly of the substrate is made of metal, so some plating on the holding assembly is inevitable.

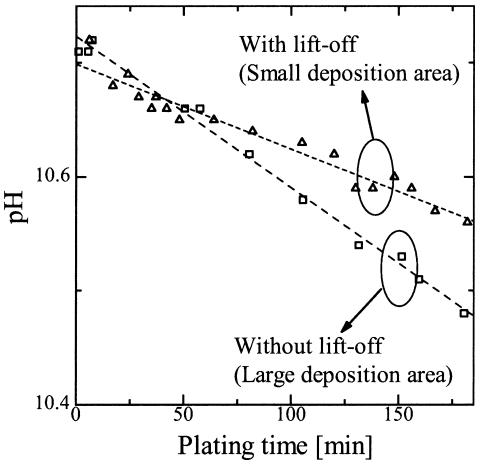


Fig. 4 pH decrease in plating bath.

4.2 Polishing and Fabricated Microchannel

After the sacrificial layer was formed by electroless plating, the sacrificial layer was polished so that the height of the layer was the same as the trench height. The conditions for electroless plating are shown in Table 1, and the polishing conditions for MP and CMP are shown in Table 2.

After cleaning with pure water and organic solvents and the deposition of the cover layer using the conditions shown in Table 3, a microchannel was formed by wet etching the sacrificial layer using a nitric acid and chromium etchant (supplied by Wako Pure Chemical Industries, Ltd.). Perspective SEM images of microchannels fabricated in accordance with the steps in the fabrication process as shown in Figs. 2(a) and 2(b) are shown in the following subsections.

4.2.1 Fabrication Without Lift-Off Process

Figure 5 shows an SEM image after plating, and Fig. 6 shows SEM and AFM images after polishing. Figure 7 shows the final fabricated microchannel.

After the plating, the thickness of copper on the land area was 10 μm and the bump on the surface was negligible. First, to reduce the copper layer on the land area, the copper layer was polished by CMP, whose polishing speed was faster than MP. The copper layer was reduced to less than 0.5 μm and then polished by MP. A previously unseen crack was observed on the center of the surface of the sacrificial layer. In some microchannels, voids sometimes appeared in the sacrificial layer depending on the location and width of the trench. The surface roughness on the sacrificial layer without the lift-off process was much greater than on the surface of the sacrificial layer formed by the lift-off process, which is described in the next subsection.

The void was formed in the sacrificial layer because the inlet of the plating solution was closed before the trench was filled. Filling is from the bottom of the trench. The formation of the previously unseen crack is attributed to the fragile nature of the sacrificial layer around the center, where the plated material bridges both sides of the trench. The roughness of the surface of the sacrificial layer implies that the

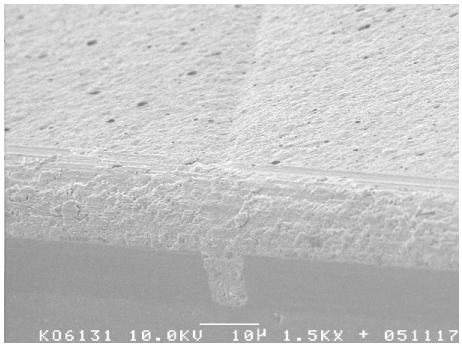
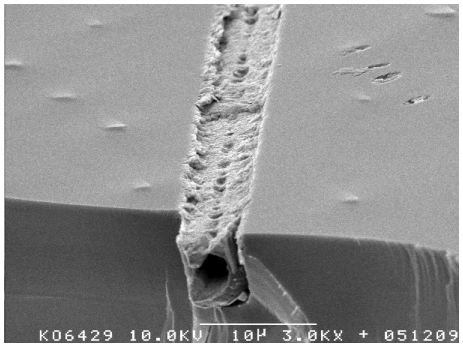
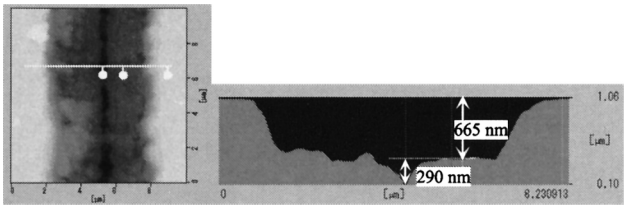


Fig. 5 After plating (without lift-off process).



(a) SEM image.



(b) AFM image.

Fig. 6 After polishing (without lift-off process).

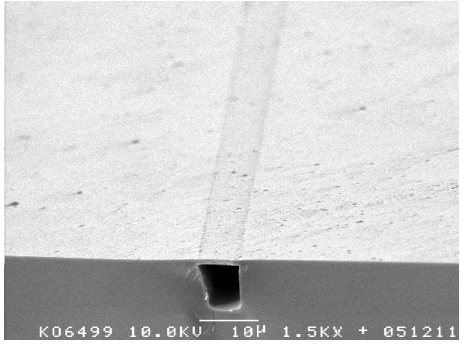


Fig. 7 Fabricated microchannel (without lift-off process).

copper is porous owing to the deterioration of the plating conditions in the trench resulting from a lack of agitation.

As described above, although the sacrificial layer formed by this process has some defects, the fabricated microchannel shown in Fig. 7 is as high quality as those described in the next subsection.

4.2.2 Fabrication with Lift-Off Process

Figure 8 shows an SEM image of the trench after the selective plating process in the trench using the lift-off technique. Next, Figs. 9 and 10 show perspective SEM and AFM images of the trench after CMP polishing only and after MP polishing only, respectively. Note that in Fig. 9 a dent appeared at both ends of the sacrificial layer and that roughness also appeared on the surface. The dent at both sides of the sacrificial layer arises because the sacrificial layer becomes brittle through the chemical effects of CMP, and can be easily etched isotropically.

In contrast to this, note that in Fig. 10, a high-quality

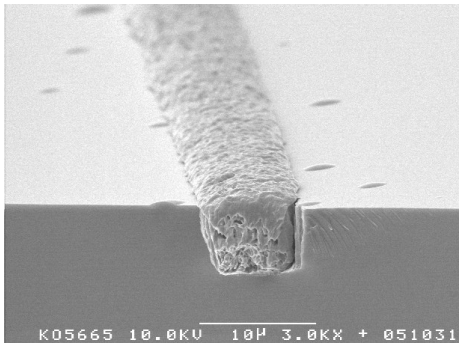
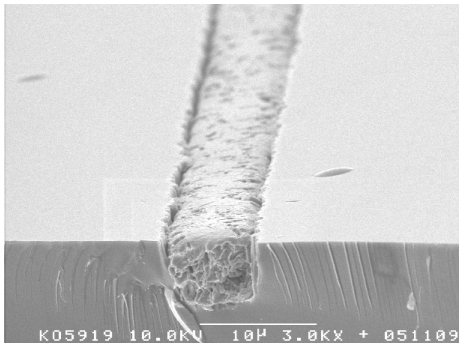
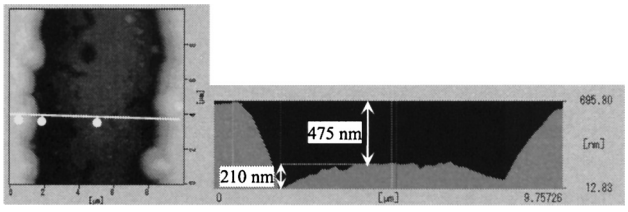


Fig. 8 After plating (using lift-off process).

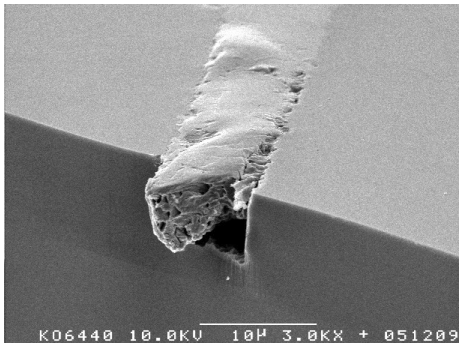


(a) SEM image.

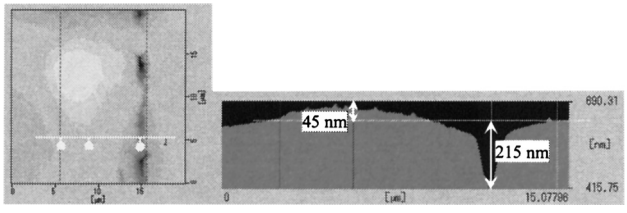


(b) AFM image.

Fig. 9 After polishing (CMP only) (using lift-off process).



(a) SEM image.



(b) AFM image.

Fig. 10 After polishing (MP only) (using lift-off process).

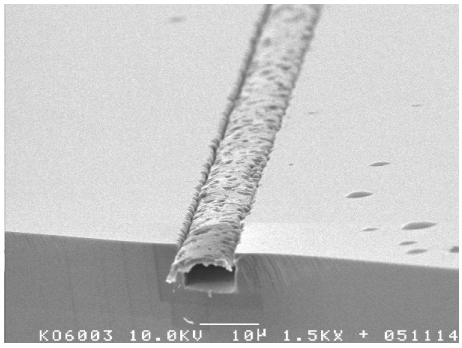


Fig. 11 Fabricated microchannel (polished by CMP only).

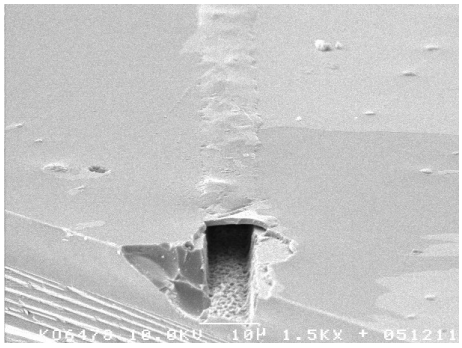


Fig. 12 Fabricated microchannel (polished by MP only).

sacrificial layer with a flat, smooth surface was obtained. Figure 10 also shows that the sacrificial layer is dense, because the surface of the sacrificial layer is smooth.

SEM images of microchannels are shown in Figs. 11 and 12. These are microchannels fabricated by CMP only and MP only, respectively. Figure 11 shows that the dents remained at each end, although they were slightly smoothed. The electrode could not be formed on the sample shown in Fig. 11, because the surface was not flat. On the other hand, Fig. 12 shows that a high-quality microchannel with a flat, smooth top surface was successfully formed. When the sacrificial layer was much thicker than the depth of trench (about 6 μm), similar microchannels were successfully formed by CMP followed by MP. To obtain a smooth surface in a microchannel, the planarization of the sacrificial layer by MP is more suitable than by CMP.

4.2.3 Fabricated Microchannel and Optical Loss

The tilt angle of the sidewall ranged from 0.035 to 0.07 radians. The r.m.s. roughness of the sidewall was 0.25 μm. These parameters cause radiation and scattering losses at the reflection state. The coupling efficiency η_{ang}, which is determined by the tilt of sidewall $\delta\theta$ [rad], is expressed by

$$\eta_{ang} = \exp\left[-\left(4\pi\frac{w_0}{\lambda}\delta\theta\right)^2\right], \tag{1}$$

where w_0 is the spot size in the vertical direction and λ is the wavelength in vacuum. The coupling efficiency η_{scatt}, determined by the scattering due to the r.m.s. roughness σ, is expressed by [11]

$$\eta_{scatt} = \exp\left[-\left(4\pi\frac{\sigma}{\lambda}n_{eq}\sin\theta_{in}\right)^2\right], \tag{2}$$

where n_{eq} is the equivalent index of the waveguide and θ_{in} is the angle of intersection between waveguide and microchannel.

These losses are calculated to be $\alpha_{ang} = -10\log\left(\eta_{ang}\right)$ =0.02–0.1 dB and $\alpha_{scatt} = -10\log\left(\eta_{scatt}\right)$ =20 dB assuming w_0=1 μm, λ=1.55 μm, n_{eq}=1.5 and θ_{in}=$\pi/2$. These parameters of the optical switch are described in Sect. 4.3. The tilt angle and the r.m.s. roughness of the sidewall appear during the fabrication of the trench by RIE. These problems will be reduced by smoothing the mask pattern and the improvement in the RIE condition. For example, the reflection loss can be suppressed to less than 1 dB if the r.m.s. roughness is reduced to less than 55 nm.

4.3 Optical Waveguide Switch Based on Microfluidics

4.3.1 Structure and Switching Principle

Our goal is to realize an optical waveguide switch based on microfluidics that can be operated mechanically. Some optical MEMS switches have been reported [12], [13] that are based on the movement of a bubble driven by the change in surface tension induced by a temperature gradient. However, these switches consume a lot of power. Generally speaking, voltage driving is more effective for low power consumption than current driving. The power consumption W [W] is given by

$$W = IV, \tag{3}$$

where I [A] is the electric current and V [V] is the voltage applied to the device. The driving of this switch is equivalent to the charging of an electric capacitor. Thus, in the steady state, no electric current flows and the power consumption is almost zero, except for the leakage current. When the charge Q [C] is accumulated in the capacitor C [F], the accumulated energy J [J] is expressed by

$$J = \frac{1}{2}QV = \frac{1}{2}CV^2, \tag{4}$$

where V [V] is the driving voltage of the switch. When the dimension of the electrode, including the bonding pad, is assumed to be 1 mm^2, the distance between the electrodes is 10 μm and the relative permittivity of SiO_2 is 3.8, the capacitance of the switch is calculated to be 3.3 pF. The energy required to accumulate the charge in the capacitor is only 1.5×10^{-7} J, assuming that the driving voltage is 300 V. The previously reported bubble-type optical switch [12], which is driven by thermocapillarity, requires a power consumption of 0.15 W and the switching time is 6 ms (J=0.15 · 6×10^{-3}=0.9 mJ). The power consumption of our switch is three orders of magnitude less than the previous switch. In

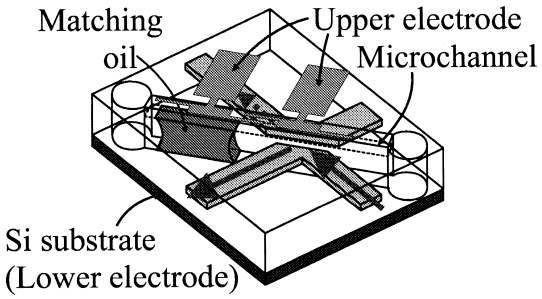


Fig. 13 Perspective view of optical waveguide switch based on microfluidics driven by electrostatic force.

this way, a voltage-driven optical switch is more suitable for low power consumption than the current-driven optical switch.

Figure 13 shows a perspective view of the optical switch. A tube-type microchannel intersects the crossing point of the cross grid busline waveguides. A droplet of index-matching oil (Shin-Etsu Chemical Co., Ltd., KF56, n_D=1.50) is injected into the microchannel. When the matching oil is driven to the crossover site of the waveguide and microchannel, the input light passes straight through the microchannel to the through port. On the other hand, when the matching oil is excluded from the crossover site, the input light is reflected to the cross port owing to the total internal reflection. Matching oil is driven by an electrostatic force (Maxwell's stress) induced by the upper electrode on the microchannel and lower electrode formed on the Si substrate. Maxwell's stress is induced by an electric field applied parallel to the boundary between different materials, and is directed from a high-dielectric-constant material (matching oil) to a low-dielectric-constant material (air). This pressure P [Pa] is expressed by

$$P = \frac{1}{2}(\varepsilon_1 - \varepsilon_2) E^2, \tag{5}$$

where ε_1 and ε_2 are the dielectric constants of the two materials, and E [V/m] is the electric field. The droplet is latched when the driving force is not applied. This is because a latching force is induced by the roughness of the sidewall of the microchannel. A cross-sectional SEM image of the microchannel and a microscopic top view of the optical switch are shown in Figs. 14 and 15, respectively.

The optical waveguides were fabricated on a 3-inch-diameter Si wafer. The core material was 8%Ta_2O_5-92%SiO_2(n=1.56@1.55 μm), and the cladding material was SiO_2(n=1.45@1.55 μm). These layers were deposited by RF sputtering. The core thickness was designed to be 0.8 μm to satisfy the single-mode condition in the vertical direction. The core width was 10 μm so that the misalignment of the mirror position (sub-micron order) did not significantly increase the insertion loss. For patterning of the waveguides, RIE with a Cr mask and C_2F_6 gas were used. The microchannel was 5 μm high and 8 μm wide. To fabricate the microchannels, the process shown in Fig. 2(b) was used, and MP was used to smooth the sacrificial layer.

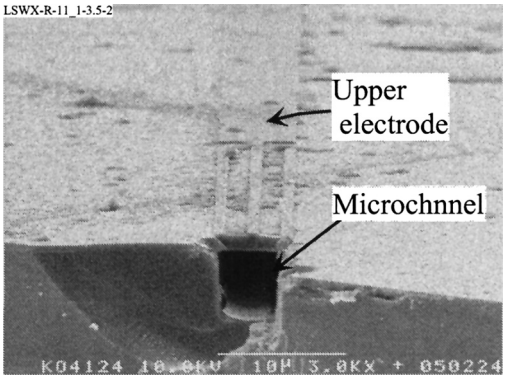


Fig. 14 Cross-sectional SEM image of microchannel and electrode.

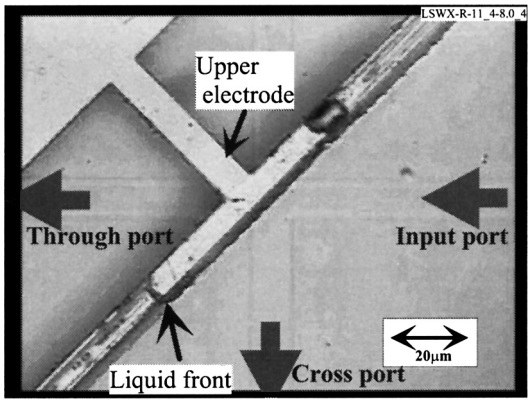


Fig. 15 Microscopic top view of optical switch.

4.3.2 Measurement

When the matching oil lay initially on the crossover site of the waveguide and microchannel, the matching oil was driven out from the crossover site by applying a voltage to the electrodes, and the output power from the cross port was measured against the applied voltage. The measured result is shown in Fig. 16. The liquid droplet was observed to be driven to the outside of the crossover site at 300 V, and the extinction ratio was 23 dB.

The wavelength dependence of the through port response was measured, and the result is shown in Fig. 17. In this measurement, the matching oil lay outside the crossover site (OFF state), and was moved to the crossover site (ON state) by applying a voltage of 350 V. There is no wavelength dependence in the ON state. However, in the OFF state, periodic wavelength dependence was observed. This seems to be caused by the excitation of higher-order modes at the mirror, because the waveguide is larger than the single-mode condition.

The temporal response of the through port from the ON state to the OFF state is shown in Fig. 18. The fall time was 63 ms at the applied voltage of 300 V. A summary of the switching characteristics of this device is shown in Table 4.

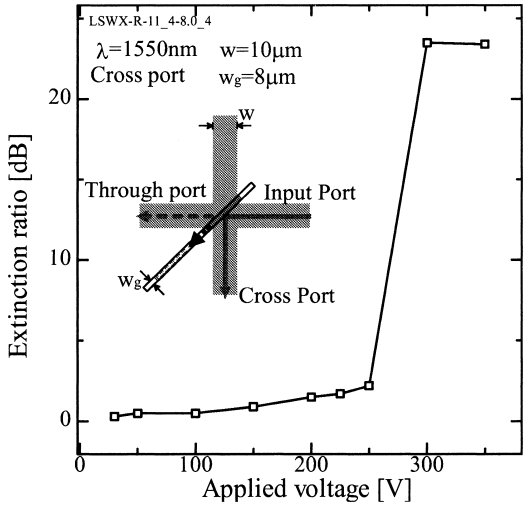


Fig. 16 Measured ON/OFF switching characteristics of cross port response (TM-mode).

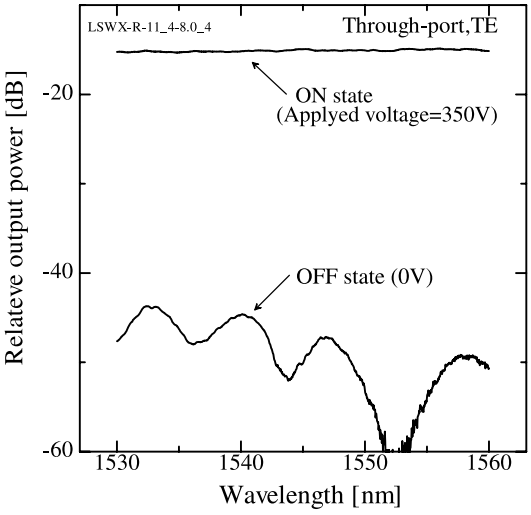


Fig. 17 Wavelength dependence of through-port response (TE-mode).

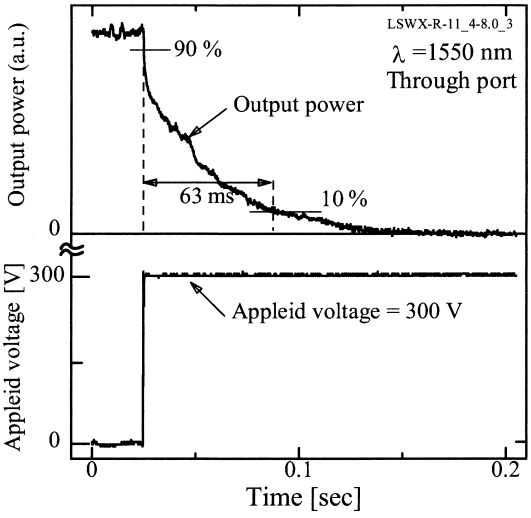


Fig. 18 Temporal response of through port (applied voltage=300 V).

Table 4 Characteristics of optical switch (@1.55 μm).

	Through port	Cross port
Driving voltage	210–350 V	
Insertion loss	15.0 dB	35.4 dB
Extinction ratio	35–39 dB	23 dB
Cross talk	−55 dB	−59 dB
PDL	3.5 dB	0.9 dB

5. Conclusion

In this study, we proposed and developed a fabrication process for a microchannel using a sacrificial layer and the Damascene process. We proposed two fabrication processes: 1) the conventional Damascene process, and 2) the combination of the lift-off technique and the Damascene process. High-quality microchannels can be obtained by either process. In the fabrication process using the lift-off technique for the selective deposition of the sacrificial layer in the trench, a high-quality microchannel is obtained by planarization of the sacrificial layer using MP.

Using process 2), an optical switch using microfluidics was actually fabricated, and the switching operation was demonstrated. The extinction ratio of the optical switch was 35 dB, and the activation voltage was 300 V.

This fabrication process does not require ultimate clean and flat surface, which are required in the bonding method. The thickness of the plated copper layer is not important, provided it is thicker than the depth of the trench, because the copper layer is polished to flatten the sacrificial layer. The cover layer is formed by sputtering deposition so as to cover the sacrificial layer. Thus, a microchannel with a thin cover layer with a large tolerance can be fabricated easily. Possible applications of this fabrication technique are the fabrication of microchannels in a microfluidic chip and the formation of an ultralow-refractive-index region in a photonic integrated circuit.

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