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A Multi-Band Burst-Mode Clock and Data Recovery Circuit

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SUMMARY A multi-band burst-mode clock and data recovery (BMCDR) circuit is presented. The available data rates are 2488.32 Mbps, 1244.16 Mbps, 622.08 Mbps, and 155.52 Mbps, which are specified in a gigabit-capable passive optical network (GPON) [1]. A half-rate and low-jitter gated voltage-controlled oscillator (GVCO) and a phase-controlled frequency divider are used to achieve the multi-band reception. The proposed BMCDR circuit has been fabricated in a 0.18 μm CMOS process. Its active area is 0.41 mm^2 and consumes 70 mW including I/O buffers from a 1.8 V supply.

key words: *multi-band, burst-mode, clock and data recovery, voltage-controlled oscillator*

1. Introduction

Passive optical networks solve the bottleneck among backbone networks and LANs. To connect many optical network units (ONUs) with an optical line termination (OLT), the time division multiple access (TDMA) scheme is adopted. Therefore, the OLT may receive the sequent burst-mode data from ONUs. The clock and data recovery (CDR) circuit at the OLT must detect the input data within tens of bit times and recover the clock and data. Obviously, it is difficult for the conventional CDR circuits to settle within such a short time. To achieve a short acquisition time, the gated voltage-controlled oscillators (GVCOs) [2]–[8] are widely adopted.

Conventional GVCOs are roughly classified into two categories [2]–[8]. One uses the edge detection circuit with a half bit-time delay line to trigger the GVCO [5], [7], [8]. The accuracy of the half bit-time delay line limits the jitter tolerance and bit-error rate. The other combines two GVCOs with a NOR gate [2]–[4] or multiplexer [6] to realize a burst-mode clock and data recovery (BMCDR) circuit. The conventional GVCOs operate within two states: one is the oscillating state and the other is the latching state. It results in the significant inter-symbol interference (ISI) caused by random data patterns for the GVCOs. Moreover, the delay cells in a GVCO are composed of logic gates instead of simple inverters. It will increase the bandwidth requirement of the delay cells. In this work, a half-rate GVCO using only multiplexers is presented. The bandwidth requirement of the delay cells is relaxed and the low ISI is also achieved. To receive the multi-band data, the phase-controlled frequency divider is also presented.

This paper is organized as follows. Section 2 introduces this multi-band BMCDR circuit and its building blocks. The jitter tolerance analysis for the proposed BMCDR circuit is given in Sect. 3. The experimental results are given in Sect. 4 and the conclusions are given in Sect. 5.

2. Circuit Description

The proposed multi-band BMCDR circuit is shown in Fig. 1. It consists of the proposed GVCO, a phase-locked loop (PLL) using a duplicate GVCO, the phase-controlled frequency dividers, a 4-to-1 multiplexer, a double-edge-triggering D flip-flop (DDFF) and the matching circuit. For two GVCOs, one is connected to the input data and the other one is connected to logic ONE. The former is in charge of tracking the phase of the input data while the latter is used as a voltage-controlled oscillator (VCO) in a PLL. This PLL is locked at 1.25 GHz, which is designed for the half-rate data of 2.5 Gbps, with a reference clock of 19.53 MHz and a divide-by-64 divider.

According to different data rates, the external bit-rate selection signal picks one of the four clocks from the 4-to-1 MUX as the recovered clock. Because the recovered clock goes through the phase-controlled frequency dividers and the 4-to-1 multiplexer, a matching circuit is needed to match the delays to get the lowest bit-error rate. The detail circuitries are described as follows.

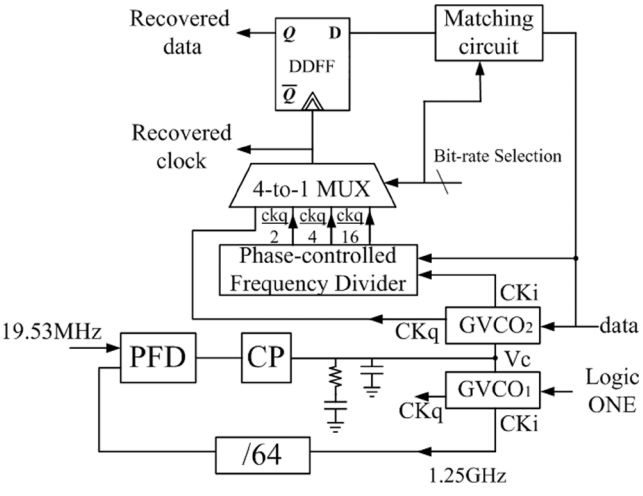

Fig. 1 The proposed burst-mode clock/data recovery circuit.

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2.1 The Proposed GVCO

In general, the proposed GVCO is composed of voltage-controlled multiplexers, M1–M9, and the duty cycle correction (DCC) circuits as shown in Fig. 2. When the input data is high, M1–4 form an oscillator and M6 outputs the clock B, which is the complement of the clock A. On the other hand, when the input data is low, M1–M2 and M5–M6 form an oscillator and M4 outputs the clock A. Once the input data change, the clock A or B tracks the data. Figures 3(a)–(c) illustrate how the proposed GVCO adjusts its output phase when the clock lags, leads, and locks with the data, respectively. As shown in Fig. 3(a), when the clock lags data, the clocks A and B change their polarity before the threshold voltage. It is equivalent to speed up the clock to compensate the lagged phase. Similarly, in Fig. 3(b), when the clock leads data, the clock A and B change after the threshold voltage to correct the phase. When the CDR circuit is locked with the input data, the timing diagram is shown in Fig. 3(c). The transient response for a conventional GVCO with latching problems is also shown in Fig. 3(d). In this figure, a GVCO starts to oscillate when the input data is high and stops to be latched when the input data is low. The serious amplitude variations happen if the output is latched to VDD or GND. Due to the AM/PM conversion, the jitter of the conventional GVCO increases. In the proposed GVCO, the clock A or B is never latched. Thus, the ISI due to the amplitude variations is improved. The simulation results will be given in the following paragraphs (given in Fig. 6).

The delay cell for the proposed GVCO is shown in Fig. 4(a) which is a voltage-controlled multiplexer using

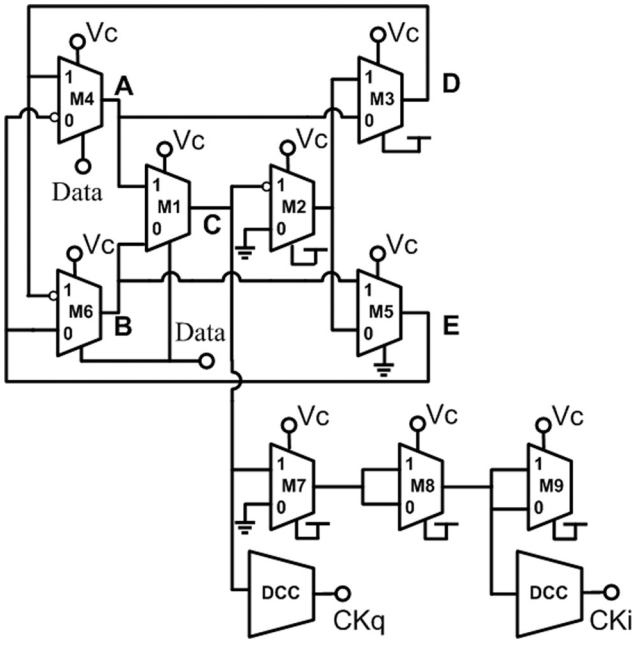


Fig. 2 The proposed GVCO.

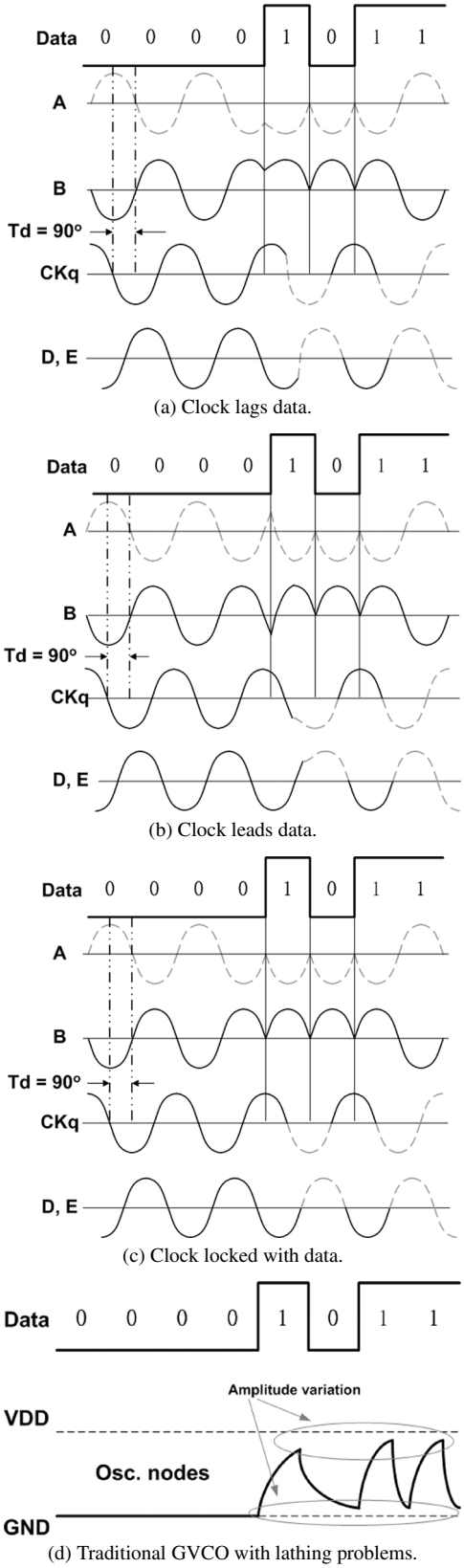


Fig. 3 The timing diagram of the proposed GVCO and the traditional GVCO.

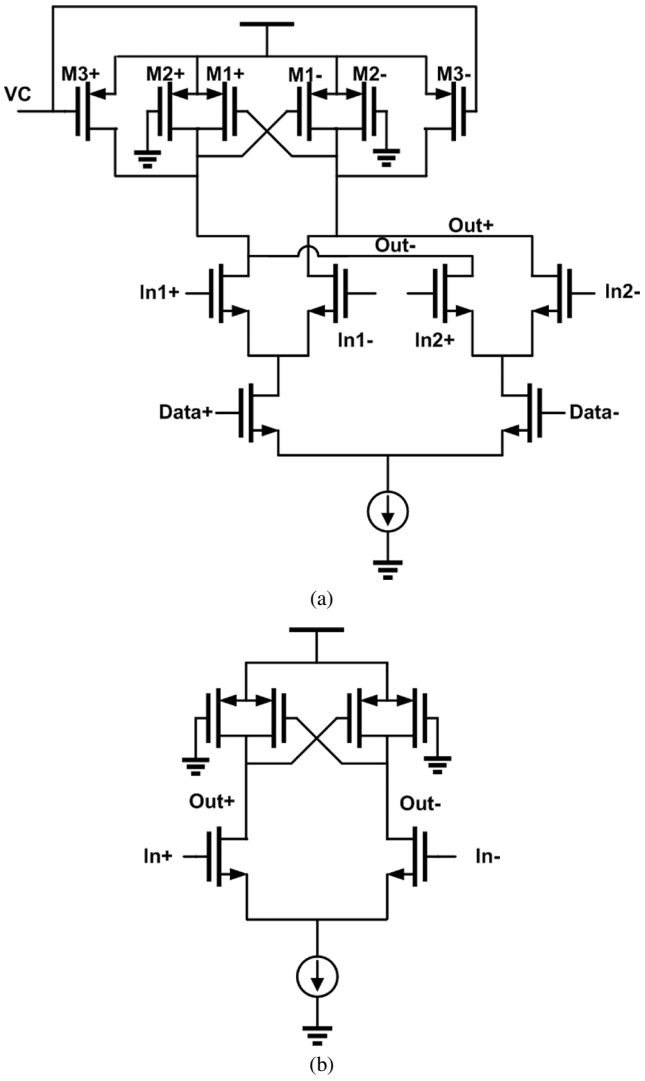


Fig. 4 (a) The delay cell in the proposed GVCO, (b)The duty cycle correction buffer.

the current-mode logics. In Fig. 4(a), M3+/− is used as a voltage-controlled resistor to adjust the delay. The gate of M2+/− is connected to ground to operate as a resistor. M1+ and M1− form a cross-coupled pair to make the transition faster. The data+/− is used to select one of the two inputs, in1+/− and in2+/−. The tail current source is used to reduce the supply noise, since it is current steering. For a conventional GVCO [2], [3], [7], the edge detecting circuit and complex logic circuits, such as NAND or NOR gates, are needed. To realize the mutli-Gb/s GVCO, the current-mode logics (CMLs) are widely used. However, the speed of the CML NAND or CML NOR gates is much slower than that of the CML multiplexer. It is because the parasitic capacitance of the cascade transistors is increased in NAND or NOR CML gates. Since the delay cell in Fig. 4(a) is realized by CML multiplexers, the proposed GVCO will have a wide bandwidth. The DCC circuit, as shown in Fig. 4(b), is also added to ensure the half-rate operation.

Compared with the half-rate GVCO circuit described in [6] which 5 multiplexer-based delay cells and at least 4 delay buffers are used, only 6 multiplexer-based delay cells are required in our proposed GVCO. This means lower power consumption for high data rate transmission. Furthermore, only three multiplexers experience input data switching, but in [6] the input data should drive 5 multiplexer-based delay cells. Hence, our proposed GVCO also relaxes the output loading on the previous stage, such as a burst-mode limiting amplifier.

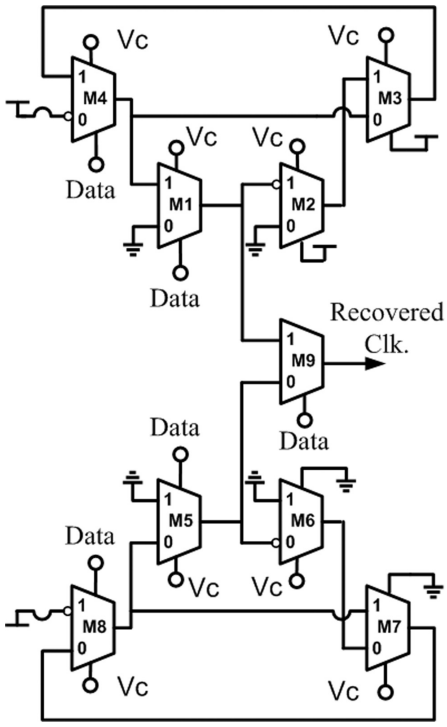
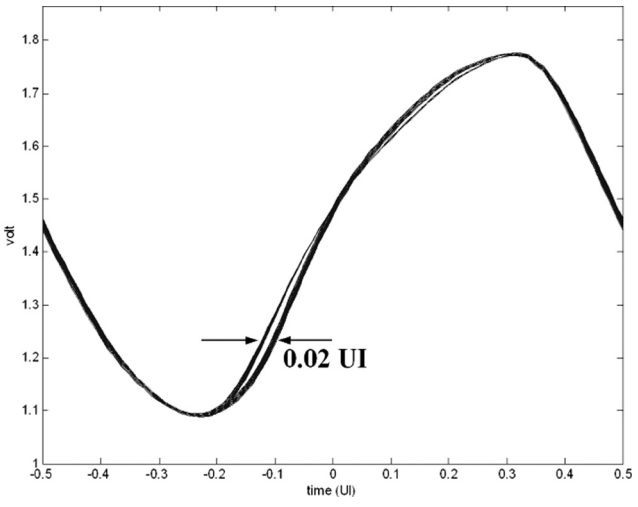
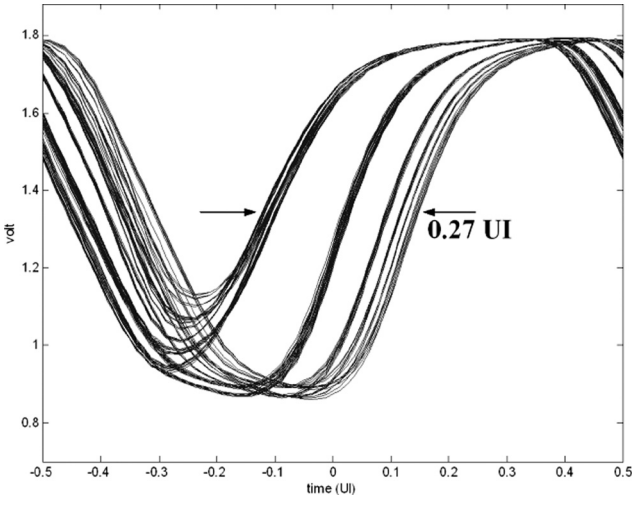


Fig. 5 Conventional GVCO with latching problem.

Since the conventional GVCO may latch or oscillate according to the corresponding data, the data-dependent ISI occurs. A GVCO suffers from the latching problem plotted in Fig. 5 and the proposed one are simulated with a 2.5 Gbps 2^7-1 jitter-free data with 30% transition time. The GVCO in Fig. 5 incorporates two conventional multiplexer-based GVCOs and one multiplexer. When the incoming data is high the upper GVCO composed of the multiplexers M1–4 oscillates and serves output clock. Meanwhile, the lower GVCO composed of the multiplexers M5–8 stops. The condition when incoming data is low can be derived in the same manner. Both GVCOs oscillates at 1.25 GHz by using four delay cells of Fig. 4(a). Figures 6(a) and 6(b) show the simulated transient responses of the recovered clocks for the proposed GVCO and the one with latching problem, respectively. From the simulation results, the proposed GVCO gives an ISI jitter of 0.02 unit interval (UI) and the conventional one gives an ISI jitter of $0.27UI$. Figure 7 shows the simulated jitter for the proposed GVCO and the one with latching problem by changing the number of the delay cells from four to eight. For the proposed GVCO, the extra cells are inserted between the multiplexers, M1 and



(a)



(b)

Fig. 6 Simulated transient response of the recovered clock for (a) the proposed GVCO, (b) GVCO with latch problem.

M2. For the conventional GVCO with latching problem, the extra cells are inserted between the multiplexers, M1 (M5) and M2 (M6). The proposed GVCO maintains a better jitter than the conventional one. Although the number of the delay cells increases, the jitter is decreased for the GVCO in Fig. 5; however, its oscillation frequency is also decreased. We should stress further that in this simulation we construct a conventional GVCO with latching problems by using the same multiplexer delay cell because we try to provide a fair comparison. However, the latching nature makes this kind of oscillator require much more bandwidth to achieve the same performance as the proposed one; even they consist of only multiplexers. Compared to the measurement results in [6], our proposed GVCO indeed provides 80% improvement on the jitter performance under the same data rate and consumes less power.

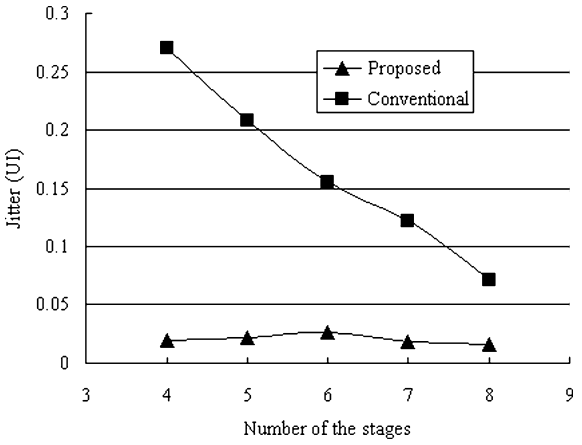


Fig. 7 Simulated jitters for the proposed GVCO and the conventional one using different delay stages.

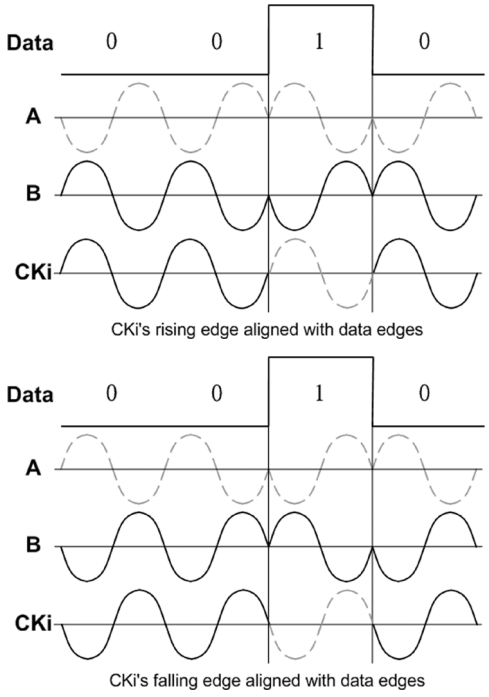


Fig. 8 Two possible conditions for the proposed GVCO under full-rate operation.

2.2 Phase-Controlled Frequency Divider

In the previous section, our GVCO works well for half-rate data at 2.5 Gbps. For a lower data rate, the GVCO's output clock should be divided for the desired bit rate so as to sample the DDFF correctly. Since the GVCO still oscillates at 1.25 GHz, it does not be suited for the data with a lower bit-rate. For example, to consider the 1.25 Gbps data, the proposed GVCO becomes a full-rate one but it still tracks the input data phase. Since any data edge (rising or falling) may correct the phase of the GVCO, two possible steady-state conditions appear in a full-rate operation for our GVCO. As

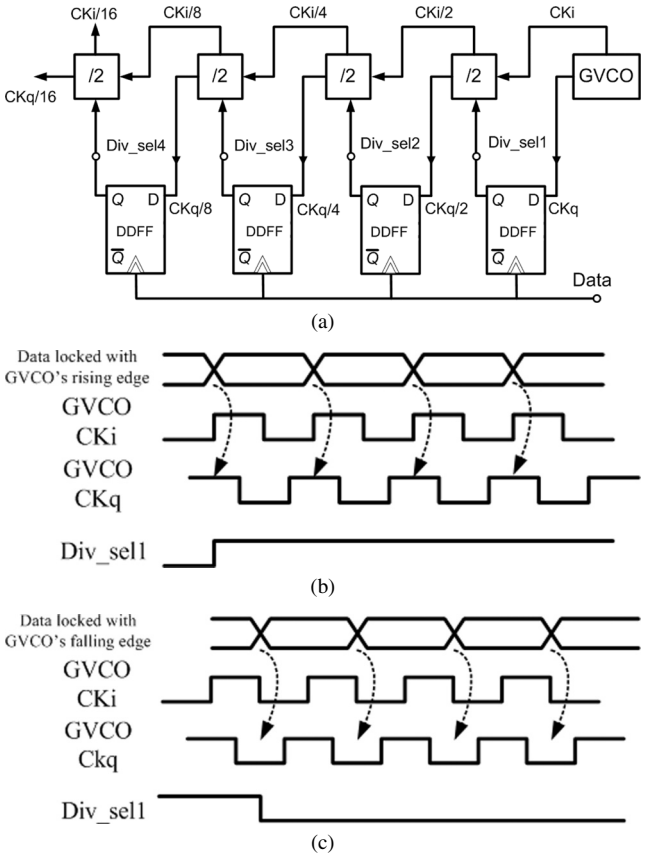


Fig. 9 (a) The phase-controlled frequency divider, (b) Div_sel1 = 1, when data locked with GVCO's rising edge, (c) Div_sel1 = 0, when data locked with GVCO's rising edge.

shown in Fig. 8, the data may align with the rising or falling edge of the GVCO. It causes a problem when the GVCO is divided by two. It is because both the divide-by-2 in-phase and quadrature-phase clocks have the possibility to be the actual sampling one.

To solve this problem, the conventional frequency divider is modified to know which edge (rising or falling) is aligned with the data. The proposed phase-controlled frequency divider is shown in Fig. 9(a). Every divide-by-2 circuit has a DDFF, which the input data samples the preceding quadrature-phase clock and the sampled result serves as the divider selection signal (Div_sel). If the preceding in-phase clock's (CKi) rising edge is aligned with data, the first divider selection signal, Div_sel1, is set to ONE. The timing diagram is shown in Fig. 9(b). Similarly, Fig. 9(c) shows the condition when the preceding in-phase clock's falling edge is aligned with data, and the first divider selection signal, Div_sel1, is set to be "0." The phase-controlled divide-by-2 divider is shown in Fig. 10. It is composed of a multiplexer, which is controlled by the divider selection signal, and two edge-triggering DFFs.

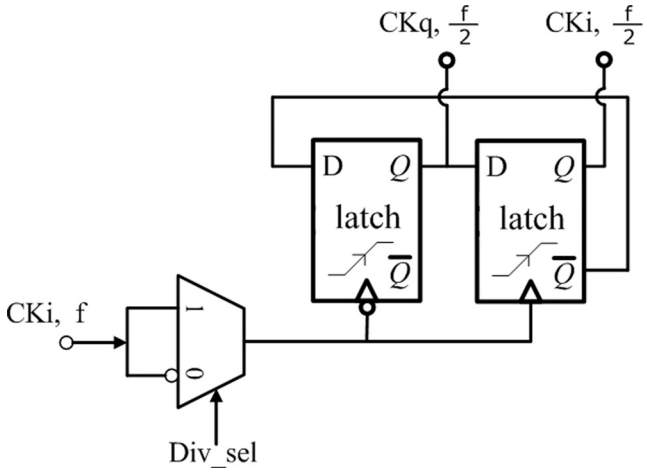


Fig. 10 A phase-controlled divide-by-two divider.

2.3 Double-Edge-Triggering D-Flip Flop (DDFF) and 4-to-1 Multiplexer

The current-mode logic (CML) circuits are widely used for high speed digital circuits. The CML latch and multiplexer are the basic building blocks to realize all the circuits in this work and they are shown in Figs. 11(a) and (b), respectively. The DDFF is shown in Fig. 11(c), which is composed of two CML latches and a multiplexer. The 4-to-1 multiplexer of Fig. 2 is shown in Fig. 11(d). The matching circuits are the replica of the phase-controlled frequency divider and the multiplexers.

3. Jitter Tolerance Analysis

For a GVCO, the phase tracking process is similar to the "sample and hold" in phase domain as shown in Fig. 12. It is because the phase of a GVCO aligns with input data once the data transition occurs. To recover the data correctly, the phase error between the GVCO and input data can not exceed $0.5UI$, i.e.,

$$|\Phi_{\text{data}} - \Phi_{\text{GVCO}}| < 0.5UI \tag{1}$$

where Φ_{data} and Φ_{GVCO} is the phase of the input data and GVCO, respectively. Since the data transition occurs at discrete time, the phase of input data and that of the GVCO are expressed as

$$\Phi_{\text{data}} = A\cos\omega(nT) \tag{2}$$

$$\Phi_{\text{GVCO}} = A\cos\omega(n-k)T \tag{3}$$

where A is the amplitude of the jitter modulation, ω is the jitter modulation frequency of the input data, T is the bit time of the input data, n is the time index and k is the number of the successive identical bits in the input data.

Considering the static phase error and noise from the GVCO, the time uncertainty $U(t)$ is adopted. Since there is a frequency deviation between the data rate and the free run

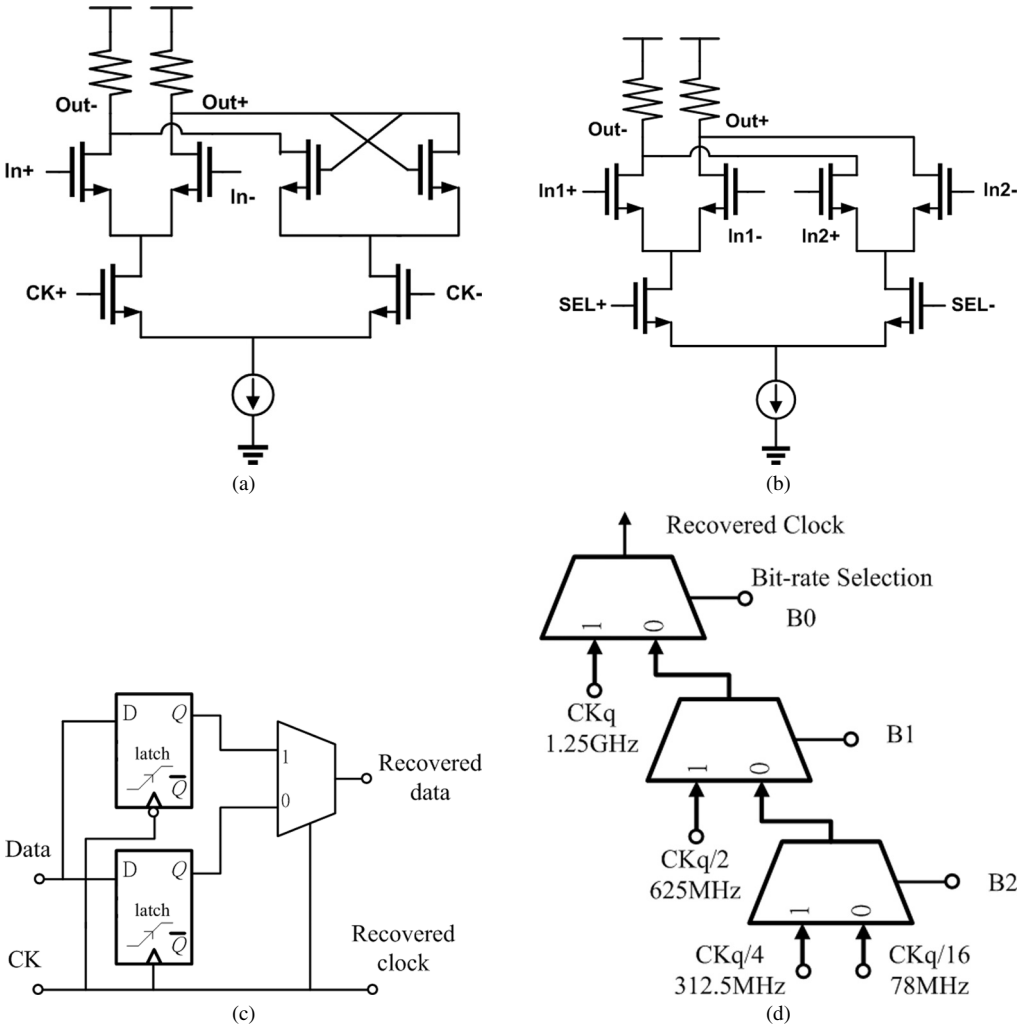


Fig. 11 (a) CML latch, (b) CML multiplexer, (c) CML DDFF and (d) 4-to-1 multiplexer.

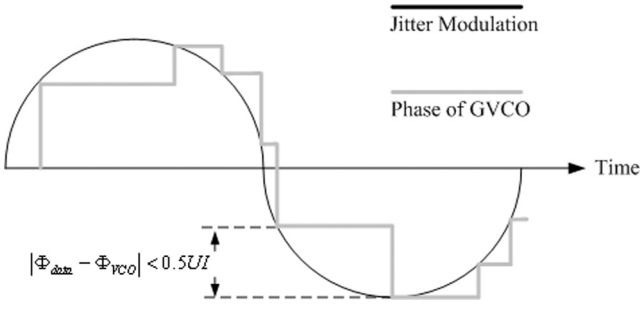


Fig. 12 Jitter tracking process.

frequency of the GVCO, their phases will drift away without any data transition and $\frac{\Delta f}{f_{\text{nom}}}k$ is also included, where Δf means the frequency deviation and f_{nom} means the nominal frequency of the GVCO, and the ratio is multiplied by k because this deviation will accumulate jitter for successive k identical bits. Equation (1) is modified as

$$|A\cos\omega(nT) - A\cos\omega(n-k)T| < 0.5 - U(t) - \frac{\Delta f}{f_{\text{nom}}}k \quad (4)$$

After calculations, Eq. (4) becomes

$$A < \frac{0.5 - U(t) - \dfrac{\Delta f}{f_{\text{nom}}}k}{\left|2\sin\left[\dfrac{\omega\cdot T\cdot(2n-k)}{2}\right]\sin\left[\dfrac{\omega\cdot T\cdot k}{2}\right]\right|} \quad (5)$$

From Eq. (5) and Fig. 12, the jitter tolerance changes when the long run bits change at different time index n. From Fig. 12, if the long run bit happens at steeper part in jitter modulation, the maximum jitter modulation amplitude is smaller. To predict the worst case, the maximum jitter modulation amplitude becomes

$$A < \frac{0.5 - U(t) - \dfrac{\Delta f}{f_{\text{nom}}}k}{2\sin\dfrac{\omega\cdot T\cdot k}{2}} \quad (6)$$

Because $\frac{\omega\cdot T\cdot k}{2}$ is much smaller than one, the maximum jitter modulation amplitude of Eq. (6) is simplified as

$$A < \frac{0.5 - U(t) - \dfrac{\Delta f}{f_{\text{nom}}} k}{\omega \cdot T \cdot k} \tag{7}$$

Equation (7) can be used to calculate the jitter tolerance for the GVCO-based burst-mode CDR circuits. The simulated time uncertainty is $0.02UI$ and $0.27UI$ for the proposed GVCO and the conventional one, respectively, as shown in Figs. 6(a) and (b). The jitter tolerance of both GVCO-based burst-mode CDR circuits are simulated as shown in Fig. 13

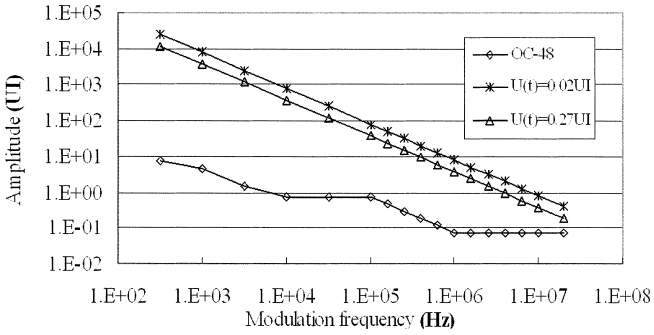


Fig. 13 Simulated jitter tolerance.

with $k = 23$ and $\frac{\Delta f}{f_{\text{nom}}}$ =500 ppm. The jitter tolerance mask for OC-48 application is also provided. The jitter tolerance of the CDR circuit using the proposed GVCO has a better

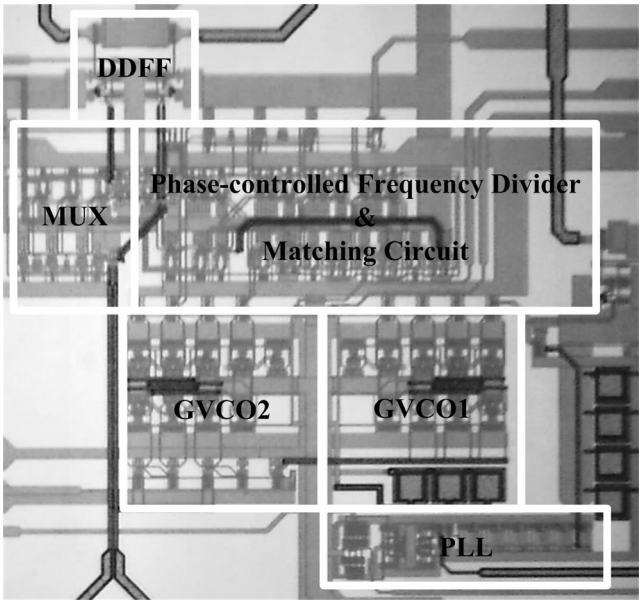
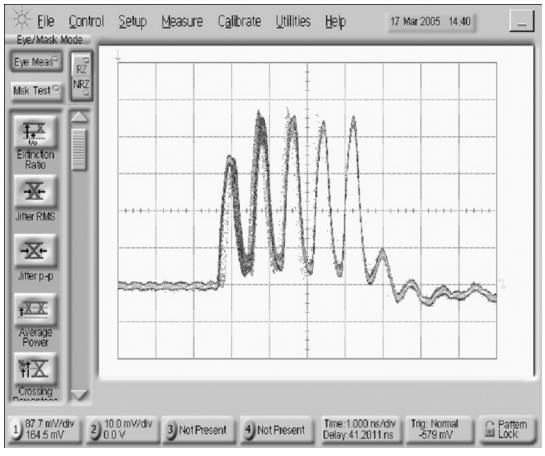
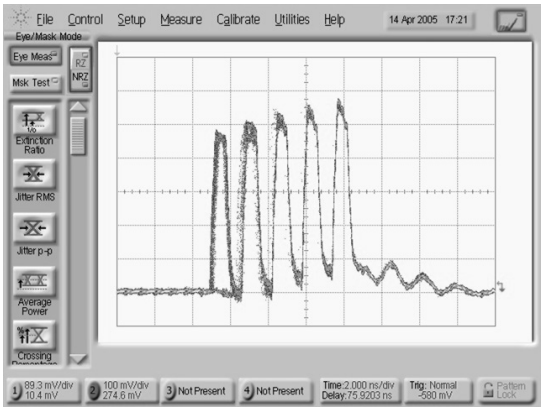


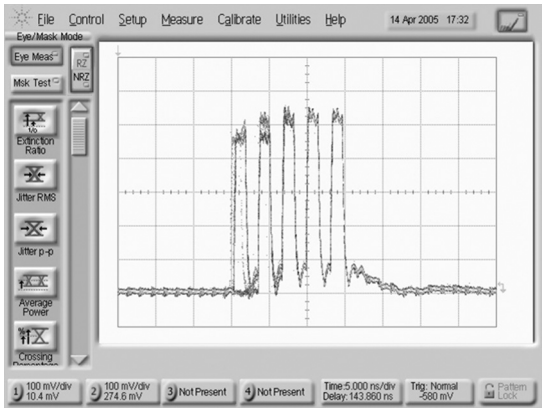
Fig. 14 Die photo.



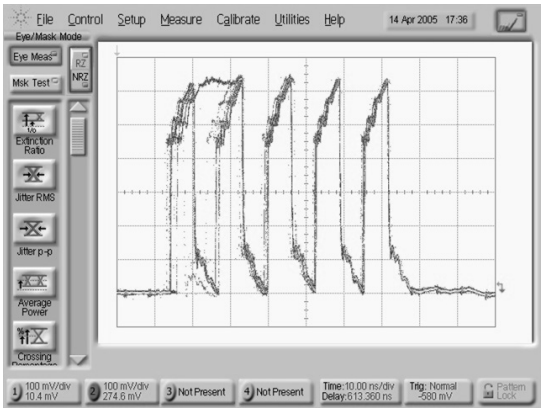
(a) 2488.32 Mbps



(b)1244.16 Mbps

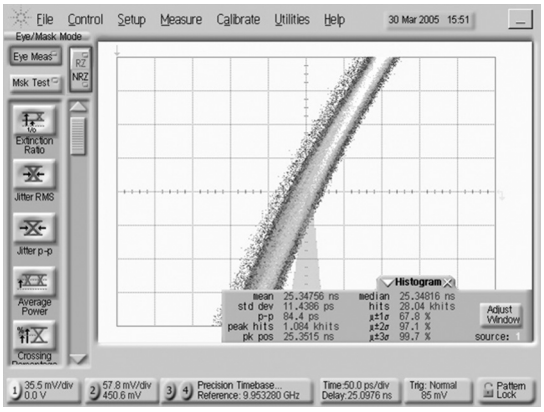


(c) 622.08 Mbps

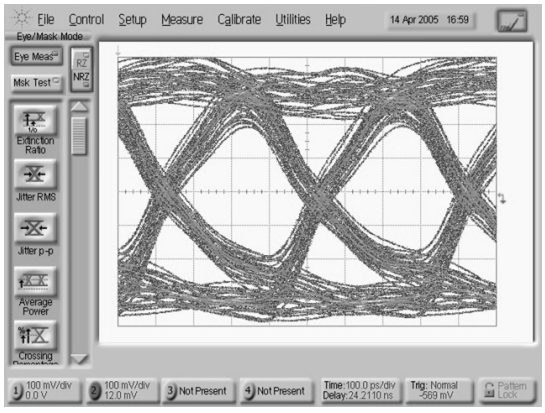


(d) 155.52 Mbps

Fig. 15 The measured burst-mode acquisition at different data rates.



(a)



(b)

Fig. 16 (a) The measured jitter for the recovered clock, (b) the measured eye diagram for a 2.44832 Gbps PRBS of $2^7 - 1$.

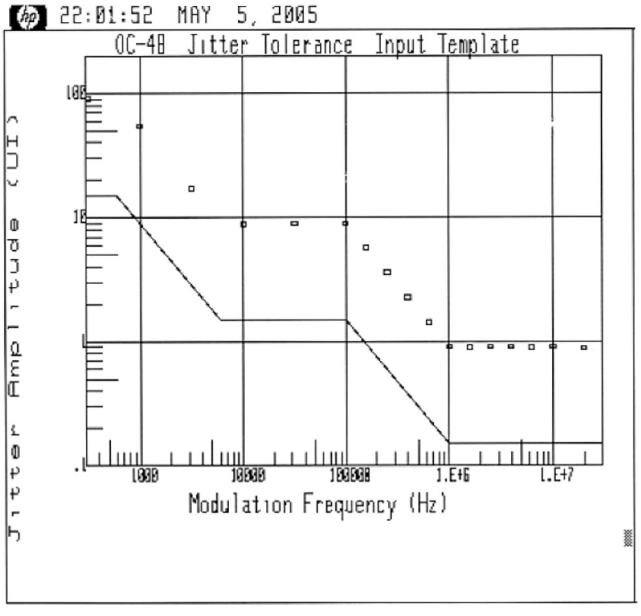


Fig. 17 Measured jitter tolerance at 2.48832 Gbps.

performance.

4. Experimental Results

This chip has been fabricated in a 0.18 μm CMOS process. The die photo is shown in Fig. 14 and the core area is 0.41 mm^2. The power dissipation is 70 mW from a 1.8 V supply voltage. Figure 15 shows the burst-mode acquisition at different data rate. The data pattern is set "1 0 1 0 1 0 1 0 1" followed by one hundred "0." Therefore, the phase of the recovered clock is somewhat uncertain during the "zero zone," and after about six data transitions, the recovered clock locks with data. In Fig. 15, the first bits have been correctly recovered; however, the transient jitter is larger than usual one [7]. To declare the performance in a conservative way similar to [7], the locked time is less than 7 bits. On the other hand, the specification of data acquisition time for GPON is 108 bits at a data rate of 2488.32 Mbps, so the proposed burst-mode CDR still meets the requirement well. Figure 16(a) shows the measured jitter for the recovered clock and Fig. 16(b) shows the measured eye diagram for the recovered data for a 2.44832 Gbps PRBS of $2^7 - 1$. Other data rates are also measured, but they are not shown in here. Under a PRBS of $2^{23} - 1$, the measured jitter tolerance is shown in Fig. 17 compared with the OC-48 mask. In the measurement, the amplitude of the jitter modulation is limited by instruments, but the simulated jitter tolerance is actually better than the measured one as indicated Fig. 12. The measurement results are summarized in Table 1. In Table 1, since the PLL in our CDR circuit is not synchronized with the pattern generator under measurement, there is some

Table 1 Measurement summary.

Data rate	2488.32Mbps, 1244.16Mbps 622.08Mbps, and 155.52Mbps
Process	CMOS 0.18um
Supply	1.8V
Power	70mW @ 1.8V
Frequency tolerance	>4%
Active area	0.41mm^2
Rms Jitter of the recovered clock	11.44ps with a PRBS of 2^7-1 15.26ps with a PRBS of $2^{31}-1$
Peak-to-Peak Jitter of the recovered clock	84.4ps with a PRBS of 2^7-1 115.16ps with a PRBS of $2^{31}-1$
Locking time	6 bits
BER	$<10^{-12}$ with a PRBS of 2^7-1

Table 2 Comparisons with previous BMCDR circuits.

	[6]	[7]	[8]	This Work
Data rate	2.5Gbps 1.25Gbps	10Gbps	622Mbps	2488.32Mbps 1244.16Mbps 622.08Mbps 155.52Mbps
Process	CMOS 0.18um	CMOS 0.13um	CMOS 0.35um	CMOS 0.18um
Supply	1.8V	2.5V	3.3V	1.8V
Power	60mW without buffers	1.2W	130mW	70mW
Die size	N/A	2.5mm x 2.5mm	2.1mm x 2.1mm	1.5mm x 1mm
Rms Jitter	16.19ps (2^7-1)	3.2ps (2^{31}-1)	11.35ps (PLL)	11.44ps (2^7-1)
Pk-Pk Jitter	108ps (2^7-1)	19.6ps (2^{31}-1)	76ps (PLL)	84.4ps (2^7-1)
Locked time	1bit	3bits	1bit	<7 bits
BER	N/A	$<10^{-12}$	$<10^{-12}$	$<10^{-12}$

frequency mismatch between our GVCO and the input data. It makes the measured jitter worse under a longer consecutive identical digit (CID) for a PRBS of $2^{31}-1$. Table 2 gives the performance comparisons with the previous works.

5. Conclusions

A multi-band BMCDR circuit using frequency dividers is implemented in 0.18 μm CMOS process. The proposed GVCO prevents the latching operation so as to provide much better performance on ISI than the conventional GVCO, and the modified frequency dividers that choose the correct sampling phase automatically can provide multi-band operation. This chip includes a CDR core and a PLL that provide the control voltage to the GVCO in the CDR core. This chip consumes 70 mW with 1.8 V power supply and exhibits BER $< 10^{-12}$ with a $2^7 - 1$ PRBS.

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