

Proposal of a Desk-Side Supercomputer with Reconfigurable Data-Paths Using Rapid Single-Flux-Quantum Circuits

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SUMMARY We propose a desk-side supercomputer with large-scale reconfigurable data-paths (LSRDPs) using superconducting rapid single-flux-quantum (RSFQ) circuits. It has several sets of computing unit which consists of a general-purpose microprocessor, an LSRDP and a memory. An LSRDP consists of a lot of, e.g., a few thousand, floating-point units (FPUs) and operand routing networks (ORNs) which connect the FPUs. We reconfigure the LSRDP to fit a computation, i.e., a group of floating-point operations, which appears in a 'for' loop of numerical programs by setting the route in ORNs before the execution of the loop. We propose to implement the LSRDPs by RSFQ circuits. The processors and the memories can be implemented by semiconductor technology. We expect that a 10 TFLOPS supercomputer, as well as a refrigerating engine, will be housed in a desk-side rack, using a near-future RSFQ process technology, such as 0.35 μm process.

key words: *superconductor, rapid single-flux-quantum circuit, reconfigurable data-path, high-performance computing, supercomputer*

1. Introduction

Superconducting rapid single-flux-quantum (RSFQ) circuit technology [1] is expected to be a next generation circuit technology which enables ultra high-speed computation with ultra low-power consumption [2]. Several simple RSFQ microprocessor LSIs with more than ten thousand Josephson junctions have been fabricated using 2 μm process technology [3]–[5]. 1 μm process technology with five interconnection layers is now available [6]. The increase of the wiring layers combined with the passive transmission line technology [7], [8] further increases the circuit integration density. Now, it is attractive to make study on computing systems using RSFQ circuits which are difficult to be implemented by using semiconductor circuits. In this paper, as such a computing system, we propose a desk-side supercomputer using RSFQ circuits.

Numerical analysis and simulation of large and compli-

cated systems are necessary for research and development in various fields. Providing high computation power to individual researchers is crucial for progress of the research and development. A desk-side supercomputer will provide such high computation power to individual researchers. Note that implementing such a compact supercomputer by using semiconductor circuits is difficult because of the heat radiation.

RSFQ circuits have good features of high-speed switching, high-speed signal transmission, low power consumption and hence low heat radiation, etc. In order to make the most of these features in a desk-side supercomputer, we have to adopt a computer architecture suitable for RSFQ implementation. Especially, it is important to balance the computation speed and the memory bandwidth and to solve so-called 'memory-wall problem.' 'Memory-wall problem' is the problem that the memory bandwidth cannot be wide enough related to the processor performance because of the gap between the operating speed of a processor and that of a memory, and hence, the performance of a computer is limited [9], [10]. In an RSFQ supercomputer, this problem would be more crucial, because RSFQ circuits operates so fast while large-scale superconductive random access memory seems difficult to be implemented.

We propose a desk-side supercomputer with large-scale reconfigurable data-paths (LSRDPs) using RSFQ circuits. It has several sets of computing unit which consists of a (general-purpose) microprocessor, an LSRDP and a memory. An LSRDP consists of a lot of, e.g., a few thousand, floating-point units (FPUs) and operand routing networks (ORNs) which connect the FPUs [11]. We reconfigure the LSRDP to fit a computation, i.e., a group of floating-point operations, which appears in a 'for' loop of numerical programs, by setting the route in ORNs before the execution of the loop. In the LSRDP, a lot of FPUs work in parallel with pipelined fashion, and hence, very high-performance computation is achieved. Furthermore, since the output of an FPU is forwarded to another FPU via an ORN, memory access for storing/loading intermediate results is no longer necessary, and hence, the 'memory-wall problem' is relaxed. We propose to implement the LSRDPs by RSFQ circuits. (We call them SFQ-RDPs.) The processors and the memories can be implemented by semiconductor technology. We expect that a 10 TFLOPS supercomputer, as well as a refrigerating engine, will be housed in a desk-side rack, using a near-future RSFQ process technology, such as

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0.35 μm process.

In the next section, we will briefly describe the features of RSFQ circuits. In Sect. 3, we will explain the LSRDP. In Sect. 4, we will propose a desk-side supercomputer with SFQ-RDPs. Section 5 will conclude the paper.

2. Features of RSFQ Circuits

The basic component of RSFQ digital circuits is a superconducting loop with Josephson junctions. A single-flux quantum, which appears as a voltage pulse (SFQ pulse), is used as the carrier of information. The width of an SFQ pulse is several pico-seconds and the height is about 1 mV. Therefore, the energy consumed for switching is much smaller and the speed for switching is higher than those of CMOS circuits, respectively.

By the passive transmission line (PTL) technology developed recently, in an RSFQ chip, ballistic transmission of an SFQ pulse on superconducting wirings is possible, and therefore, fast and high-throughput intra-chip signal transmission is achieved [7], [8]. Note that RSFQ circuits are free from a delay for recharge process of capacitors/inductors, in contrast to CMOS circuits. Furthermore, by the recently developed multi-chip module (MCM) technology, inter-chip transmission of an SFQ pulse at throughput over 100 Gbps is also achieved [14].

Several simple RSFQ microprocessor LSIs with more than ten thousand Josephson junctions have been fabricated using 2 μm process technology [3]–[5]. 1 μm process technology with five interconnection layers is now available [6]. The increase of the wiring layers combined with the PTL technology further increases the circuit integration density. For the recent progress of RSFQ circuit technology, see e.g., [2], [5]. Note that the operating speed and integration density of RSFQ circuits increase with scale-down of dimensions, as semiconductor LSIs.

The number of gates that can be integrated into an RSFQ LSI chip is much fewer than a CMOS chip at present. However, since the heat radiation is very low, high-density packaging is possible using the MCM technology, and therefore, large-scale RSFQ circuits can be implemented more compactly than CMOS circuits. Recall that the throughput of inter-chip signal transmission is comparable to that of intra-chip signal transmission.

Since an SFQ pulse is used as the carrier of information, RSFQ circuits work by pulse logic. Therefore, each logic gate of RSFQ circuits is a clocked gate and has a function of latch. In other words, latches can be implemented without additional costs. RSFQ digital circuits are suitable for pipeline processing on streaming data. On the other hand, they are not suitable for processing with feedback loops and conditional branches.

As stated above, RSFQ circuits have many good features. Development of a desk-side supercomputer may be possible, using these features. In order to make the most of these features in a computer, we have to adopt a computer architecture suitable for RSFQ implementation. Espe-

cially, it is important to balance the computation speed and the memory bandwidth, as will be stated in the next section.

3. Large-Scale Reconfigurable Data-Path

The main challenge of the desk-side supercomputing is to develop a compact, high-performance computation engine. On the other hand, the memory-wall problem is emerging as one of the greatest impediments to the microprocessor system performance [9], [10]. As a solution to this problem, we adopt the Large-Scale Reconfigurable Data-Path.

3.1 Memory-Wall Problem: A Performance Limitation in Parallel Computing

‘Memory-wall problem’ is the problem that the memory bandwidth cannot be wide enough related to the processor performance because of the gap between the operating speed of a processor and that of a memory, and hence, the performance of a computer is limited [9], [10].

Nowadays, there are many applications which are the target of supercomputer systems. An example is molecular orbital calculation which is indispensably required to analyze or predict various chemical properties theoretically.

The most laborious part of molecular orbital application comprises four parallel loops, in which various types of molecular integrals are calculated numerously. In the calculations whose angular momentum is up to 1, each molecular integral calculation has 17 inputs and from 1 to 81 outputs. On the other hand, the amount of floating point arithmetic operations for each calculation is between 122 and 1237, and the critical path length of data flow graphs (DFGs) is from 13 to 76. Therefore, regardless of the features in four parallel loops, each loop has the potential to be executed efficiently under the parallel computation by using the small number of I/O data.

To execute this application efficiently, PC cluster computers or vector type computers have been utilized. Similarly, to achieve the calculation performance, a parallel computer referred to as EHPC/ERIC has been developed formerly for the molecular orbital calculation in part of our research work [12], [13]. This computing system exploits many processor nodes, which are special purpose processors for the molecular integral calculation, for four parallel loop calculations, hence, achieving remarkable parallelization efficiency. However, processing a large amount of intermediate data for calculating molecular integrals in loop bodies is a bottleneck in obtaining higher speedup. The ratio of the time spent for executing load/store operations to the total execution time is 90% which is noticeable due to necessity of accessing to the main memory by the high fraction of load/store instructions. This shows a typical memory-wall problem.

3.2 LSRDP: A Well Balanced Approach Between Computing Performance and Amount of Memory Accesses

Generally speaking, by improving the parallel arithmetic operations, higher memory bandwidth will be required which is a barrier in the performance improvement as mentioned before. However, according to the result of our experiments, 81% of load/store operations concerns to the read/write operations on the intermediate data (spill code). By eliminating the load/store operations which correspond to the spill code, a considerable performance improvement is achievable, hence, reduction in the required memory bandwidth while keeping a high computational performance.

In order to achieve this goal, we have proposed a complexity-effective high-performance accelerator called a Large-Scale Reconfigurable Data-Path (LSRDP) [11]. An LSRDP mainly consists of two parts: a 2-dimensional array of FPUs and flexible operand-routing networks (ORNs) as depicted in Fig. 1. The LSRDP has the following features.

Providing Large-Scale FPU Array: We use hardware resources for *computational unit* rather than *memory*. Unlike recent high-end microprocessor chips, we do not dissipate the hardware budget to on-chip memory like caches. This design strategy makes it possible to implement a thousand of FPUs on a chip or in a MCM by advanced future process technologies, resulting in extremely high peak performance. The FPUs are arranged as a 2-dimensional array and the output of each FPU can be fed to one or more FPUs via ORN switches. We do not support feedback connections. Namely, the flow of data in the FPU array is one way. This complexity-effective microarchitecture makes the implementation of an LSRDP easier, and potentially can im-

prove its operation frequency.

Achieving Low Memory-Bandwidth Pressure: In an LSRDP, a data flow graph (DFG) extracted from a target application program is mapped to the 2-dimensional FPU array. Since the cascaded FPUs can generate a final result without temporally memorizing intermediate data, we can reduce the number of memory load/store operations corresponding to spill codes. Therefore, memory bandwidth required to achieve high performance can be reduced. Furthermore, since a loop-body mapped into the FPU array is executed in pipeline fashion, LSRDP can provide high throughput computing.

Supporting Coarse-Grain Re-configurability: An LSRDP has to be an adaptable accelerator, because we target various scientific applications. In order to satisfy this requirement, we allow dynamically reconfiguring the FPUs and ORNs. Originally, FPUs support multiple functions such as add, sub, and multiply, and an ORN consists of programmable switches. By means of setting the control signals provided to FPUs and ORN switches, we can change the function of the LSRDP at run time. This flexibility makes it possible to implement various DFGs onto the FPU array.

4. Desk-Side Supercomputer with SFQ-RDPs

We propose a desk-side supercomputer with LSRDPs using RSFQ circuits. It has several sets of computing unit which consists of a (general-purpose) microprocessor, an LSRDP and a memory, as shown in Fig. 2. Data are fed to the LSRDP from the memory via streaming buffers (SBs). We propose to implement the LSRDPs, as well as the SBs, by RSFQ circuits. Recall that LSRDPs have features suitable for RSFQ implementation as shown in the previous section. The processors and the memories can be implemented by semiconductor technology.

As a feasibility study, we have estimated the system size and power consumption of 10 TFLOPS SFQ-LSRDP system assuming a near-future RSFQ process technology. The specification of the assumed process is described in Table 1. The design rule, the critical current density of Josephson junctions (JJs), J_c , and the number of metal layers of the present advanced RSFQ process are $1\ \mu\text{m}$, $10\ \text{kA}/\text{cm}^2$ and 9 (5 for wiring), respectively [6]. Therefore the assumed process seems to be available in the near future. Due to its eight-times higher J_c , the clock frequency of beyond 80 GHz is achieved even in complex digital systems. We also assume self-shunt junction technology in the process, which will reduce the area of the circuits effectively by eliminating the shunt resistance [15].

According to a rough estimation based on our previous study of RSFQ microprocessors [3]–[5], 80 GHz 4-bit-slice 64-bit floating-point adders and multipliers can be designed

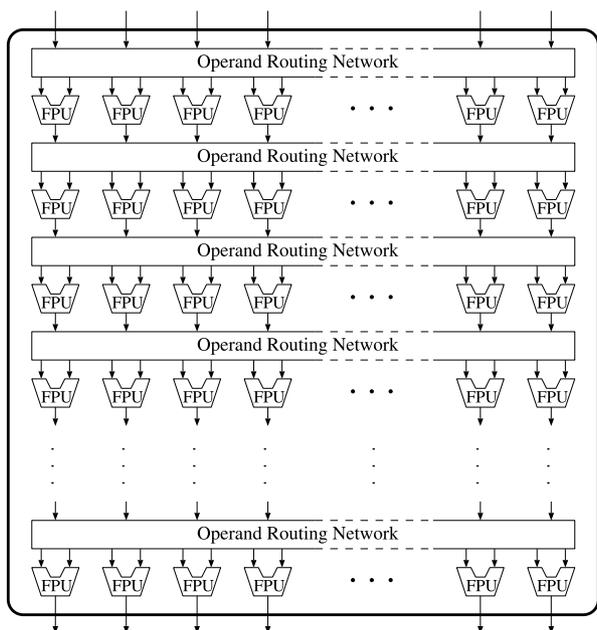


Fig. 1 A large-scale reconfigurable data-path.

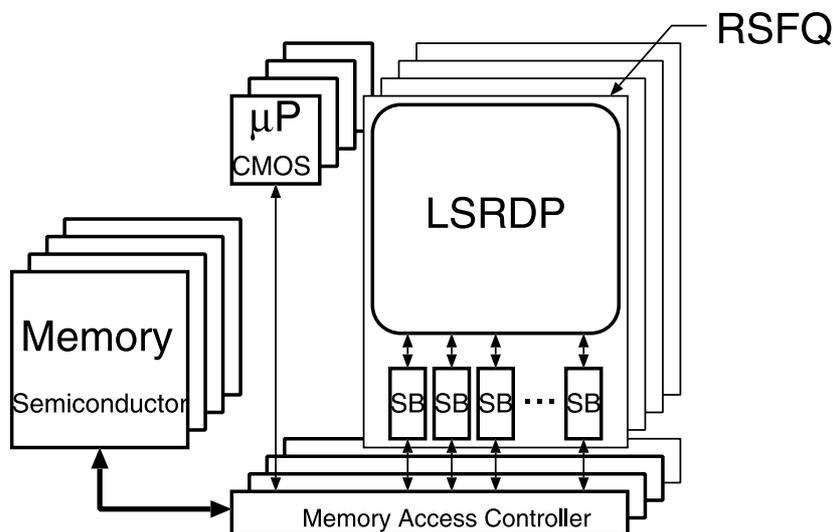


Fig. 2 A supercomputer with SFQ-RDPs.

Table 1 The assumed RSFQ process technology.

Minimum line width	0.35 μm
Critical current density J_c of JJs	80 kA/cm ²
# of JJs per chip	5.0 M/1 cm square die
Operating clock frequency	80 GHz
# of metal layers	9 (5 wiring layers)

by using about 80,000 JJs, which have 4 GFLOPS operation performance. Assuming the same number of JJs for a one-to-eight RSFQ ORN per FPU, one row of 32 FPUs with an ORN can be integrated on a 1 cm square die. A resultant SFQ-RDP chip has a performance of 128 GFLOPS and consumes electric power of about 51.2 mW. It should be noted that we assumed the LR biasing technique to reduce the power consumption of RSFQ circuits in the estimation [16].

32 SFQ-RDP chips and two 64 Kb SB chips will be mounted on an 8 cm square multi-chip module (MCM) which provides superconducting chip-to-chip interconnections of an 80 Gbps/channel bandwidth. The 34 chips will be connected in series. Consequently, one MCM will contain an LSRDP including 1024 FPUs, i.e., a square array of 32 by 32 FPUs. The total peak performance and power consumption of the MCM are estimated to be about 4.1 TFLOPS and 1.6 W, respectively.

The maximum and the minimum required memory bandwidths theoretically depend on the number of FPUs in each row, the execution rate of floating point operations by each FPU and the number of source operands for each FPU. For a configuration comprising 32×32 FPUs with the capability of executing 4GFLOPS/FPU and two double floating point operands for each FPU, the maximum and the minimum required input bandwidths are 2 TB/s (32FPUs) and 64 GB/s (1FPU), respectively. On the other hand, the maximum and the minimum required output bandwidths are 1 TB/s (32FPUs) and 32 GB/s (1FPU), respectively. In a molecular integral real application, for a DFG including 17

inputs and 1 output, input and output bandwidths are 1 TB/s and 32 GB/s, respectively. Moreover, in the case where all four indices in the four parallel loops introduced in Sect. 3.1 have the same value, the required input bandwidth can be reduced to 256 G–512 GB/s. The required bandwidths are being approximated at present time, since a precise evaluation depends on the SBs, configuration of the FPU array, data transferring method from memory to the MCM, the input size of application, and so on. Here, we assume that the bandwidth for each MCM is 512 GB/s.

The activity of FPUs in weighted average is estimated to be almost 60%. This number comes from our LSRDP mapping results. Activity of FPUs in LSRDP depends on FPU utilization multiplied by execution time ratio which is the ratio of time spent for DFG execution to their total execution time. For calculation of the molecule named Gly-Ala-Gln-Met-Tyr peptide where four parallel loop calculations are executed as explained in Sect. 3.1, it is required to map at least five DFG expressions to the FPU array of LSRDP. The second and the third recursive expressions exploit 64% of FPUs, the others require 60%. If the size of a DFG (e.g., DFG corresponding to the fifth recursive expression) exceeds 1024 (32×32 FPUs), it should be divided to smaller DFGs to be mappable onto the LSRDP. For each DFG, a configuration bit-stream is generated which is loaded on the LSRDP at run-time. Execution latency of a recursive calculation depends on the number of DFGs generated for the expression as well as the LSRDP maximum execution latency. Each of the first four DFGs belonging to recursive expressions needs one configuration to map on LSRDP, but the last DFG needs two configurations. By utilizing the ratio of subtotal execution time of each DFG, the weighted average of FPU's activity is 61%.

Providing four sets of the computing unit, we will have a 10 TFLOPS supercomputer, which consumes electric power of about 6.5 W. Total bandwidth between the MCMs at 4.2 K and the memories at room temperature is 2 TB/s,

Table 2 The performance, number of JJs and power consumption of the SFQ-RDP system and those of its components.

	Performance	# of JJs	Power consumption
1 FPU	4 GFLOPS	80k	0.8 mW
1 Chip (32 FPUs with an ORN)	128 GFLOPS	5.12 M	51.2 mW
1 MCM (32 FPU chips and 2 SB chips)	peak: 4.1 TFLOPS effective: 2.5 TFLOPS	164 M	1.6 W
System (4 MCMs)	peak: 16.4 TFLOPS effective: 10 TFLOPS	656 M	7.7 W (7.7 kW for 4.2 K refrigerator)

and to sustain the bandwidth, more than 1,000 sets of an interface and a cable are necessary assuming the interface bandwidth of 20 Gb/s. The power consumption of an interface is estimated to be about 200 μ W. Heat flow from a cable with low thermal conductivity, such as brass semi-rigid coaxial cables with the diameter of 0.86 mm, is evaluated to be less than 1 mW. Finally, we found that the power consumption of the RSFQ-RDP system at 4.2 K is about 7.7 W. This power will be easily removed by using commercially available refrigerators with wall outlet power of about 7.7 kW in the near future.

The performance, the number of JJs and the power consumption of the SFQ-RDP system and those of its components are listed in Table 2. On the other hand, if we fabricate a 10 TFLOPS machine using state-of-the-art RISC-based CMOS microprocessors, the total system occupies 30 racks and consumes electric power of about 120 kW. It should be also noted that if we implement a 2.5 TFLOPS LSRDP chip using a future 45 nm CMOS technology, the power consumption of the chip will be about 1 kW, which is far from the cooling limit of a chip.

5. Conclusion

We have proposed a desk-side supercomputer with large-scale reconfigurable data-paths using superconducting rapid single-flux-quantum circuits. We expect that a 10 TFLOPS supercomputer, as well as a refrigerating engine, will be housed in a desk-side rack, using a near-future RSFQ process technology, such as 0.35 μ m process.

In order to develop fundamental technologies for an SFQ-RDP, researches on the following issues are necessary.

- LSRDP architecture
 - Optimization of LSRDP architecture
 - A compiler for LSRDP
 - Algorithms suitable for execution on LSRDP
- SFQ-RDP
 - Floating-Point arithmetic circuits for SFQ-RDP
 - Routing network for SFQ-RDP
- Support for RSFQ circuit design
 - Logic cell library
 - CAD tools for layout and logic design
- RSFQ process and circuit technologies
 - Reliable process technology
 - Advanced wiring technology

We have started a five-year project for these researches [17].

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