LETTER

MTR-Fill: A Simulated Annealing-Based X-Filling Technique to Reduce Test Power Dissipation for Scan-Based Designs

Dong-Sup SONG[†a)], **Jin-Ho AHN**[††], **Tae-Jin KIM**[†], *Nonmembers, and* **Sungho KANG**[†b)], *Member*

SUMMARY This paper proposes the minimum transition random X-filling (MTR-fill) technique, which is a new X-filling method, to reduce the amount of power dissipation during scan-based testing. In order to model the amount of power dissipated during scan load/unload cycles, the total weighted transition metric (TWTM) is introduced, which is calculated by the sum of the weighted transitions in a scan-load of a test pattern and a scan-unload of a test response. The proposed MTR-fill is implemented by simulated annealing method. During the annealing process, the TWTM of a pair of test patterns and test responses are minimized. Simultaneously, the MTR-fill attempts to increase the randomness of test patterns in order to reduce the number of test patterns needed to achieve adequate fault coverage. The effectiveness of the proposed technique is shown through experiments for ISCAS'89 benchmark circuits.

key words: *low power test, scan-based test, X-filling, test application time*

1. Introduction

Power dissipation during testing becomes a significant problem as the size and complexity of system-on-chips (SoCs) continue to grow. The excessive power during testing may cause several problems including circuit damage, yield loss, and increased product costs. Previous techniques for test power reduction have focused on reducing the shift power dissipation during test applications, which is based on four major approaches: scheduling, test vector manipulation, circuit modification, and scan chain modification.

As one of test vector modification methods, X-filling techniques have already been shown to be efficient in reducing power during testing [1]–[3]. The X-filling techniques are heuristics for assigning 0's or 1's to X values in test cubes in order to better achieve a specific goal. Because the X-filling techniques utilize the X-values that are the greater part of all the bits in the test cubes, the switching activities obtained from the X-filled test patterns can be significantly reduced. Random X-filling (R-fill) and minimum transition X-filling (MT-fill) are widely used X-filling methods in industry [4]. When power is a consideration, it is generally better to use MT-fill. MT-fill involves filling strings of X's with the same value to minimize the number of transitions. While MT-fill minimizes power, it has the following two drawbacks:

- Because MT-fill may not be as effective as R-fill for detecting additional faults, the number of test patterns that are needed to achieve complete fault coverage is increased.
- Despite its effectiveness in reducing power dissipation during testing, MT-fill has the disadvantage of not considering signal transitions in the scan-unload of a test response but only minimizing the weighted transition metric (WTM) in the scan load of a test pattern.

To overcome this problem, a novel simulated annealing algorithm is proposed that is based on the X-filling technique, which is called the minimum transition random X-filling (MTR-fill). In order to consider signal transitions in both the scan-load of a test pattern and the scan-unload of a test response simultaneously, the proposed MTR-fill uses the total weighted transition metric (TWTM) as a cost function of the simulated annealing process. The TWTM is calculated by the sum of weighted transitions in the test pattern and the corresponding test response. The new solution of the simulated annealing process is determined so that the randomness of the intermediate test pattern is increased. If the TWTM cost of the new solution is less than that of the current solution, the new solution is accepted as the best solution. Therefore, with the simulated annealing process, test patterns generated by the proposed MTR-fill obtain appropriate fault coverage with smaller-sized test patterns and lower amounts of testing power dissipated compared with those required by MT-fill.

2. Basic Idea

Scan shifting power dissipation includes not only the power dissipation that is produced during the scan-load of a test pattern, but also the power dissipation that is produced during the scan-unload of a test response. MT-fill is clearly effective in minimizing the test power dissipation that is produced during the scan load. However, since MT-fill does not consider signal transitions during the scan unload, minimization of the scan shifting power dissipation cannot be guaranteed when carrying out a scan test. Consider the following example.

Assume that a scan chain test cube t_i of the circuit shown in Fig. 1 is as follows: $t_i = \{F_1, F_2, F_3, F_4, F_5\}$ = XXXX1. In addition, t_1 = 11111 and t_2 = 10111 are scan chain test patterns that are obtained after X-filling on the scan chain test cube of t_i. Here, t_1 is the MT-filled scan

Manuscript received September 5, 2007.
Manuscript revised November 30, 2007.

[†]The authors are with the Department of Electrical and Electronic Engineering, Yonsei University, Korea.
[††]The author is with the Department of Electronic Engineering, Hoseo University, Korea.
a) E-mail: songdongsup@dopey.yonsei.ac.kr
b) E-mail: shkang@yonsei.ac.kr

DOI: 10.1093/ietisy/e91–d.4.1197

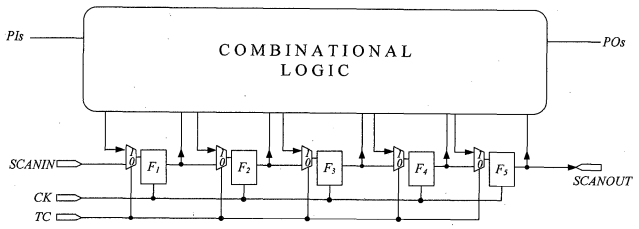

Fig. 1 Example of a full-scan circuit.

chain test pattern. The WTM metric models the fact that the scan in power for a given scan chain test pattern depends not only on the number of transitions in the pattern but also on their relative positions. Consider a scan chain of length L and a scan chain test pattern $t_i = \{t_{i,1}, t_{i,2}, \ldots t_{i,L}\}$ where $t_{i,j}$ represents the j-th bit of t_i. The WTM for t_i is given by:

$$WTM(t_i) = \sum_{j=1}^{L-1} (L-j) \cdot (t_{i,j} \oplus t_{i,j+1})$$

According to the definition of WTM, the WTM of t_1 is 0 and WTM of t_2 is 3. During the scan-load, t_1 is expected to have less power dissipation than t_2. However, this does not mean that t_1 is more power-effective than t_2. This is because scan shifting consists of both a scan-load and a scan-unload. Assume that when t_1 and t_2 are applied to the circuit the scan chain test responses, r_1 = 01010 and r_2 = 00111, are obtained, respectively. During the scan-unload, the WTM of r_1 is calculated to be 10, and WTM of r_2 is calculated to be 2. As a result, the MT-filled test pattern, t_1, has a total of 10 weighed signal transitions during scan shifting, whereas t_2 has only 5 weighted signal transitions.

The randomness of a scan chain test pattern t_i is given by:

$$randomness\ of\ t_i = \frac{\min(N_1(t_i), N_0(t_i))}{L}.$$

Here, $N_1(t_i)$ is the number of "1" bits in the scan chain test pattern t_i and $N_0(t_i)$ is the number of "0" bits in the scan chain test pattern t_i. The randomness of a test pattern indicates the probability that it will detect additional faults with the test pattern when it is reversely fault simulated. As a test pattern increases randomness, the chance of detecting additional faults is increased. Therefore, if the randomness of each test pattern is increased, the required amount of test patterns that are needed can be reduced to achieve adequate fault coverage. According to the definition of randomness, the randomness of t_1 is 0, and the randomness of t_2 is 0.2. Because t_2 has higher randomness than t_1, which is X-filled by the MT-fill algorithm, it is more likely that t_2 will detect additional faults than t_1.

3. Minimum Transition Random X-Filling Algorithm

Figure 2 shows the proposed MTR-fill algorithm. The MTR-fill is implemented with simulated annealing processes. As the outermost loop (line 4) is iterated, the cost

```
1  Function Minimum Transition Random Fill {
2   INPUT: fault list f, T_init, T_low, IPT, K_T
3   OUTPUT: low power test pattern set T_new
4   while( there is no fault in the fault list f ) {
5     t_i = a deterministic test pattern with maximized X values
6     t_ibest = t_iinit = MT-fill(t_i);
7     r_ibest = r_iinit = obtain test response(t_iinit);
8     C_ibest = C_iinit = compute cost(t_iinit, r_iinit);
9     T = T_init;
10    while(T > T_low) {
11      if( no cost reduction in the last IPT iterations ) break;
12      for(i=1; i ≤ IPT; i++) {
13        t_inew = new solution(t_ibest);
14        r_inew = obtain test response(t_inew);
15        C_inew = compute cost(t_inew, r_inew);
16        ΔC = C_inew − C_ibest;
17        if(ΔC<0) t_ibest, r_ibest, and C_ibest are set to t_inew, r_inew, and C_inew;
18        else {
19          p = e^(-ΔC/T);
20          if(random[0,1] < p))
21          t_ibest, r_ibest, and C_ibest are set to t_inew, r_inew, and C_inew;
22        }
23      }
24      T = K_T × T;
25    }
26    delete fault f_s that can be detected by t_ibest from fault list f
27    save t_ibest to T_new
28  }
29  } //End Minimum Transition Random Fill
```

Fig. 2 The proposed MTR-fill algorithm.

of the TWTM is minimized by appropriately assigning 0 or 1 to the X-value that exists in the test cube t_i. t_i is a deterministic test cube (line 5) that is generated by ATPG, so that the undetermined inputs remain X-values. The initial test pattern t_{iinit} and the initial test response r_{iinit} are the initial solutions of the annealing process, which are determined using t_i. The initial test pattern t_{iinit} is derived by MT-filling the X-values of t_i (line 6), and the initial test response r_{iinit} is the test response of the circuit on t_{iinit} (line 7). The proposed simulated annealing algorithm uses the TWTM with a pair consisting of a test pattern and a test response as a cost function in order to minimize the scan shifting power dissipation.

The TWTM of a pair consisting of a test pattern t_i and test response r_i is defined as follows.

$$TWTM(t_i) = \sum_{j=1}^{L-1} (t_{i,j} \oplus t_{i,j+1}) \times j + \sum_{j=1}^{L-1} (r_{i,j} \oplus r_{i,j+1}) \times j \quad (1)$$

Here, L represents the length of the scan chain, while $t_{i,j}$ and $r_{i,j}$ signify the j-th bit of t_i and r_i, respectively.

The initial cost C_{iinit} is calculated using t_{iinit} and r_{iinit} (line 8). The middle loop modifies the control parameter of the simulated annealing algorithm, which is gradually lowered as the annealing process proceeds. Within the inner loop, new solutions, t_{inew} and r_{inew}, are generated with a constant control parameter value by the following method (line 13, line 14).

- t_{inew} : Define the bit positions that are assigned to the X-value in the deterministic test cube t_i obtained from

line 4 as free positions. t_{inew} is the test pattern that is derived by flipping the k-th bit value of t_{ibest}. At this time, k is randomly selected from the free positions.

- r_{inew} : A test response pattern is acquired by applying t_{inew} on the circuit under test.

The cost C_{inew} is calculated using the cost function TWTM on the new solution t_{inew} and r_{inew} (line 15). If t_{inew} and r_{inew} produce the minimum cost of all the solutions, t_{inew} and r_{inew} are accepted as t_{ibest} and r_{ibest} (line 17). New solutions are either accepted or rejected depending on the acceptance criterion defined in the simulated annealing algorithm (line 19 – line 21). Here, random[0,1] is an uniform random number between 0 and 1 (line20). When the final best solution t_{ibest} is determined by the annealing process, all faults that are detected by t_{ibest} are eliminated from the fault list f (line 26). The above process is repeated until there are no more faults in the fault list f.

4. Experimental Results

In this section, the efficiency of the proposed MTR-fill is demonstrated for the ISCAS'89 benchmark circuits. During the simulated annealing process, the parameters are set up as $T_{init} = 5.0$, $T_{low} = 0.1$, $K_t = 0.9$, and $IPT = 500$. In the ATPG process, a random pattern testing session is not included and all test patterns are generated with a deterministic test pattern generation session by targeting the entire single stuck-at fault. The generated test patterns are compacted by the reverse order fault simulation. Each benchmark circuit was considered as a full scan circuit with a single scan chain.

Table 1 presents the results of the proposed MTR-fill algorithm, together with those by R-fill, 0-fill, and MT-fill. The 'Fault Cov.' column and the 'No. of Test' columns show the fault coverage obtained for stuck-at faults and the number of test patterns needed to acquire the corresponding fault coverage for each X-filling heuristic. The 'P_{ave}' and the 'P_{peak}' columns represent the average scan shifting power and the peak scan shifting power, respectively. These are given by the following equations.

$$P_{ave} = \frac{\sum_{i=1}^{N} TWTM(t_i)}{N} \tag{2}$$

$$P_{peak} = \max_{1 \le i \le N} TWTM(t_i) \tag{3}$$

The last column shows the effects of test length on the proposed MTR-fill technique. The 'Test redu.' column is calculated by the ratio of the number of reduced test patterns over the number of test patterns that are required in the MT-fill technique. The proposed MTR-fill attempts to increase the randomness of the test patterns by flipping the current logic value of a randomly selected bit during the simulated annealing process. As a consequence, the proposed method reduces the test length by 18.1% in comparison with those that use the MT-fill.

Table 2 compares the test power reduction of the proposed MTR-fill to that of previous works. Note that the test power reduction found in the previous work indicates only

Table 1 Experimental results of the proposed MTR-fill technique.

Circuit	Fault Cov. (%)	R-fill			0-fill			MT-fill			Proposed MTR-fill			
		No. of Test	P_{ave}	P_{peak}	No. of Test	P_{ave}	P_{peak}	No. of Test	P_{ave}	P_{peak}	No. of Test	P_{ave}	P_{peak}	Test redu. (%)
s5378	99.13	270	14132	16598	638	4225	6291	491	3361	5413	428	3026	5051	12.8
s9234	93.48	425	21895	25296	965	11168	13046	490	10470	13524	454	7085	9833	7.3
s13207	98.46	501	203713	225507	1711	90418	120941	589	87059	113070	546	52804	81241	7.3
s15850	96.68	474	141005	159914	1671	57910	83412	577	55441	81666	484	29741	55682	16.1
s35932	99.19	79	1379144	1595691	589	51520	83176	547	33240	79820	324	31424	75850	40.8
s38417	99.47	1031	1232412	1355437	2573	227416	281984	2263	174333	269912	1934	127947	213967	14.5
s38584	95.85	704	1014658	1079256	1922	541275	574792	1348	470685	557567	973	302689	381214	27.8
Ave.	97.47	498	572423	636786	1438	140562	166235	901	119227	160139	735	79245	117548	18.1

Table 2 Comparison results of test power reduction with previous works.

Circuit	Power reduction compared to MT-fill				Power reduction compared to R-fill			Power reduction compared to 0-fill			
	Test smoothing [1]		Proposed MTR-fill		SB-Filling [2]	Proposed MTR-fill		MTC-Filling [3]		Proposed MTR-fill	
	P_{ave} redu. (%)	P_{peak} redu. (%)	P_{ave} redu. (%)	P_{peak} redu. (%)	P_{peak} redu. (%)	P_{ave} redu. (%)	P_{peak} redu. (%)	P_{ave} redu. (%)	P_{peak} redu. (%)	P_{ave} redu. (%)	P_{peak} redu. (%)
s5378	12.9	23.8	10.0	6.7	74.2	78.6	69.6	18.07	2.92	28.4	19.7
s9234	11.8	13.7	32.3	27.3	43.8	67.6	60.8	40.31	8.46	36.6	24.6
s13207	17.6	42.4	39.3	28.1	85.3	74.1	64.0	34.46	13.85	41.6	32.8
s15850	20.3	58.3	46.4	31.8	NA	78.9	65.2	30.01	15.99	48.6	33.2
s35932	16.7	21.6	5.5	5.0	NA	97.7	95.2	NA	NA	39.0	8.8
s38417	13.5	38.4	26.6	20.7	52.5	89.6	84.2	39.39	14.93	43.7	24.1
s38584	14.5	15.6	35.7	31.6	NA	70.2	64.7	35.39	9.29	44.1	33.7
Ave.	15.3	30.6	28.0	21.6	63.95	79.5	72.0	32.94	10.91	40.3	25.3

the scan-load power reduction. However, the test power reduction of the proposed MTR-fill technique includes both the scan-load power reduction and the scan-unload power reduction. The proposed method has achieved an average reduction of 28% in P_{ave} and 21.6% in P_{peak} compared with the MT-fill technique. As shown in Table 2, the MTR-fill of the X-values leads to a more significant savings in average and peak power dissipation than in previous work.

5. Conclusions

In this paper, a new X-filling technique, called MTR-fill, is proposed in order to address the problem of excessive power dissipation during scan testing. During the simulated annealing process, the MTR-fill reduces the number of signal transitions in a scan-load test pattern and a scan-unload test response simultaneously by appropriately assigning X-values to 0's or 1's. Simultaneously, the proposed MTR-fill attempts to increase the randomness of the test pattern by flipping the current logic value of a randomly selected bit to reduce the number of test patterns needed to achieve adequate fault coverage. Experimental results show that lower test power dissipation and a small number of test patterns are required compared with those needed for the MT-fill method. The proposed MTR-fill method offers a feasible solution to the power dissipation problem by reducing the test application time in scan-based logic testing.

References

[1] T. Hayashi, N. Ikeda, T. Shinogi, H. Takase, and H. Kita, "Low power oriented test modification and compression techniques for scan based core testing," IEEE Proc. Asian Test Symposium, pp.327–332, 2006.

[2] N. Badereddine, P. Girard, S. Pravossoudovitch, C. Landrault, A. Virazel, and H.J. Wonderlich, "Minimizing peak power consumption during scan testing: Structural technique for don't care bits assignment," IEEE Proc. Research in Microelectronics and Electronics, Ph. D., pp.65–68, 2006.

[3] J. Song, H. Yi, D. Hwang, and S. Park, "A compression improvement technique for low-power scan test data," IEEE Proc. TENCON, pp.1–4, 2006.

[4] K.M. Butler, J. Saxena, T. Fryars, G. Hetheringon, A. Jain, and J. Lewis, "Minimizing power consumption in scan testing: Pattern generation and DFT techniques," IEEE Proc. Int. Test Conf., pp.355–364, 2004.