# A BiCMOS Dynamic Multiplier Using Wallace Tree Reduction Architecture and 1.5V Full-swing BiCMOS Dynamic Logic Circuit

J.B. Kuo, K.W. Su, and J.H. Lou
Rm. 338, Dept. of Electrical Eng., National Taiwan University
Roosevelt Rd., Sec. 4, Taipei, Taiwan 106-17

## Abstract

*This paper presents a BiCMOS dynamic multiplier, which is free from race and charge sharing problems, using Wallace tree reduction architecture and 1.5V full-swing BiCMOS dynamic logic circuit. Based on a 1μm BiCMOS technology, a 1.5V 8x8 multiplier designed, shows a 2.3x improvement in speed as compared to the CMOS static one.*

## Introduction

High-speed multipliers are usually realized by parallel architectures [1], where Wallace reduction structure [1][2] and carry look ahead circuit have been used to enhance the speed performance. In a high-speed parallel multiplier using Wallace tree reduction structure, the most important building cells are the full adder circuit and the carry look-ahead circuit. Although CMOS dynamic technique [2][3] can provide a speed advantage over the static one for implementing serial adders, it's not suitable for realizing the full adder circuit for parallel multipliers using Wallace tree reduction structure due to race problems [3]. Currently, BiCMOS static logic circuits have been proved to be helpful for realizing high-speed VLSI systems [4]. In fact, BiCMOS dynamic logic circuits can also be very helpful for implementing high-speed digital systems. Recently, a BiCMOS dynamic carry look ahead circuit, which is built by cascading BiCMOS dynamic logic gates without race problems, has been reported [5]-[8]. However, it's for 5V operation. For advanced BiCMOS technologies, scaling power supplies is unavoidable [9][10]. For a deep sub-half-micron BiCMOS technology, a 1.5V supply is necessary. Recently, a 1.5V BiCMOS static logic circuit [11] has been reported. In this paper, a 1.5V BiCMOS dynamic multiplier using Wallace tree reduction techniques and 1.5V full-swing BiCMOS dynamic logic circuit without race and charge sharing problems is described. In the following sections, the BiCMOS dynamic full adder circuit and carry look-ahead circuit based on the 1.5V full-swing BiCMOS dynamic logic circuit techniques is described first, followed by the 8x8 multiplier circuit, and discussion.

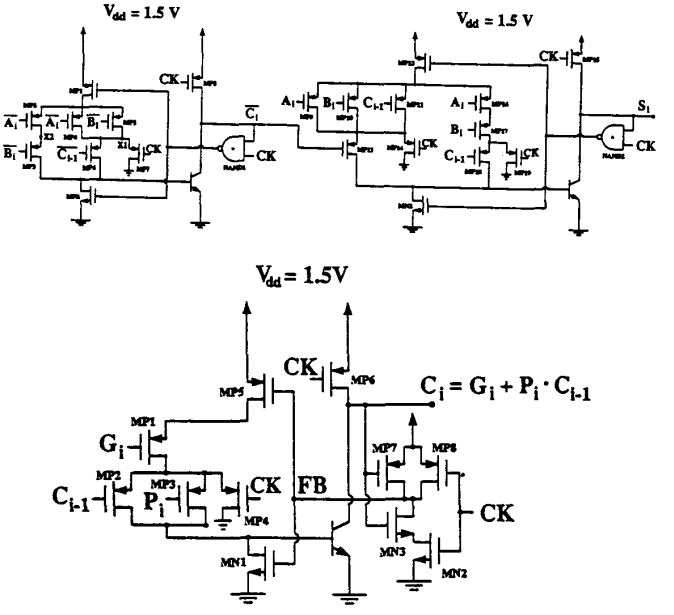


Figure 1: (a) The 1.5V full-swing BiCMOS dynamic full adder circuit. (b) The 1.5V full-swing BiCMOS dynamic carry look-ahead circuit.

## The 1.5V BiCMOS Dynamic Full-Adder and CLA Circuit

Figs. 1(a)&(b) show the 1.5V BiCMOS dynamic full adder and CLA circuit. As shown in Fig. 1(b), the BiCMOS dynamic full adder circuit is composed

of cascading two non-inverting BiCMOS dynamic logic cells [12] for 1.5V operation. The first BiCMOS dynamic logic cell is used to implement the $\overline{carry}$ signal (carry=AB+BC+AC) and the second cell is used to realize the sum signal (sum=$\overline{carry}$(A+B+C)+ABC). As in a dynamic BiCMOS digital circuit [12], during the precharge period, the clock signal (CK) is low and the outputs of two cells are charged to high and the bipolar devices are turned off by MN1 and MN2, which are controlled by CMOS NAND1 and NAND2. In addition, MP1 and MP2 are off at this time. During the logic evaluation period, the clock signal (CK) is high. During the initial period of the logic evaluation period, MP1 and MP12 are on and MN1 and MN2 are off. If at least any two of the three ($\overline{A_i}$, $\overline{B_i}$, $\overline{C_i}$) inputs are low, the $\overline{carry}$ signal is pulled low by the pull-down bipolar transistor. Then, the sum signal will be pulled down only when all of the three signals $A_i$, $B_i$, $C_i$ are low or when the $\overline{carry}$ signal is low and at least one of the three signals $A_i$, $B_i$, $C_i$ is low. Using the non-inverting BiCMOS logic circuits, the full adder can be used in the high-speed parallel multiplier with Wallace reduction structure without race problems. Furthermore, in order to avoid charge sharing problems [13], MP7, MP14, MP19 have been used.

In a dynamic logic circuit, charge sharing [13] can be a serious problem. Consdier the first logic circuit ($\overline{C_i}$) in the following situation. In a period, $\overline{A_i}$ and $\overline{B_i}$ are low and $\overline{C_{i-1}}$ is high. During this period, the voltage at node $X1$ is pulled high to $1.5V$ and the bipolar device is off since the base is pulled down to ground. In the second period, $\overline{A_i}$ and $\overline{B_i}$ switch from low to high and $\overline{C_{i-1}}$ turns low. During this period, the bipolar device is supposed to maintain the off condition. However, due to the parasitic capacitance at node $X1$, the base voltage may not be $0V$ any more. This is called charge sharing, which is often a problem when the cascoding input path is long. Here, using MP7 to set the voltage at $X1$ to $0.7V$ during each period, charge sharing has been avoided. In the full adder circuit, only the nodes with a large parasitic capacitance are equipped with the "charge-sharing prevention" transistors – MP7, MP14, and MP19. In nodes with a small parasitic capacitance, for example at node $X2$, it's not necessary.

Fig. 1(b) shows the BiCMOS dynamic carry look-ahead circuit. The function of the carry look-ahead circuit is:

$$C_i = G_i + C_{i-1} \cdot P_i, \quad for \quad i = 1 \sim n$$

where $n$ is the bit number. $G_i$ and $P_i$ are the generate and propagate signals ($G_i = X_i \cdot Y_i$, $P_i = X_i \oplus Y_i$) produced from two inputs ($X_i, Y_i$) to the half adder. In the carry look-ahead circuit, each bit *carry* signal ($C_i$) is high if the generate signal ($G_i$) is high or if the propagate signal ($P_i$) is high and the *carry* signal of the previous bit ($C_{i-1}$) is high.

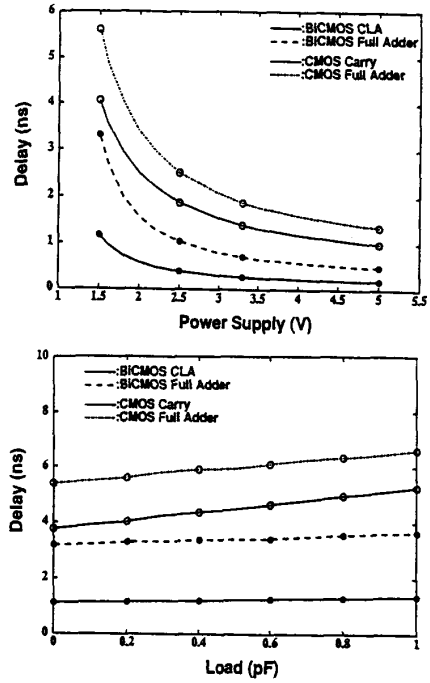


Figure 2: Propagation delay of the full adder and the carry look-ahead using the 1.5V full-swing BiCMOS dynamic logic circuit technique vs. (a) the supply voltage. (b) load.

Fig. 2(a) shows the propagation delay vs. the power supply voltage of the full adder circuit and the carry look-ahead circuit using the BiCMOS dynamic and CMOS static techniques. The design is based on a $1\mu m$ BiCMOS technology, where it has a gate oxide thickness of $180\mathring{A}$, a threshold voltage of $\pm 0.7V$ and a bipolar device with a unity gain frequency of $8GHz$. The aspect ratios of all NMOS and PMOS devices used are $36\mu m/1\mu m$ and $64\mu m/1\mu m$, respectively. In the study, an output load of $0.2pf$ has been assumed. For a power supply voltage of $5V$, the speed advantage of the CLA and the full-adder using BiCMOS dynamic circuit is 5.3x and 2.8x, respectively. For a power supply voltage of $1.5V$, the speed advantage of the CLA and the full-adder using BiCMOS is 3.5x and 1.7x, respectively. Fig. 2(b) shows the propagation delay vs. the load of the full adder circuit and the carry look-ahead circuit using the BiCMOS dynamic and

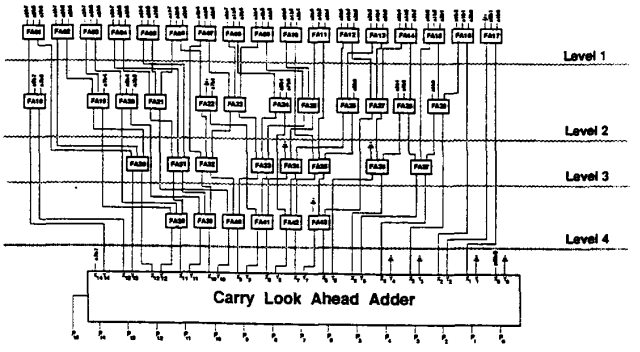


Figure 3: Block diagram of the 8x8 parallel multiplier using Wallace tree reduction architecture with 1.5V BiCMOS dynamic full adders and carry look ahead circuit.

CMOS static techniques. As shown in Fig. 1(b), the propagation delay of the BiCMOS dynamic circuits is less sensitive to the load. The consistent higher speed advantage of the BiCMOS dynamic full adder is very important for realizing parallel multipliers using Wallace tree reduction architecture.

## The BiCMOS Dynamic Multiplier

High-speed parallel multipliers with Wallace tree reduction structure have been realized by CMOS static circuits [2] but they suffer from the speed penalty as a result of complex routing, long wiring, irregular layout of the architecture [2]. Due to race problems, CMOS dynamic circuits are not suitable for building high-speed parallel multipliers with Wallace tree reduction structure. In fact, the BiCMOS dynamic circuits are appropriate for implementing Wallace tree reduction architecture with complicated wiring. In order to show the versatilities of the BiCMOS dynamic full adder circuit for constructing parallel multipliers with Wallace tree reduction structure, an 8x8 parallel multipliers as shown in Fig. 3 has been designed. Fig. 4 shows the layout of the BiCMOS dynamic 8x8 parallel multipliers using Wallace tree reduction architecture. The die area is $3144\mu m \times 1455\mu m$. A large portion of the space is allocated for the complex routing, long wiring and irregular layout for realizing the Wallace tree reduction architecture.

Fig. 5 shows the transient waveforms at $P_{15}$ and $X_6$ of the critical path via FA12, FA26, FA35, FA43, and the CLA as shown in Fig. 3. As shown in the figure, a full swing of 1.5V has been obtained. Note that as the

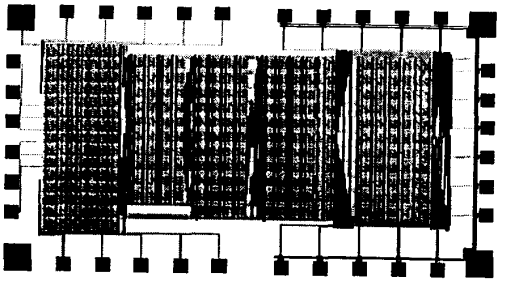

Figure 4: Layout of the BiCMOS dynamic 8x8 parallel multipliers using Wallace tree reduction architecture. The die area is $3144\mu m \times 1455\mu m$

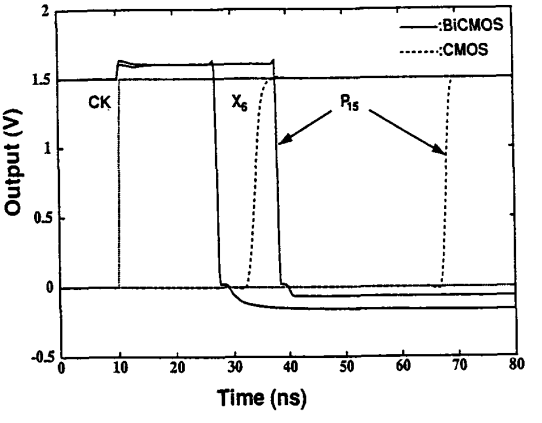


Figure 5: Transient waveform at $P_{15}$ and $X_6$ of the critical path via FA12, FA26, FA35, FA43, and the CLA.

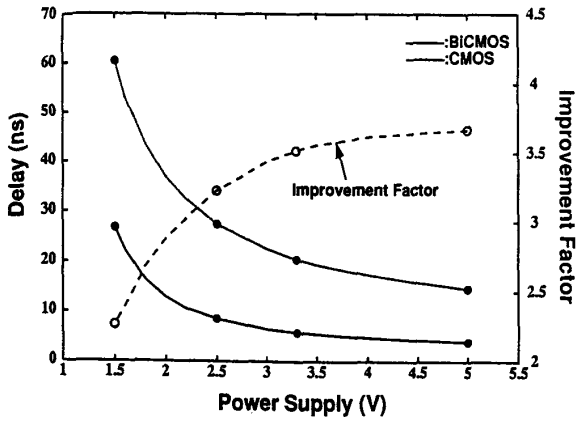


Figure 6: Propagation delay of the critical path vs. the supply voltage in the 8x8 parallel multiplier using Wallace tree reduction architecture and the 1.5V full-swing BiCMOS dynamic logic circuit.

CK signal turns high, the node voltage exceeds 1.5V, which is due to the clock feedthrough over the $C_{gd}$ of the precharge PMOS devices. In addition, the node voltage may go below 0V, which is the result of the effect of the $C_{bc}$ of the bipolar device.

Fig. 6 shows the propagation delay of the critical path vs. the supply voltage in the 8x8 parallel multiplier using Wallace tree reduction architecture and the 1.5V full-swing BiCMOS dynamic logic circuit. As shown in this figure, at a power supply voltage of $5V$, the speed advantage of the BiCMOS dynamic multiplier is 3.67x. At a supply of $1.5V$, the speed advantage is 2.26x.

## Conclusion

This paper presents a BiCMOS dynamic multiplier, which is free from race and charge sharing problems, using Wallace tree reduction architecture and 1.5V full-swing BiCMOS dynamic logic circuit. A 1.5V 8x8 multiplier, which is designed based on a $1\mu m$ BiCMOS technology, shows a 2.3x improvement in speed as compared to the CMOS static one.

## References

[1] S. Waser et. al., "Introduction to Arithmetic for Digital Systems Designers," HRW 1982

[2] [2] D. G. Crawley, G. A. J. Amaratunga, "8x8 bit Pipelined Dadda Multiplier in CMOS," *IEE Proc. G*, No. 6, pp. 231-240, Dec. 1988

[3] N. F. Goncalves and H. J. DeMan, "NORA:A Racefree Dynamic CMOS Technique for Pipeline Logic Structures," *IEEE Journal Solid State Circuits*, Vol. SC-18, No3, pp.261-266, June 1983

[4] M. Kubo, I. Masuda, K. Miyata, and K. Ogiue, "Perspective on BiCMOS VLSI's," *IEEE J. Solid State Circuits*, Vol. 23, No. 1, pp.5-11, Feb. 1988

[5] J. B. Kuo, H. J. Liao, and H. P. Chen, "BiCMOS Dynamic Manchester Carry Look Ahead Circuit for High Speed Arithmetic Unit VLSI," *Electronics Letters*, pp.476, Vol. 28, No. 5, 1992

[6] [6] H. P. Chen, H. J. Liao, and J. B. Kuo, "BiCMOS Dynamic Full Adder Circuit for High-Speed Parallel Multipliers," *Electronics Letters*, Vol. 28, No. 12, pp. 1124-1126, June 1992

[7] J. B. Kuo, H. J. Liao, and H. P. Chen, "A BiCMOS Dynamic Carry Look Ahead Circuit with Carry Skip for High Speed CPU VLSI," *IEEE Trans. Circuits and Systems*, Dec. 1992

[8] J. B. Kuo, H. J. Liao, and H. P. Chen, "A BiCMOS Dynamic Carry Look-Ahead Adder Circuit for VLSI Implementation of High Speed Arithmetic Unit," *IEEE Journal Solid State Circuits*, pp. 375-378, March 1993

[9] D. L. Harame, E. F. Crabbe, J. D. Cressler, J. H. Comfort, J. Y. C. Sunj, "A High Performance Epitaxial SiGe-Base ECL BiCMOS Technology," *Digest of IEDM*, pp. 19-22, 1992

[10] T. M. Liu, G. M. Chin, D. Y. Jeon, M. D. Morris, V. D. Archer, H. H. Kim, M. Cerullo, K. F. Lee, J. M. Sung, T. Y. Chiu, A. M. Voshchenkov, and R. G. Swartz, "A Half-Micron Super Self-Aligned BiCMOS Technology for High Speed Applications," *Digest of IEDM*, pp.23-26, 1992

[11] M. Hiraki, K. Yano, M. Minami, K. Sato, N. Matsuzaki, A. Watanabe,T. Nishida, K. Sasaki, and K. Seki, "A 1.5V Full-Swing BiCMOS Logic Circuit," *IEEE J. Solid State Circuits*, Vol. 27, No. 11, pp. 1568-1573, No. 1992

[12] J. B. Kuo, Y. G. Chen, and J. Y. Wang, "A Low-Voltage BiCMOS Dynamic Minimum Circuit using a "BiPMOS Pull-down" Structure for VLSI Implementation of Fuzzy Controllers," *Electronics Letters* , accepted and to be published.

[13] J. A. Pretorius, A. S. Shubat, C. A. T. Salama, "Charge Redistribution and Noise Margins in Domino CMOS Logic," *IEEE Trans. Circuits and Systems*, Vol. 33, No. 8, pp. 786-793, Aug. 1986