

Thorough Testing of Any Multiport Memory With Linear Tests

Said Hamdioui, *Member, IEEE*, and Ad J. van de Goor, *Fellow, IEEE*

Abstract—The quality of tests, in terms of fault coverage and test length, is strongly dependent on the used fault models. This paper presents realistic fault models for multiport memories with p ports, based on defect injection and SPICE simulation. The results show that the fault models for p -port memories consist of p classes: single-port faults, two-port faults, ..., p -port faults. In addition, the paper discusses the test procedure for such memories; it shows that the time complexity of the required tests is not exponential proportionally with p , as published by different authors, but it is linear, irrespective of the number of ports of which the multiport memory consists.

Index Terms—Fault coverage, fault models, multiport/single-port memories, spot defects, weak faults.

I. INTRODUCTION

FAST and efficient testing is an important step in any manufacturing process. The cost of testing such memories increases rapidly with every generation [1]. Precise and realistic fault modeling in order to design efficient tests, while keeping test cost and time within economically acceptable limits, are therefore essential.

A novel characteristic of today's memories is the presence of multiple ports to allow the two common operations (read and/or write) to be performed simultaneously. Testing of such *multiport* (MP) memories requires special tests since the multiple and simultaneous access can sensitize faults that are different from the conventional *single-port* (SP) memory faults.

In spite of the growing use of MP memories, little *experimental* work has been published. In [2], an *ad hoc* test with no specific fault model was described. In [3], a built-in-self-test (BIST) circuit, based on a serial interfacing technique for embedded *two-port* (2P) memories, was reported. However, the used fault models were very *simplistic*, and the proposed BIST requires a modification of the design. For the same fault models, modified march tests and BIST circuits were reported in [4]–[6]. In [7]–[10] it has been shown *theoretically* that the conventional tests for SP memories are *insufficient* for MP memories. Moreover, *theoretical* fault models, together with their tests, were developed. However, the introduced fault models are *not* based on any experimental/industrial analysis. In addition, the proposed tests have a time complexity which is exponentially proportional with the number of ports of the MP memory; that makes them

not practical. In [11], port interferences in 2P memories were *experimentally* analyzed, based on an industrial design and SPICE simulation; however, the analysis was restricted to only the interference between the bit lines and the word lines of the two ports. A similar, but theoretical work, has been reported in [12].

It can be seen from the above that little *experimental* research has been done on testing MP memories. Experimental research is required in order to develop *realistic* fault models and, thereafter, *optimal* tests. In this paper, a complete analysis of spot defects in MP memories will be presented, resulting in realistic fault models. The paper is organized as follows. Section II establishes an inventory of all possible spot defects in the memory cell array. Section III gives a description of the simulation model and methodology. Section IV derives the functional fault models based on the simulation results, which will be presented in Section V. Section VI analyzes the probabilities of occurrence of these faults. Section VII discusses the test procedure, while Section VIII ends with conclusions.

II. CLASSIFICATION OF SPOT DEFECTS

Many faults in the memory circuit are caused by undesired particles called *spot defects* (SDs). Depending on their conductivity, they can cause undesired connections or disconnections in the memory. They can be divided into three groups:

- *Open*: an extra resistance within a connection. The resistor value called R_{op} is given by $0 < R_{op} \leq \infty$.
- *Short*: an undesired resistive path between a node and V_{cc} or V_{ss} . The resistor value called R_{sh} is given by $0 \leq R_{sh} < \infty$.
- *Bridge*: an undesired resistive path between two connections, which are not V_{cc} or V_{ss} . The resistor value called R_{br} is given by $0 \leq R_{br} < \infty$.

In this paper, a complete analysis of the above SDs will be done for a differential access p -port (pP) memory cell shown in Fig. 1. In order to do that, all possible SDs in the pP memory cell have to be defined and located.

SDs can occur in any subcircuit of the memory circuit. In this paper, we will restrict ourselves to SDs in the memory cell array. Fig. 2 gives an overview of *memory cell array spot defects* (MCASDs). It should be noted that the discussion of SDs in this section will be done for a memory cell with any number of ports p .

Many SDs can be identified in a pP memory. However, due to the symmetric structure of the cell, only a subset needs to be simulated. For identifying the not-to-be simulated SDs, the following terminology will be introduced:

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The authors are with the Laboratory of Computer Engineering, Delft University of Technology, 2628 CD Delft, The Netherlands (e-mail: said@ce.et.tudelft.nl; vdGoor@carit.et.tudelft.nl).

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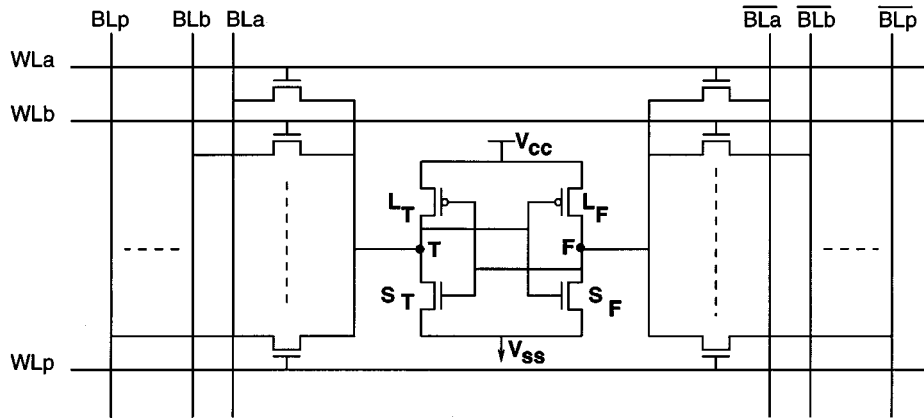
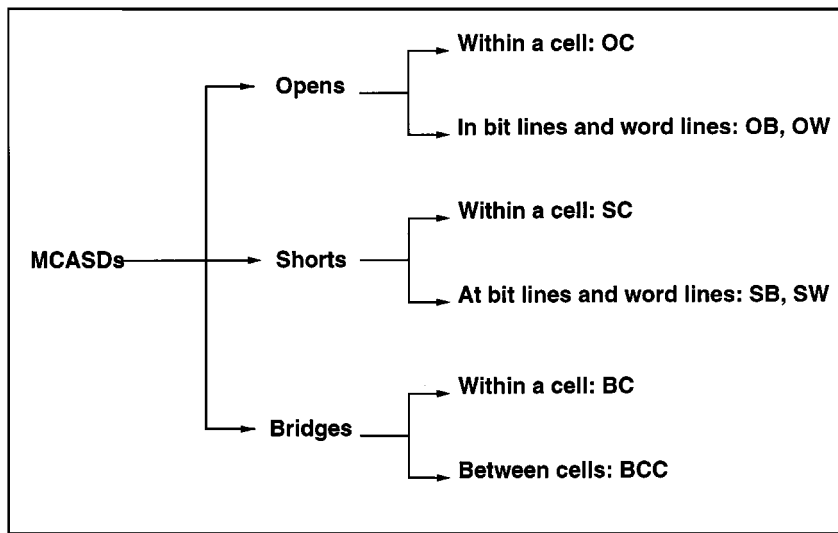
Fig. 1. A differential p -port memory cell.

Fig. 2. Classification of MCASDs.

- *Similar behavior*: A spot defect SD1 (i.e., open, short, or bridge) shows a similar behavior to SD2 if SD1 and SD2 present the same defect, but belong to different ports; e.g., a bridge between bit line BL_a and word line WL_b has a similar behavior to a bridge between bit line BL_b and word line WL_a .
- *Complementary behavior*: SD1 shows a complementary behavior to SD2 if SD1 and SD2 present defects in which locations in the memory cell are symmetrical to each other; e.g., a bridge between the bit lines BL_a and BL_b at the true side has a complementary behavior to a bridge between \overline{BL}_a and \overline{BL}_b at the false side. In this case, the functional fault behavior of SD1 is similar to that of SD2, with the only difference being that all 1s are replaced with 0s and vice versa. E.g., if due to the presence of SD1 the operation read 0 (r0) causes an up transition in the cell, then in the presence of SD2 the r1 operation causes a down transition in the cell.
- An SD1 (involving two cells) shows an **interchanged behavior** to an SD2 (involving the same two cells) if the fault behavior of SD1 is similar to that of SD2, with the only difference being that the *aggressor cell* and the *victim cell* are interchanged; whereby, the victim cell is

the cell where the fault appears, while the aggressor cell is the cell to which the sensitizing operation (state) should be applied.

- *Interchanged complementary behavior*: SD1 shows an interchanged complementary behavior to SD2 if SD1 shows a complementary and interchanged behavior to SD2.

A. Definition and Location of Opens

Opens in the memory cell can be classified as *opens within a cell* (denoted as *OC*) and opens at bit lines (*OB*) and at word lines (*OW*).

1) *Opens Within a Cell*: In this case, the p -port memory cell will be considered without bit lines and word lines to which it is connected. In order to define all possible opens, the cell will be considered as a graph in which all branches can show such a defect. Fig. 3 shows all possible locations of opens within a memory cell. Note that cells that belong to adjacent rows share the same V_{cc} or V_{ss} line and that the opens at such lines are considered as opens within a cell. Opens at locations OC_x and OC_{xc} will show *complementary* fault behaviors due to the symmetric structure of the memory cell, while opens at locations OC_x and OC_{xs} will show *similar* fault behaviors due to the fact

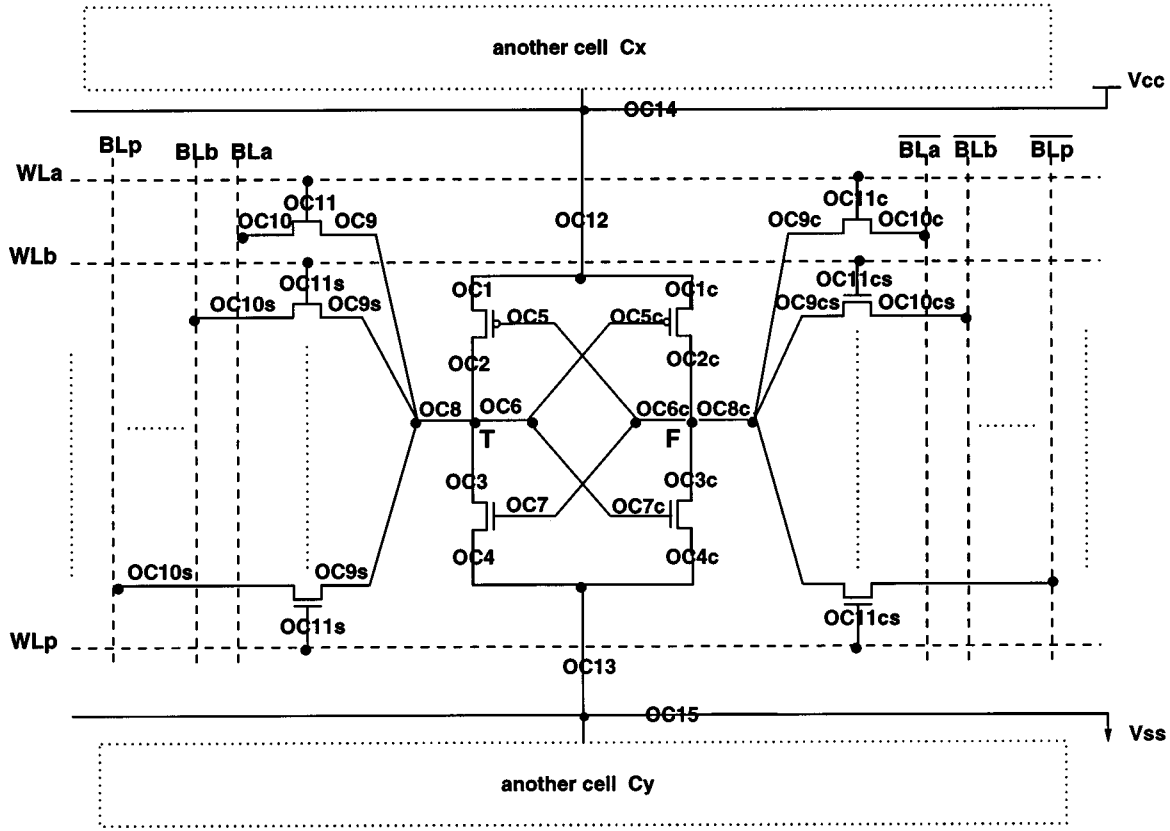


Fig. 3. Opens within a cell.

that the cell has p similar ports. For that reason, one can be limited to simulate opens OC_x only. From these, the behavior of the opens OC_{xc} and OC_{xs} can be derived. The first block of Table I shows the OCs. The first column lists the OC_x opens, which are the minimal set that needs to be simulated, the third column gives the number of opens within one group. A group is a set of defects having a similar and/or a complementary fault behavior (e.g., opens at the source of the pull-up transistor at the true side consist of two opens, $OC1$ and $OC1c$). Note that the total number of opens within a cell (including opens at V_{cc} and opens at V_{ss}) is $20 + 6p$, whereby p is the number of ports; note also that each port will add six possible opens to the list of opens (e.g., $OC9$, $OC10$, $OC11$, $OC9c$, $OC10c$, and $OC11c$).

The fourth column in Table I classifies the opens into *single-port fault defects (SFDs)* and *multiport fault defects (MFDs)*. The SFDs are spot defects that *only* can cause single-port (SP) faults; they *cannot* cause special faults for MP memories. The SP faults are faults that can be sensitized using a single port. The MFDs are defects that can cause SP faults as well as MP faults; such faults require the use of multiple ports simultaneously in order to be sensitized. This classification is based on the simulation results done for a differential two-port (2P) memory [13], [16]; the SDs causing only SP faults in 2P memories are considered SFDs, while SDs causing SP faults as well as two-port faults (i.e., faults requiring the use of two ports simultaneously in order to be sensitized) are considered MFDs. Note that only $OC3$ and $OC4$ from Table I are MFDs. The fact that these two opens are MPDs can be explained as follows: when a single read operation is performed to the

TABLE I
LIST OF OPENS

Open	Description	#	Class
OC1	Source of pull-up at true side	2	SFD
OC2	Drain of pull-up at true side	2	SFD
OC3	Drain of pull-down at true side	2	MFD
OC4	Source of pull-down at true side	2	MFD
OC5	Gate of pull-up at true side	2	SFD
OC6	Cross coupling at true side	2	SFD
OC7	Gate of pull-down at true side	2	SFD
OC8	Connection of the pass transistors	2	SFD
OC9	Pass transistor connection to T	$2p$	SFD
OC10	Pass transistor connection to bit line	$2p$	SFD
OC11	Gate of pass transistor at true side	$2p$	SFD
OC12	V_{cc} path of the cell broken	1	SFD
OC13	V_{ss} path of the cell broken	1	SFD
OC14	V_{cc} path shared by adjacent cells	1	SFD
OC15	V_{ss} path shared by adjacent cells	1	SFD
OB_w	the bit line BL_i at the write side	$2p$	SFD
OB_r	the bit line BL_i at the read side	$2p$	SFD
OW	the word line WL_i	p	SFD

cell, in the presence of $OC3$ (or $OC4$), a resistor divider will be formed by the pass transistor and the pull-down transistor together with $OC3$. If the resistance value of the defect is high enough, the voltage of the cell's node (during a read operation) will increase above the threshold voltage, and consequently the cell will flip. If two (or more) simultaneous read operations are performed, then two voltage dividers will be formed which

have an additive effect on the cell's node. That means that the voltage on the node, in the presence of OC3, depends on the number of simultaneous read operations. Therefore OC3 is an MFD. Note that given the results for a 2P memory, then in order to examine a p -port memory, only the two MFDs (OC3 and OC4) need to be resimulated. This eliminates a lot of simulation work.

2) *Opens at Bit Lines and Word Lines:* Bit lines and word lines are connected to many cells. Therefore, an open at a bit line or a word line can influence the behavior of the operations applied to all these cells. In the following, first opens at bit lines will be discussed and thereafter at word lines.

Opens at Bit Lines: If we consider that the memory cell array is located between the read and the write circuit, then the opens at bit lines can occur in the following locations:

- an open between the cell and the write circuits (denoted as OB_w);
- an open between the cell and the read circuits (denoted as OB_r).

Since there are p pairs of bit lines connected to each cell, $4p$ opens at bit lines can exist; $2p$ opens at the side of the write circuits and $2p$ opens at the side of the read circuits. However, one only needs to simulate two opens (e.g., OB_w and OB_r at BL_i) because the behavior of the other opens (e.g., opens at \overline{BL}_i , BL_j , \overline{BL}_j , etc.) can be derived (i and j denote any two different ports). This is because opens at bit lines belonging to different ports and to the true side (e.g., BL_i and BL_j) have similar behaviors, while opens at the false side (e.g., \overline{BL}_i and \overline{BL}_j) have complementary behaviors to opens at the true side.

Opens at Word Lines: The word lines are only driven by the row decoder. Since the opens at the pass transistor gates have already been defined as opens within a cell, the only remaining opens are those in the common word lines. The influence of such opens is the same for all cells along the word lines. We will define OW as an open at the word line WL_i ; note that the total number of opens at word lines is p and that they all have similar behaviors (e.g., an open at WL_j has a similar behavior to an open at WL_i).

The second block in Table I lists the OBs and the OWs; the minimal set of opens at bit lines and at word lines that has to be simulated consists of three opens while there $5p$ possible opens at bit lines and word lines. Note that all these opens can cause only SP faults and no special faults for MP memories since the fault effects of such defects can only impact the operation applied via the port to which the SD belongs [13], [16]; e.g., an open at the word line of port i (P_i) can only impact the operations performed via P_i .

B. Definition and Location of Shorts

The shorts are classified as *shorts within a cell* (denoted as SC) and *shorts at bit lines* (SB) and at *word lines* (SW). Power shorts (i.e., shorts between V_{cc} and V_{ss}) are excluded, since they do not belong to the class of memory cell array faults; they impact the behavior of the whole circuit.

1) *Shorts Within a Cell:* To define shorts within a cell (SC s), a cell has to be considered as a graph in which all nodes can show a short. The cell is considered without bit lines and word lines.

TABLE II
LIST OF SHORTS

Shorts	Co. behavior	#	Class
SC1 T- V_{cc}	F- V_{cc}	2	SFD
SC2 T- V_{ss}	F- V_{ss}	2	MFD
SB1 BL_i - V_{cc}	\overline{BL}_i - V_{cc}	$2p$	SFD
SB2 BL_i - V_{ss}	\overline{BL}_i - V_{ss}	$2p$	SFD
SW1 WL_i - V_{cc}		p	SFD
SW2 WL_i - V_{ss}		p	SFD

Each short is defined as a pair of nodes in which one node is V_{cc} or V_{ss} . The first block of Table II lists the possible SCs; shorts at F show complementary behaviors to shorts at T; see Fig. 1. Note that the number of shorts within a cell is 4, irrespective of the number of ports p . In addition, and based on the simulation results of 2P memories [13], [16], SC1 can only cause SP faults, while SC2 can cause SP faults as well as special MP faults. Note that in the presence of SC2, a voltage divider will be formed during the read operations; the fault effect is then similar to that of OC3 and OC4.

2) *Shorts at Bit Lines and at Word Lines:* The cells belonging to the same column or the same row are connected to the same bit lines and word lines, respectively. Therefore, shorts at bit lines (SBs) and at word lines (SWs) can affect the behavior of all operations performed to these cells. Shorts at bit line BL_i and at word line WL_i have similar behaviors to shorts at BL_j and at WL_j , respectively; and shorts at \overline{BL}_i have complementary behaviors to short at BL_i , whereby i and j can be any two different ports. The second and the third block of Table II list the possible SBs and SWs; shorts with complementary behavior are grouped together in the same row. The number of shorts within each group is also given in the table. The total number of SBs and SWs for an MP cell with p ports is $6p$; while one needs to simulate only four. Note that all SBs and SWs are SFDs, since the fault effects of such defects can only impact the operation applied via the port to which the SD belongs [13], [16].

C. Definition and Location of Bridges

A bridge in a p -port memory cell array can connect any arbitrary pair of nodes. However, the following assumptions are made: 1) the nodes have to be located close to each other, such that the bridge can occur only within a single cell or between physically adjacent cells, and 2) the defect can involve two nodes *at the most*. These two assumptions are verified, based on the real data found using *inductive fault analysis* (IFA), which shows that the occurrence probability of defects involving more than two nodes is very small (3.4% on the average), since they require that a defect has to be very large [13], [16]. The bridges in the memory cell array can be divided into two groups:

- *Bridges within a cell* (BCs): All bridges connecting two nodes of the same cell, including the p pairs of bit lines and the p word lines to which it is connected.
- *Bridges between cells* (BCCs): All bridges connecting nodes of an adjacent cells, including the bit lines and the word lines to which the cells are connected.

TABLE III
LIST OF BRIDGES WITHIN A CELL (BCs)

Bridge	Comp. behavior	#	Class
BC1 T-F		1	SFD
BC2 T- BL_i	F- BL_i	$2p$	SFD
BC3 T- \overline{BL}_i	F- \overline{BL}_i	$2p$	SFD
BC4 T- WL_i	F- WL_i	$2p$	SFD
BC5 BL_i - \overline{BL}_i		p	SFD
BC6 BL_i - BL_j	\overline{BL}_i - \overline{BL}_j	$p(p-1)$	MFD
BC7 BL_i - \overline{BL}_j		$p(p-1)$	MFD
BC8 BL_i - WL_i	\overline{BL}_i - WL_i	$2p$	SFD
BC9 BL_i - WL_j	\overline{BL}_i - WL_j	$2p(p-1)$	SFD
BC10 WL_i - WL_j		$\frac{p(p-1)}{2}$	SFD

1) *Bridges Within a Cell*: To define all possible bridges within a cell (BCs), the cell has to be considered as a graph in which each node can be connected to another by a bridge. Each p -port cell consists of $3p + 2$ nodes n_i ($n_i \in \{T, F, BL_i, \overline{BL}_i, WL_i\}$): a true and a false node (T, F), $2p$ bit lines (BL_i, \overline{BL}_i), and p word lines (WL_i); whereby i is one of the p ports ($i \in \{a, b, c, \dots, p\}$). Therefore, there are $C_2^{3p+2} = (3p+2)!/(2!(3p)!) = (9p^2 + 9p + 2)/2$ bridges. Table III shows all possible bridges within a cell. Note that bridges with similar or complementary behaviors are grouped together in the same row, such that one can restrict the simulation to only one bridge of each row; e.g., only the first column of the table. The total number of bridges within one group is given in the third column of the table; the class of BCs is also given based on the simulation results for 2P memories [13], [16]. Note that only BC6 and BC7 can cause special faults in MP memories since they involve bit lines belonging to different ports [13], [16].

2) *Bridges Between Cells*: Bridges between cells (BCCs) consist of BCCs in the same row (rBCCs), BCCs in the same column (cBCCs), and BCCs on the same diagonal (dBCCs). To establish all possible BCCs, the configuration shown in Fig. 4 will be considered. It consists of four cells, namely C_1 , C_2 , C_3 , and C_4 . Note that the adjacent cells can belong to the same column, the same row, or to the same diagonal. The cells C_1 and C_3 , as well as the cells C_2 and C_4 , are adjacent in the same row and therefore have common word lines, while the cells C_1 and C_2 (as well as the cells C_3 and C_4) are adjacent in the same column and therefore have common bit lines.

a) *Bridges Between Cells in Same Row*: In order to find all possible bridges between adjacent cells in the same row (rBCCs), only C_1 and C_3 have to be considered; see Fig. 4. Both C_1 and C_3 consist of $2 + 3p$ nodes: C_1 consists of T1, F1, $BL1_i$, $\overline{BL1}_i$, and $WL1_i$, while C_3 consists of T3, F3, $BL2_i$, $\overline{BL2}_i$, and $WL1_i$; $i \in \{a, b, \dots, p\}$. Since both cells have a common word line, only the true or false node (T1, F1) of C_1 and its p pairs of bit lines can form a bridge with the true/false node or with the p pairs of bit lines of C_3 . Therefore, there are $(2 + 2p) * (2 + 2p) = 4p^2 + 8p + 4$ possible bridges, $n_1 - n_2$, between the two cells; whereby, n_1 is a node of C_1 ($n_1 \in \{T1, F1, BL1_i, \overline{BL1}_i\}$) and n_2 is a node of C_3 ($n_2 \in \{T3, F3, BL2_i, \overline{BL2}_i\}$). The first block of Table IV shows all possible rBCCs; ports i and j indicate any two different ports. Bridges with a complementary, an interchanged, or an interchanged complementary (I.C.) behavior are grouped

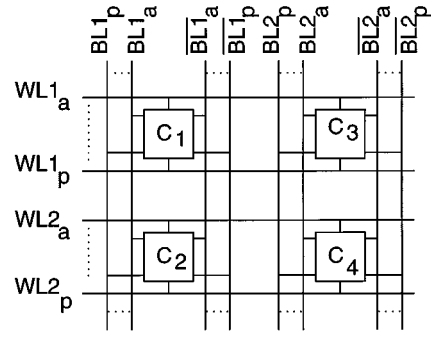


Fig. 4. Four cell configuration.

together in the same row. The total number of bridges within one group is given in the fifth column of the table. Note that the $4p^2 + 8p + 4$ possible bridges are grouped in only eight groups. The class of rBCCs is also given based on the simulation results found for 2P memories [13]. Note that all rBCCs can cause special faults in MP memories.

b) *Bridges Between Cells in Same Column*: In order to find all possible bridges between adjacent cells in the same column (cBCCs), only C_1 and C_2 have to be considered; see Fig. 4. Both C_1 and C_2 consist of $2 + 3p$ nodes: C_1 consists of T1, F1, $BL1_i$, $\overline{BL1}_i$, and $WL1_i$, while C_2 consists of T2, F2, $BL1_i$, $\overline{BL1}_i$, and $WL2_i$; $i \in \{a, b, \dots, p\}$. Note that the two cells share the same bit lines. Therefore, there are $(2 + p) * (2 + p) = p^2 + 4p + 4$ possible bridges, $n_1 - n_2$, between C_1 and C_2 ; whereby, $n_1 \in \{T1, F1, WL1_i\}$ and $n_2 \in \{T2, F2, WL2_i\}$. A bridge between the bit lines and the nodes T2 or F2 is excluded since it belongs to bridges within a cell, which are already considered in Section II-C1. The second block of Table IV lists the $p^2 + 4p + 4$ possible cBCCs; they are grouped into five groups. Note that only three cBCC groups can cause special faults in MP memories.

c) *Bridges Between Diagonal Cells*: The possible bridges between cells belonging to the same diagonal, dBCCs (i.e., C_1 and C_4 of Fig. 4), consist only of four bridges; see the third block of Table IV. All other bridges between the nodes of C_1 and the nodes of C_4 are already considered in rBCCs and cBCCs; this is because C_4 has the same word lines as C_2 and the same bit lines as C_3 .

III. SIMULATION MODEL/METHODOLOGY

In this section, the simulation model as well as the simulation methodology will be discussed.

A. Simulation Model

The SPICE-like circuit simulation environment¹ (CSE) has been used for the simulation. Since CSE requires too much simulation time for a complete memory, an appropriate simulation model has to be built, which will both accurately describe the behavior of the memory while requiring only a reasonable simulation time. The accuracy of the simulation model determines the accuracy of the results, which implies that the model has to approximate the actual memory structure as close as possible.

The simulation model consists of a 2×2 memory cell array; each port can be accessed using the p ports of the memory. In

¹Intel internal electrical circuit simulator

TABLE IV
LIST OF BRIDGES BETWEEN ADJACENT CELLS (BCCs)

Bridge BCC	Complementary behavior	Interchanged beh.	I.C. behavior	# of bridges	Class
rBCC1 T1-T3	F1-F3			2	MFD
rBCC2 T1-F3	F1-F3			2	MFD
rBCC3 T1- $BL2_i$	F1- $BL2_i$	$BL1_i$ -T3	$BL1_i$ -F3	$4p$	MFD
rBCC4 T1- $BL2_i$	F1- $BL2_i$	$BL1_i$ -T3	$BL1_i$ -F3	$4p$	MFD
rBCC5 $BL1_i - BL2_i$	$BL1_i - BL2_i$			$2p$	MFD
rBCC6 $BL1_i - BL2_j$	$BL1_i - BL2_j$			$2p(p-1)$	MFD
rBCC7 $BL1_i - BL2_i$	$BL1_i - BL2_i$			$2p$	MFD
rBCC8 $BL1_i - BL2_j$		$BL1_i - BL2_j$		$2p(p-1)$	MFD
cBCC1 T1-T2	F1-F2			2	MFD
cBCC2 T1-F2	F1-T2			2	MFD
cBCC3 T1- $WL2_i$	F1- $WL2_i$	T2- $WL1_i$	F2- $WL1_i$	$4p$	MFD
cBCC4 $WL1_i$ - $WL2_i$				p	SFD
cBCC5 $WL1_i$ - $WL2_j$				$p(p-1)$	SFD
dBCC1 T1-T4		F1-F4		2	MFD
dBCC2 T1-F4		F1-T4		2	MFD

addition, all cells of the memory cell array sharing the same bit lines or the same word lines (with the 2×2 model) are added to the simulation model such that their loading can be taken into account. The model also contains p duplicated read and write circuits (i.e., precharge circuits, write drivers, sense amplifiers, etc). Moreover, the model also includes the resistance of the interconnections as well as the coupling between the adjacent cells. The model has been built for a differential 2P memory as well as for differential three-port (3P) memory, using Intel real designs.

B. Simulation Methodology

The simulation methodology has to examine all allowed operations in the to be simulated p P memory, for all opens, shorts, and bridges, by examining the resistance range for each SD from 0Ω to $\infty \Omega$.

For a 2P memory, the methodology has to verify in addition to SP operations (i.e., read and write), all allowed 2P operation in the considered 2P memory design; they consist of the following.

- Two simultaneous read operations to the same location, as well as to different locations.
- Two simultaneous write operations to different locations.
- Simultaneous read and write to different locations.
- Simultaneous read and write to the same location. However, in that case the read data will be discarded; i.e., the write operation has a high priority.

For the 3P memory, the methodology has to verify all SP operations, all allowed 2P operations (which are the same as above), as well as all allowed 3P operations. The latter consists of the following simultaneous operations.

- Three operations (read and/or write) to different locations.
- Three read operations to the same and/or different location(s).
- Three write operations to different locations.
- Two reads to the same location and a write to another location.
- Two reads and write to the same location. However, in that case the read data will be discarded; i.e., the write operation has a high priority.

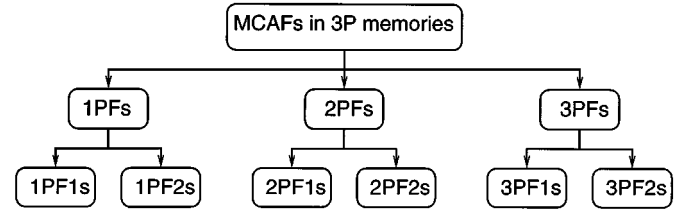


Fig. 5. Classification of MCAFs in 3P memories.

IV. FUNCTIONAL FAULT MODELS

The simulation has been done for all opens, shorts, and bridges by examining the resistance range from 0Ω to $\infty \Omega$, for a 2P SRAM design as well as for a 3P SRAM design [13], [16]. Each faulty behavior is reported in terms of a *fault primitive (FP)*; i.e., a compact notation describing the faulty behavior. It should be noted that after the simulation has been done for 2P SRAMs, the simulation has been redone only for MFDs (i.e., SD causing 1PFs as well as 2PFs) for the 3P SRAM design. Some simulation results will be given in Section V.

In order to design memory tests for detecting faults, the electrical faults caused by the SDs (expressed in terms of FPs) have to be translated into *functional fault models (FFMs)*; whereby, an FFM is defined as a nonempty set of FPs. For example, a stuck-at fault (SAF) is an FFM, while the MATS+ [17] test has been designed to detect SAFs. The FFM for 2P SRAMs, which can be considered as a subset of the FFM for 3P SRAMs, are described in [13] and [14]. In this section, first the FFM for a differential 3P SRAM will be presented, based on the simulation results; thereafter, the results will be extended for any MP memory with p ports.

A. FFM for 3P Memories

Based on the number of ports required in order to sensitize the faults, FFM for memory cell array faults (MCAFs) in 3P memories can be classified into *single-port faults (1PFs)*, *two-port faults (2PFs)*, and *three-port faults (3PFs)*; see Fig. 5. The 1PFs are faults that can be sensitized using SP operations. They are divided into 1PFs involving a single cell (1PF1s) and 1PFs involving two cells (1PF2s). The 2PFs are faults that cannot be

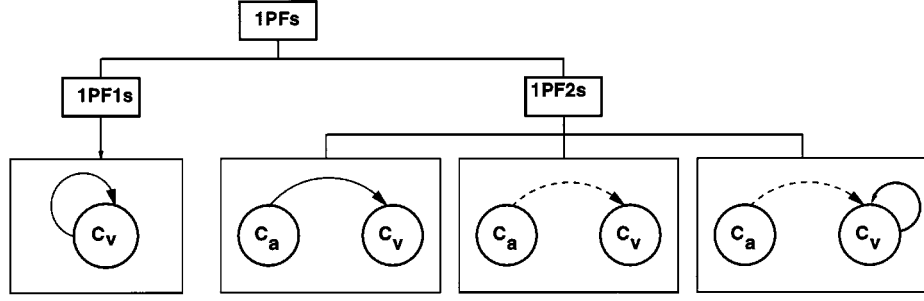


Fig. 6. Classification of 1PFs.

sensitized using SP operations; they require the use of the two ports of the memory simultaneously and are also divided into 2PFs involving a single cell (2PF1s) and 2PFs involving two cells (2PF2s). On the other hand, 3PFs are faults that cannot be sensitized using SP operations or 2P operations; they require the use of the three ports of the memory simultaneously. The 3PFs can be also divided into 3PFs involving a single cell (3PF1s) and 3PFs involving two cells (3PF2s). In the following the three classes will be discussed in detail.

1) *Single-Port Faults* : 1PFs are divided into faults involving a *single-cell* (1PF1s) and faults involving *two-cells* (1PF2s); see Fig. 6. The 1PF1s consist of single-cell FPs; they have the property that the cell used for sensitizing the fault is the same cell as where the fault appears. The 1PF2s have the property: (a) the application of a single-port operation (solid arrow in Fig. 6) to the *aggressor cell* (c_a), (b) the state of the cell c_a (dashed arrow in the figure), or (c) the application of a single-port operation to the *victim cell* (c_v) with cell c_a in certain state, has as a consequence that a fault will be sensitized in the cell c_v .

To denote the 1PFs faults, the following precise compact notation referred as a *fault primitive* (FP), which will prevent ambiguities and misunderstandings, will be used.

- $\langle S/F/R \rangle$ (or $\langle S/F/R \rangle_v$): denotes an FP involving a single-cell (a 1PF1); the cell c_v (victim cell) used to sensitize a fault is the same as where the fault appears. S describes the value/operation sensitizing the fault; $S \in \{0, 1, w0, w1, w \uparrow, w \downarrow, r0, r1, \forall\}$, whereby 0 (1) denotes a zero (one) value, $w0$ ($w1$) denotes a write 0 (1) operation, $w \uparrow$ ($w \downarrow$) denotes an up (down) transition write operation, $r0$ ($r1$) denotes a read 0 (1) operation, and \forall denotes any operation ($\forall \in \{0, 1, w1, w0, w \uparrow, w \downarrow, r1, r0\}$). If the fault effect of S appears after a time T , then the sensitizing operation is given as S_T . F describes the value of the *faulty cell* (v-cell); $F \in \{0, 1, \uparrow, \downarrow, ?\}$, whereby \uparrow (\downarrow) denotes an up (down) transition, and $?$ denotes an undefined state of the cell (e.g., the true and the false node of the cell have the same voltage). R describes the logical value which appears at the output of the SRAM if the sensitizing operation applied to the v-cell is a *read* operation: $R \in \{0, 1, ?, -\}$, whereby $?$ denotes an undefined or random logical value. An undefined logical value can occur if the voltage difference between the bit lines (used by the sense amplifier) is very small. A '-' in R means that the output data is not applicable; e.g., if $S = w0$,

TABLE V
LIST OF 1PF1s; $x \in \{0, 1\}$

FFM	Fault primitives
SAF	$\langle \forall/0/- \rangle, \langle \forall/1/- \rangle$
TF	$\langle w \uparrow/0/- \rangle, \langle w \downarrow/1/- \rangle$
RDF	$\langle r0/\uparrow/1 \rangle, \langle r1/\downarrow/0 \rangle$
DRDF	$\langle r0/\uparrow/0 \rangle, \langle r1/\downarrow/1 \rangle$
IRF	$\langle r0/0/1 \rangle, \langle r1/1/0 \rangle$
RRF	$\langle r0/0/? \rangle, \langle r1/1/? \rangle$
DRF	$\langle 1_T/\downarrow/- \rangle, \langle 0_T/\uparrow/- \rangle, \langle x_T/?/- \rangle$
NAF	$\langle w \uparrow/0/- \rangle, \langle w \downarrow/1/- \rangle, \langle rx/x/? \rangle$
USF	$\langle wx/?/- \rangle, \langle rx/?/? \rangle$

then no data will appear at the memory output, and for that reason R is replaced by a '-'.

- $\langle S_a; S_v/F/R \rangle$ (or $\langle S_a; S_v/F/R \rangle_{a,v}$): denotes an FP involving two cells (a 1PF2); S_a describes the sensitizing operation or state of the *aggressor cell* (a-cell); while S_v describes the sensitizing operation or state of the *victim cell* (v-cell). The a-cell (c_a) is the cell sensitizing a fault in an other cell called the v-cell (c_v). The set S_i is defined as: $S_i \in \{0, 1, w1, w0, w \uparrow, w \downarrow, r1, r0\}$ ($i \in \{a, v\}$).

The 1PF1 Fault Subclass: The 1PF1 faults are FFM's consisting of single-port, single-cell FPs. They consist of nine FFM's [13], [15]; see Table V. The first column gives the abbreviation of the FFM, while the second column shows the FPs the FFM consists of (see also the sixth column of Table IX which shows the FFM to which each FP, sensitized in the presence of a certain defect, belongs):

- 1) *Stuck-at fault* (SAF): the logic value of a cell is always '0' or '1'. The SAF consists of two FPs: $\langle \forall/0/- \rangle$, and $\langle \forall/1/- \rangle$; see Table V;
- 2) *Transition fault* (TF);
- 3) *Read destructive fault* (RDF) [20];
- 4) *Deceptive read destructive fault* (DRDF) [20];
- 5) *Incorrect read fault* (IRF);
- 6) *Random read fault* (RRF);
- 7) *Data retention fault* (DRF) [21];
- 8) *No access fault* (NAF);
- 9) *Undefined state fault* (USF).

The 1PF2 Fault Subclass: The 1PF2 faults are FFM's consisting of single-port FPs, which involve two cells. They consist of seven FFM's [13], [15]; see Table VI.

TABLE VI
LIST OF 1PF2S; $x \in \{0, 1\}$

FFM	Fault primitives
CF_{ds}	$\langle wx; 0/\uparrow/- \rangle$, $\langle wx; 1/\downarrow/- \rangle$, $\langle rx; 0/\uparrow/- \rangle$, $\langle rx; 1/\downarrow/- \rangle$
CF_{st}	$\langle 1; 1/0/- \rangle$, $\langle 1; 0/1/- \rangle$, $\langle 0; 1/0/- \rangle$, $\langle 0; 0/1/- \rangle$
CF_{ir}	$\langle 0; r0/0/1 \rangle$, $\langle 0; r1/1/0 \rangle$, $\langle 1; r0/0/1 \rangle$, $\langle 1; r1/1/0 \rangle$
CF_{rr}	$\langle 0; r0/0/? \rangle$, $\langle 0; r1/1/? \rangle$, $\langle 1; r0/0/? \rangle$, $\langle 1; r1/1/? \rangle$
CF_{dr}	$\langle 0; r0/\uparrow/0 \rangle$, $\langle 0; r1/\downarrow/1 \rangle$, $\langle 1; r0/\uparrow/0 \rangle$, $\langle 1; r1/\downarrow/1 \rangle$
CF_{rd}	$\langle 0; r0/\uparrow/1 \rangle$, $\langle 0; r1/\downarrow/0 \rangle$, $\langle 1; r0/\uparrow/1 \rangle$, $\langle 1; r1/\downarrow/0 \rangle$
CF_{tr}	$\langle 0; w\downarrow/1/- \rangle$, $\langle 0; w\uparrow/0/- \rangle$, $\langle 1; w\downarrow/1/- \rangle$, $\langle 1; w\uparrow/0/- \rangle$

- 1) *Disturb Coupling Fault* (CF_{ds}) [19]: a *disturb coupling fault* is defined as a fault whereby the v-cell undergoes a transition due to a write or a read operation applied to the a-cell. It consists of eight FPs: $\langle wx; 0/\uparrow/- \rangle$, $\langle wx; 1/\downarrow/- \rangle$, $\langle rx; 0/\uparrow/- \rangle$, and $\langle rx; 1/\downarrow/- \rangle$, whereby $x \in \{0, 1\}$.
- 2) *State coupling fault* (CF_{st}) [21].
- 3) *Incorrect read coupling fault* (CF_{ir}).
- 4) *Random read coupling fault* (CF_{rr}).
- 5) *Deceptive read destructive coupling fault* (CF_{dr}).
- 6) *Read destructive coupling fault* (CF_{rd}).
- 7) *Transition coupling fault* (CF_{tr}).

2) *Two-Port Faults (2PFs)*: In order to represent MP faults (e.g., two-port faults), the following terminology will be (re)introduced [7]–[10].

- *Strong fault*: This is a memory fault that can be **fully sensitized** by an operation; e.g., an SP write or read operation fails, two simultaneous read operations fail, etc. That means that the state of the v-cell is incorrectly changed, cannot be changed, or that the sense amplifier(s) return(s) an incorrect result(s).
- *Weak fault*: This is a fault which is **partially sensitized** by an operation; e.g., due to a defect that creates a small disturbance of the voltage of the true node of the cell. However, a fault can be *fully sensitized* (i.e., becomes strong) when two (or more) weak faults are sensitized simultaneously, since their fault effects can be additive. This may occur when a *pP* operation is applied. Note that in the presence of a weak fault, all SP (read and write) operations pass correctly, and that the *pP* operations may pass correctly. The latter will be the case if the fault effects of the weak faults are not sufficient to fully sensitize a fault.

The terminology of weak and strong faults is used in representing the MP faults as follows.

- F denotes a *strong fault* F , while wF denotes the *weak fault* F . For example, RDF denotes a strong read destructive fault, while $wRDF$ denotes a weak read destructive fault.

- $\langle fault_1 \rangle \& \langle fault_2 \rangle \cdots \& \langle fault_p \rangle$: denotes a *pPF* consisting of p weak faults; ' $\&$ ' denotes the fact that the p faults *in parallel* (i.e., simultaneously) form the p PF. E.g., the $wRDF\&wRDF$ denote a 2PFs based on two weak RDFs.

Two-port faults (2PFs) cannot be sensitized using SP operations; they require the use of the two ports simultaneously. The 2PFs can be considered as a combination of *two weak faults*. They can be divided into *faults involving a single cell (2PF1s)* and *faults involving two cells (2PF2s)* [13], [14]; see Fig. 7. A taxonomy of all realistic 2PFs is given also in the same figure.

Table VII shows the FPs of which each 2PF is composed. The FP notation used to describe the 2PF1s and 2PF2s is given as follows.

- $\langle S_1 : S_2/F/R \rangle_v$: denotes a two-port FP involving a single cell (v-cell); a 2PF1. This FP requires the use of the two ports *simultaneously*. S_1 and S_2 describe the sensitizing operations or states of the v-cell; ":" denotes the fact that S_1 and S_2 are applied *simultaneously* via the two ports. F describes the value of the v-cell. Note that the sensitizing operations are applied to the same cell as where the fault appears. R is the read result of S_1 (and/of S_2) if it is a read operation.

For 2PF2s, three notations can be identified, based on the cell(s) to which the two *simultaneous* sensitizing operations are applied, either to the aggressor cell and/or to the victim cell; see Fig. 7.

- $\langle S_a : S_a; S_v/F/R \rangle_{a,v}$ denotes a 2PF2_a: an FP whereby both sensitizing operations, S_a , are applied to the a-cell. S_v denotes the state of the v-cell.
- $\langle S_a; S_v : S_v/F/R \rangle_{a,v}$ denotes a 2PF2_v: an FP whereby both sensitizing operations, S_v , are applied to the v-cell. S_a describes the state of the a-cell.
- $\langle S_a : S_v/F/R \rangle_{a,v}$ denotes a 2PF2_{av}: an FP whereby one sensitizing operation, S_a , is applied to the a-cell, and the other sensitizing operation, S_v , is applied to the v-cell.

In the above notations, F denotes the value of the faulty cell c_v , and R denotes the value which appears at the memory output if S_v is a read operation. The above notation can be extended to describe any *p*-port fault (*pPF*); e.g., $\langle S_a : S_a : S_a; S_v/F/R \rangle_{a,v}$ denotes a FP whereby three simultaneous sensitizing operations, S_a , are applied to the a-cell; while S_v denotes the state of the v-cell; etc.

The 2PF1 Fault Subclass: The 2PF1s are based on a combination of *two single-cell weak faults*. In addition, the two a-cells are the same as the v-cell; see Fig. 7. In order to sensitize a 2PF1, the same cell has to be acted upon simultaneously via the two ports. The 2PF1 consists of three FFM [13], [14], and are listed together with their FPs in Table VII (see also the sixth column of Table IX).

- $wDRDF\&wDRDF$: Applying two simultaneous read operations to a single cell causes the cell to flip, while the sense amplifiers return the *correct* values.
- $wRDF\&wRDF$: Applying two simultaneous read operations to a single cell causes the cell to flip and the sense amplifiers return *incorrect* values.

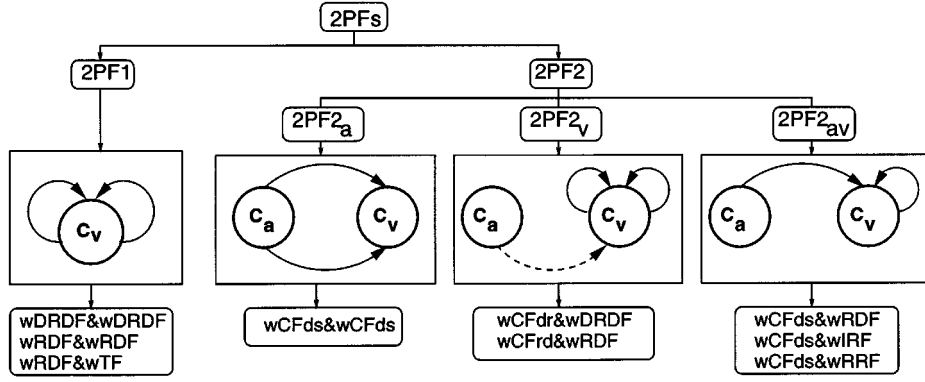


Fig. 7. Classification and taxonomy of 2PFs.

TABLE VII
LIST OF 2PFs; $x \in \{0, 1\}$ AND $d = \text{Don't Care}$

FFM	Fault primitives
wDRDF&wDRDF	$\langle r0 : r0 / \uparrow / 0 \rangle, \langle r1 : r1 / \downarrow / 1 \rangle$
wRDF&wRDF	$\langle r0 : r0 / \uparrow / 1 \rangle, \langle r1 : r1 / \downarrow / 0 \rangle$
wRDF&wTF	$\langle r0 : w \uparrow / 0 / - \rangle, \langle r1 : w \downarrow / 1 / - \rangle$
wCF _{ds} &wCF _{ds}	$\langle w0 : rd; 0 / \uparrow / - \rangle, \langle w0 : rd; 1 / \downarrow / - \rangle,$ $\langle w1 : rd; 0 / \uparrow / - \rangle, \langle w1 : rd; 1 / \downarrow / - \rangle,$ $\langle rx : rx; 0 / \uparrow / - \rangle, \langle rx : rx; 1 / \downarrow / - \rangle$
wCF _{dr} &wDRDF	$\langle 0; r0 : r0 / \uparrow / 0 \rangle, \langle 0; r1 : r1 / \downarrow / 1 \rangle,$ $\langle 1; r0 : r0 / \uparrow / 0 \rangle, \langle 1; r1 : r1 / \downarrow / 1 \rangle,$ $\langle 0; r0 : r0 / \uparrow / 1 \rangle, \langle 0; r1 : r1 / \downarrow / 0 \rangle,$ $\langle 1; r0 : r0 / \uparrow / 1 \rangle, \langle 1; r1 : r1 / \downarrow / 0 \rangle$
wCF _{rd} &wRDF	$\langle 0; r0 : r0 / \uparrow / 1 \rangle, \langle 0; r1 : r1 / \downarrow / 0 \rangle,$ $\langle 1; r0 : r0 / \uparrow / 1 \rangle, \langle 1; r1 : r1 / \downarrow / 0 \rangle$
wCF _{ds} &wRDF	$\langle w0 : r0 / \uparrow / 1 \rangle, \langle w0 : r1 / \downarrow / 0 \rangle,$ $\langle w1 : r0 / \uparrow / 1 \rangle, \langle w1 : r1 / \downarrow / 0 \rangle$
wCF _{ds} &wIRF	$\langle w0 : r0 / 0 / 1 \rangle, \langle w0 : r1 / 1 / 0 \rangle,$ $\langle w1 : r0 / 0 / 1 \rangle, \langle w1 : r1 / 1 / 0 \rangle$
wCF _{ds} &wRRF	$\langle w0 : r0 / 0 / ? \rangle, \langle w0 : r1 / 1 / ? \rangle,$ $\langle w1 : r0 / 0 / ? \rangle, \langle w1 : r1 / 1 / ? \rangle$

- *wRDF&wTF*: A cell fails to undergo a write transition if a read operation is applied to the same cell simultaneously.

It should be noted that the wDRDF&wDRDF and wRDF&wRDF can be caused by the following defects, but with different resistance values of the defect [13], [16]: (a) drain/source of the pull-down transistor of the cell broken (OC3, OC4), (b) true or false node shorted to V_{ss} (SC2), and (c) short between a cell's node and a word line of an adjacent cell (cBCC3). The wRDF & wTF can be caused by bridges between bit lines belonging to the same column, to different ports and to different sides (i.e., true side and false side) of the cell.

The 2PF2 Fault Subclass: The 2PF2s are based on a combination of weak single-cell faults and weak faults involving two cells. Depending on to which cells the two simultaneous operations are applied (to the a-cell and/or to the v-cell), the 2PF2s are divided into three types (see Fig. 7): the 2PF2_a, the 2PF2_v, and the 2PF2_{av}.

The 2PF2_a: This fault is sensitized in cell c_v by applying two simultaneous operations to the same *a*-cell c_a (solid arrows in Fig. 7). Note that in this case, the 2PF is a combination of two weak faults involving two cells; both weak faults have the same *a*-cell as well as the same *v*-cell. The 2PF2_a consists of one FFM: *wCF_{ds}&wCF_{ds}*, with eight FPs; see Table VII. Note that the $\langle w0 : rd; 1 / \downarrow / - \rangle$ denotes only one FP since the

read value is irrelevant ($d = \text{don't care}$); the read operation is used to sensitize the fault. Note also that $\langle rx : rx; 0 / \uparrow / - \rangle$ denotes two FPs since $x \in \{0, 1\}$. The 2PF2_a can be caused by bridges between nodes of adjacent cells belonging to the same row (rBCC1, rBCC2), to the same column (cBCC1, cBCC2), or on same diagonal (dBCC1, dBCC2). They can also be caused by a bridge between a node of a cell and a bit line of an adjacent cell in the same row (rBCC3, rBCC4) [13], [16].

The 2PF2_v: This fault is sensitized in cell c_v by applying two simultaneous operations to the same cell c_v (solid arrows in the figure), while the *a*-cell has to be in certain state (dashed arrow in Fig. 7). Note that this fault is a combination of two weak faults: a single-cell weak fault and a weak weak fault involving two cells, whereby the operation has to be performed to the *v*-cell while the *a*-cell has to be in a certain state. The 2PF2_v consists of two FFMs; each with two FPs (see Table VII).

- *wCF_{dr}&wRDF*: Applying two simultaneous read operations to cell c_v will cause the cell to flip if cell c_a is in a certain state. The read operations return *correct* values.
- *wCF_{rd}&wDRDF*: Applying two simultaneous read operations to cell c_v will cause the cell to flip if cell c_a is in a certain state. The read operations then return *wrong* values.

Such faults can be caused by bridges between nodes of adjacent cells belonging to the same row, the same column, or on the same diagonal [13], [16].

The 2PF2_{av}: This fault is sensitized by applying two simultaneous operations: one to cell c_a and one to cell c_v ; see Fig. 7. It is a combination of a single-cell weak fault and a weak fault involving two cells, and can be caused by bridges between bit lines of different ports belonging to the same or to adjacent columns (BC6, BC7, rBCC6, rBCC8). The 2PF2_v consists of three FFMs, each with four FPs.

- *wCF_{ds}&wRDF*: A read operation applied to cell c_v flips the cell and the sense amplifier returns an incorrect value *if* a write operation is applied to cell c_a *simultaneously*.
- *wCF_{ds}&wIRF*: A read operation applied to cell c_v returns an incorrect value *if* a write operation is applied to cell c_a *simultaneously*. It should be noted that the state of cell c_v does not change.
- *wCF_{ds}&wRRF*: A read operation applied to cell c_v returns a random value *if* a write operation is applied to cell c_a *simultaneously*.

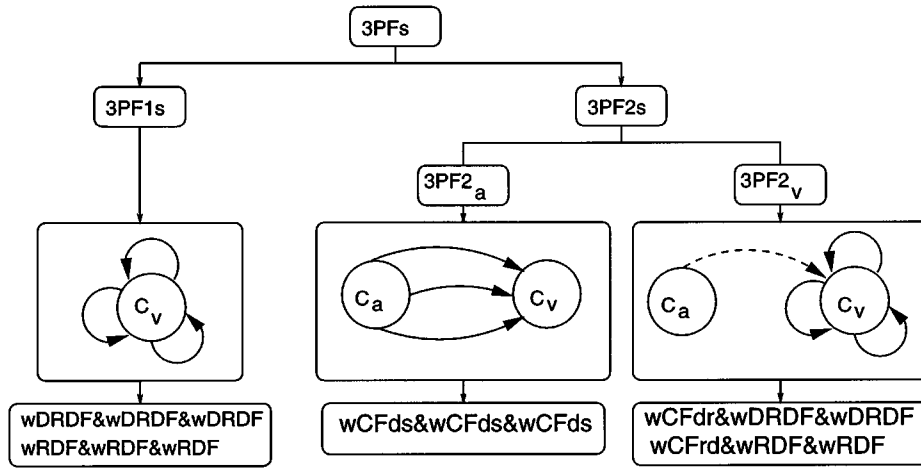


Fig. 8. Classification and taxonomy of 3PFs.

It should be noted that the above 2PFs are valid for memories which support simultaneous reading and writing of the same location, whereby the read data is discarded. If this is not supported, then the FFM $wRDF&wTF$ will not be realistic. In addition, the FFM $wCF_{ds}&wCF_{ds}$ will consist only of the FPs sensitized by simultaneous read operations to the same location.

3) *Three-Port Faults (3PFs)*: Three-port faults (3PFs) cannot be sensitized using SP operations or by using 2P operations; they require the use of the three ports simultaneously. The 3PFs can be considered as a combination of *three weak faults*. The 3PFs can be divided into faults involving a single cell (3PF1s) and faults involving two cells (3PF2s); see Fig. 8. A taxonomy of all realistic 3PFs is given in the same figure, while Table VIII shows the FPs of which each 3PF is composed. These 3PFs will be explained in detail in the following subsections.

The 3PF1s: The 3PF1s are based on a combination of *three single-cell weak faults*. In order to sensitize a 3PF1, the same cell has to be acted upon simultaneously via the three ports. It consists of two FFMs: $wDRDF&wDRDF&wDRDF$ and $wRDF&wRDF&wRDF$; each with two FPs (see Table VIII). They can be caused by the same defects as those causing the 2PF1s: $wDRDF&wDRDF$ and $wRDF&wRDF$; but with a different resistance value of the defect.

The 3PF2s: The 3PF2s are based on a combination of single-cell weak faults and weak faults involving two cells. Depending on which cells the three simultaneous operations are applied to (to the a-cell or to the v-cell), the 3PF2s are divided into two types (see Fig. 8). Based on the FPs found by simulating MFDs, the following 3PF2s have been derived (see also the sixth column of Table IX).

The 3PF2a: In this case, the 3PF is a combination of three weak faults involving two cells; they all have the same a-cell as well as the same v-cell (see Fig. 8). In order to sensitize the fault in cell c_v , three simultaneous operations have to be applied to the same cell c_a (solid arrows in the figure), while in order to detect the fault cell c_v has to be read. It consists of only one FFM: $wCF_{ds}&wCF_{ds}&wCF_{ds}$. Applying three simultaneous operations to cell c_a will sensitize a fault in cell c_v ;

TABLE VIII
LIST OF 3PFs; $x \in \{0, 1\}$ and $d = \text{Don't Care}$

FFM	Fault primitives
$wDRDF&wDRDF&wDRDF$	$\langle r0 : r0 : r0 / \uparrow / 0 \rangle$, $\langle r1 : r1 : r1 / \downarrow / 1 \rangle$
$wRDF&wRDF&wRDF$	$\langle r0 : r0 : r0 / \uparrow / 1 \rangle$, $\langle r1 : r1 : r1 / \downarrow / 0 \rangle$
$wCF_{ds}&wCF_{ds}&wCF_{ds}$	$\langle w0 : rd : rd / 0 / \uparrow / - \rangle$, $\langle w0 : rd : rd / 1 / \downarrow / - \rangle$, $\langle w1 : rd : rd / 0 / \uparrow / - \rangle$, $\langle w1 : rd : rd / 1 / \downarrow / - \rangle$, $\langle rx : rx : rx / 0 / \uparrow / - \rangle$, $\langle rx : rx : rx / 1 / \downarrow / - \rangle$
$wCF_{dr}&wDRDF&wDRDF$	$\langle 0 : r0 : r0 : r0 / \uparrow / 0 \rangle$, $\langle 0 : r1 : r1 : r1 / \downarrow / 1 \rangle$, $\langle 1 : r0 : r0 : r0 / \uparrow / 0 \rangle$, $\langle 1 : r1 : r1 : r1 / \downarrow / 1 \rangle$
$wCF_{rd}&wRDF&wRDF$	$\langle 0 : r0 : r0 : r0 / \uparrow / 1 \rangle$, $\langle 0 : r1 : r1 : r1 / \downarrow / 0 \rangle$, $\langle 1 : r0 : r0 : r0 / \uparrow / 1 \rangle$, $\langle 1 : r1 : r1 : r1 / \downarrow / 0 \rangle$

i.e., cell c_v flips. Note that this FFM consists of eight FPs; see Table VIII. The 3PF2a can be caused by the same SDs as those causing the 2PF2as, but having a different resistance value; see also Table IX.

The 3PF2v: In this case, the 3PF is a combination of three weak faults: a weak fault involving two cells and two single-cell weak faults. The weak fault involving two cells requires that the operation be performed to the v-cell while the a-cell has to be in certain state (dashed arrow in the Fig. 8). In order to sensitize the fault, three simultaneous operations have to be applied to cell c_v , and cell c_a has to be in certain state. Reading cell c_v will detect the fault. It consists of two FFMs: $wCF_{dr}&wDRDF&wDRDF$ and $wCF_{rd}&wRDF&wRDF$, each with two FPs (see Table VIII). It can be caused by the same SDs as those causing the 2PF2vs but having a different resistance value; see also Table IX.

It should be noted that the 3PFs discussed above are valid for memories allowing for two simultaneous reads and a write of the

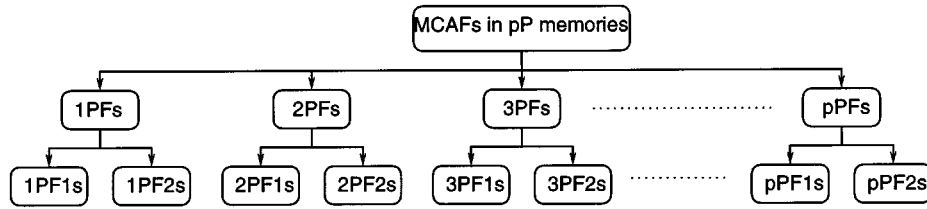
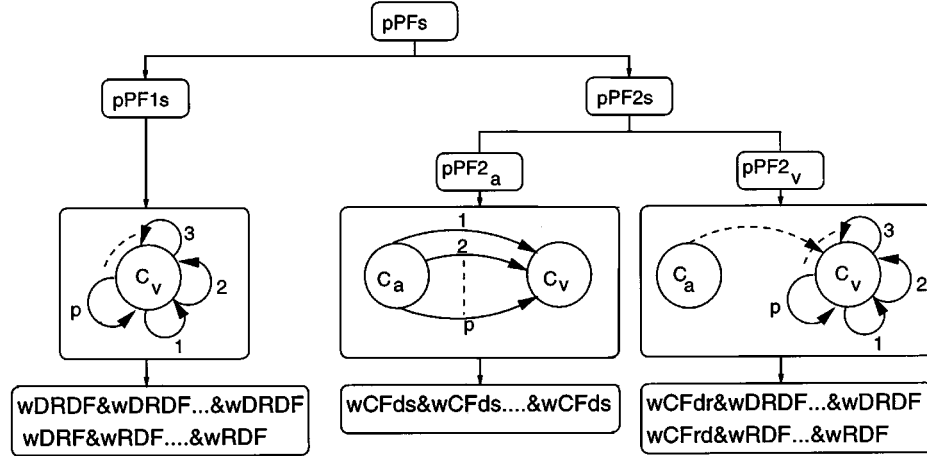
TABLE IX
OVERVIEW OF THE SIMULATION RESULTS FOR SOME MFDs; d = Don't Care Value

Label	R_{df} region	Fault primitive	Compl. fault primitive	Class	Fault model
OC3	Region I	wF	wF	-	-
	Region II	$\langle r0 : r0 : r0 / \uparrow / 0 \rangle_v$	$\langle r1 : r1 : r1 / \downarrow / 1 \rangle_v$	3PF1	$wDRDF \& wDRDF \& wDRDF$
	Region III	$\langle r0 : r0 : r0 / \uparrow / 1 \rangle_v$	$\langle r1 : r1 : r1 / \downarrow / 0 \rangle_v$	3PF1	$wRDF \& wRDF \& wRDF$
	Region IV	$\langle r0 : r0 / \uparrow / 0 \rangle_v$	$\langle r1 : r1 / \downarrow / 1 \rangle_v$	2PF1	$wDRDF \& wDRDF$
	Region V	$\langle r0 : r0 / \uparrow / 1 \rangle_v$	$\langle r1 : r1 / \downarrow / 0 \rangle_v$	2PF1	$wRDF \& wRDF$
	Region VI	$\langle r0 / \uparrow / 0 \rangle_v$	$\langle r1 / \downarrow / 1 \rangle_v$	1PF1	DRDF
	Region VII	$\langle r0 / \uparrow / 1 \rangle_v$	$\langle r1 / \downarrow / 0 \rangle_v$	1PF1	RDF
	Region VIII	$\langle r0 / \uparrow / 1 \rangle_v$ $\langle 0_T / \uparrow / - \rangle_v$	$\langle r1 / \downarrow / 0 \rangle_v$ $\langle 1_T / \downarrow / - \rangle_v$	1PF1 1PF1	RDF DRF
SC2	Region I	$\langle \forall / 1 / - \rangle_v$	$\langle \forall / 0 / - \rangle_v$	1PF1	SAF
	Region II	$\langle r1 / \downarrow / 0 \rangle_v$	$\langle r0 / \uparrow / 1 \rangle_v$	1PF1	RDF
	Region III	$\langle r1 / \downarrow / 1 \rangle_v$	$\langle r0 / \uparrow / 0 \rangle_v$	1PF1	DRDF
	Region IV	$\langle r1 : r1 / \downarrow / 0 \rangle_v$	$\langle r0 : r0 / \uparrow / 1 \rangle_v$	2PF1	$wRDF \& wRDF$
	Region V	$\langle r1 : r1 / \downarrow / 1 \rangle_v$	$\langle r0 : r0 / \uparrow / 0 \rangle_v$	2PF1	$wDRDF \& wDRDF$
	Region VI	$\langle r1 : r1 : r1 / \downarrow / 0 \rangle_v$	$\langle r0 : r0 : r0 / \uparrow / 1 \rangle_v$	3PF1	$wRDF \& wRDF \& wRDF$
	Region VII	$\langle r1 : r1 : r1 / \downarrow / 1 \rangle_v$	$\langle r0 : r0 : r0 / \uparrow / 0 \rangle_v$	3PF1	$wDRDF \& wDRDF \& wDRDF$
	Region VIII	wF	wF	-	-
BC6	Region I	$\langle w0 : r1 / \downarrow / 0 \rangle_{a,v}$	$\langle w1 : r0 / \uparrow / 1 \rangle_{a,v}$	2PF2	$wCF_{ds} \& wRDF$
	Region II	$\langle w0 : r1 / 1 / 0 \rangle_{a,v}$	$\langle w1 : r0 / 0 / 1 \rangle_{a,v}$	2PF2	$wCF_{ds} \& wIRF$
	Region III	$\langle w0 : r1 / 1 / ? \rangle_{a,v}$	$\langle w1 : r0 / 0 / ? \rangle_{a,v}$	2PF2	$wCF_{ds} \& wRRF$
	Region IV	wF	wF	-	-
BC7	Region I	$\langle r0 : w / \uparrow / 0 \rangle_v$		2PF1	$wRDF \& wTF$
		$\langle r1 : w / \downarrow / 1 \rangle_v$		2PF1	$wRDF \& wTF$
		$\langle w1 : r1 / \downarrow / 0 \rangle_{a,v}$		2PF2	$wCF_{ds} \& wRDF$
		$\langle w0 : r0 / \uparrow / 1 \rangle_{a,v}$		2PF2	$wCF_{ds} \& wRDF$
	Region II	$\langle w1 : r1 / \downarrow / 0 \rangle_{a,v}$		2PF2	$wCF_{ds} \& wRDF$
		$\langle w0 : r0 / \uparrow / 1 \rangle_{a,v}$		2PF2	$wCF_{ds} \& wRDF$
	Region III	$\langle w1 : r1 / 1 / 0 \rangle_{a,v}$		2PF2	$wCF_{ds} \& wIRF$
		$\langle w0 : r0 / 0 / 1 \rangle_{a,v}$		2PF2	$wCF_{ds} \& wIRF$
	Region IV	$\langle w1 : r1 / 1 / ? \rangle_{a,v}$		2PF2	$wCF_{ds} \& wRRF$
		$\langle w0 : r0 / 0 / ? \rangle_{a,v}$		2PF2	$wCF_{ds} \& wRRF$
	Region V	wF		-	-
rBCC1	Region I	$\langle 0 : 1 / 0 / - \rangle_{a,v}$	$\langle 1 : 0 / 1 / - \rangle_{a,v}$	1PF2	CF_{st}
	Region II	$\langle 0 : r1 / \downarrow / 0 \rangle_{a,v}$	$\langle 1 : r0 / \uparrow / 1 \rangle_{a,v}$	1PF2	CF_{rd}
		$\langle r0 : 1 / \downarrow / - \rangle_{a,v}$	$\langle r1 : 0 / \uparrow / - \rangle_{a,v}$	1PF2	CF_{ds}
	Region III	$\langle 0 : r1 : r1 / \downarrow / 0 \rangle_{a,v}$	$\langle 1 : r0 : r0 / \uparrow / 1 \rangle_{a,v}$	2PF2	$wCF_{rd} \& wDRDF$
		$\langle r0 : r0 : 1 / \downarrow / - \rangle_{a,v}$	$\langle r1 : r1 : 0 / \uparrow / - \rangle_{a,v}$	2PF2	$CF_{ds} \& wCF_{ds}$
		$\langle w0 : r1 : 1 / \downarrow / - \rangle_{a,v}$	$\langle w1 : r0 : 0 / \uparrow / - \rangle_{a,v}$	2PF2	$wCF_{ds} \& wCF_{ds}$
		$\langle w0 : r0 : 1 / \downarrow / - \rangle_{a,v}$	$\langle w1 : r1 : 0 / \uparrow / - \rangle_{a,v}$	2PF2	$wCF_{ds} \& wCF_{ds}$
	Region IV	$\langle 0 : r1 : r1 / \downarrow / 1 \rangle_{a,v}$	$\langle 1 : r0 : r0 / \uparrow / 0 \rangle_{a,v}$	2PF2	$wCF_{dr} \& wDRDF$
		$\langle r0 : r0 : 1 / \downarrow / - \rangle_{a,v}$	$\langle r1 : r1 : 0 / \uparrow / - \rangle_{a,v}$	2PF2	$wCF_{ds} \& wCF_{ds}$
		$\langle w0 : r1 : 1 / \downarrow / - \rangle_{a,v}$	$\langle w1 : r0 : 0 / \uparrow / - \rangle_{a,v}$	2PF2	$wCF_{ds} \& wCF_{ds}$
		$\langle w0 : r0 : 1 / \downarrow / - \rangle_{a,v}$	$\langle w1 : r1 : 0 / \uparrow / - \rangle_{a,v}$	2PF2	$wCF_{ds} \& wCF_{ds}$
	Region V	$\langle 0 : r1 : r1 : r1 / \downarrow / 0 \rangle_{a,v}$	$\langle 1 : r0 : r0 : r0 / \uparrow / 1 \rangle_{a,v}$	3PF2	$wCF_{rd} \& wRDF \& wRDF$
		$\langle r0 : r0 : r0 : 1 / \downarrow / - \rangle_{a,v}$	$\langle r1 : r1 : r1 : 0 / \uparrow / - \rangle_{a,v}$	3PF2	$wCF_{ds} \& wCF_{ds} \& wCF_{ds}$
		$\langle w0 : r1 : r1 : 1 / \downarrow / - \rangle_{a,v}$	$\langle w1 : r0 : r0 : 0 / \uparrow / - \rangle_{a,v}$	3PF2	$wCF_{ds} \& wCF_{ds} \& wCF_{ds}$
		$\langle w0 : r0 : r1 : 1 / \downarrow / - \rangle_{a,v}$	$\langle w1 : r1 : r0 : 0 / \uparrow / - \rangle_{a,v}$	3PF2	$wCF_{ds} \& wCF_{ds} \& wCF_{ds}$
	Region VI	$\langle 0 : r1 : r1 : r1 / \downarrow / 1 \rangle_{a,v}$	$\langle 1 : r0 : r0 : r0 / \uparrow / 0 \rangle_{a,v}$	3PF2	$wCF_{dr} \& wDRDF \& wDRDF$
		$\langle r0 : r0 : r0 : 1 / \downarrow / - \rangle_{a,v}$	$\langle r1 : r1 : r1 : 0 / \uparrow / - \rangle_{a,v}$	2PF2	$wCF_{ds} \& wCF_{ds} \& wCF_{ds}$
		$\langle w0 : r1 : r1 : 1 / \downarrow / - \rangle_{a,v}$	$\langle w1 : r0 : r0 : 0 / \uparrow / - \rangle_{a,v}$	3PF2	$wCF_{ds} \& wCF_{ds} \& wCF_{ds}$
		$\langle w0 : r0 : r1 : 1 / \downarrow / - \rangle_{a,v}$	$\langle w1 : r1 : r0 : 0 / \uparrow / - \rangle_{a,v}$	3PF2	$wCF_{ds} \& wCF_{ds} \& wCF_{ds}$
	Region VII	wF	wF	-	-
cBCC1	Region I	$\langle 0 : 1 / 0 / - \rangle_{a,v}$	$\langle 1 : 0 / 1 / - \rangle_{a,v}$	1PF2	CF_{st}
	Region II	$\langle 0 : r1 / \downarrow / 0 \rangle_{a,v}$	$\langle 1 : r0 / \uparrow / 1 \rangle_{a,v}$	1PF2	CF_{rd}
	Region III	$\langle 0 : r1 / \downarrow / 1 \rangle_{a,v}$	$\langle 1 : r0 / \uparrow / 0 \rangle_{a,v}$	1PF2	CF_{dr}
	Region IV	$\langle 0 : r1 : r1 / \downarrow / 0 \rangle_{a,v}$	$\langle 1 : r0 : r0 / \uparrow / 1 \rangle_{a,v}$	2PF2	$wCF_{rd} \& wRDF$
	Region V	$\langle 0 : r1 : r1 / \downarrow / 1 \rangle_{a,v}$	$\langle 1 : r0 : r0 / \uparrow / 0 \rangle_{a,v}$	2PF2	$wCF_{dr} \& wDRDF$
	Region VI	$\langle 0 : r1 : r1 : r1 / \downarrow / 0 \rangle_{a,v}$	$\langle 1 : r0 : r0 : r0 / \uparrow / 1 \rangle_{a,v}$	3PF2	$wCF_{rd} \& wRDF \& wRDF$
	Region VII	$\langle 0 : r1 : r1 : r1 / \downarrow / 1 \rangle_{a,v}$	$\langle 1 : r0 : r0 : r0 / \uparrow / 0 \rangle_{a,v}$	3PF2	$wCF_{dr} \& wDRDF \& wDRDF$
	Region VIII	wF	wF	-	-

same location (i.e., ' $wx_c : ry_c : ry_c$ '). If this is not supported, then the FFM: $wCF_{ds} \& wCF_{ds} \& wCF_{ds}$ will consist only of the FPs sensitized by three simultaneous read operations to the same location; i.e., ' $\langle rx : rx : rx / 0 / \uparrow / - \rangle_{a,v}$ ' and ' $\langle rx : rx : rx / 1 / \downarrow / - \rangle_{a,v}$ ' ($x \in \{0, 1\}$).

B. FFMs for pP Memories

In this section a classification of pPFs will be given; it will be based on extending the class of 2PFs and 3PFs, which are derived based on the simulation results.

Fig. 9. Classification of MCAFs in pP memories.Fig. 10. Classification and taxonomy of pPF s.

The 3PFs are divided into 3PF1s and 3PF2s. Such faults can be considered as an extension of the 2PFs; see Figs. 7 and 8. The 3PF1s, which consist of two FFMs, can be considered as an extension of the 2PF1s. For instance, the 3PF1 $wRDF \& wRDF \& wRDF$ is an extension of the 2PF1 $wRDF \& wRDF$. On the other side, the introduced 3PF2s are divided into the fault types 3PF2_a and 3PF2_v, which are extensions of the 2PF2_a, respectively, the 2PF2_v. By inspecting the two figures, one can see that there is no 3PF that can be considered as an extension of the 2PF1 $wRDF \& wTF$ neither of the 2PF2_{av} (i.e., 2PF2 sensitized by applying the two simultaneous sensitizing operations to two different cells: a-cell and v-cell). Such faults are caused by bridges between bit lines belonging to two different ports [13], [16]. It has been shown with inductive fault analysis that a bridge only occurs between physically adjacent lines and that the occurrence probability of bridges involving *at the most* two nodes is very large (96.6% on the average) compared with bridges involving more than two nodes [13]. Therefore, the assumption can be made that the 2PF2_{av} can only be caused by bridges involving at most two bit lines (belonging to different ports) that are physically adjacent to each other. That means that irrespective of the number of ports the MP memory consists of, the bridges between two bit lines belonging to any two different ports can only cause a 2PF2_{av}. Therefore, this is a unique 2PF that cannot be extended. A similar explanation can be given for the 2PF1 $wRDF \& wTF$.

Based on the above discussion, the FFMs for any MP memory can be derived. Such faults can be divided, based on the number of ports required in order to be sensitized, into p -classes: single-port faults (1PFs), two-port faults (2PFs), three-port faults (3PFs), ..., p -port faults (pPF s); see Fig. 9.

The pPF s are faults that can only be sensitized by p simultaneous operations; they are divided into faults involving a single-cell ($pPF1$ s) and faults involving two cells ($pPF2$ s); see Fig. 10. The $pPF1$ s are based on a combination of p single-cell weak faults; while the $pPF2$ s are based on a combination of single-cell weak faults and weak faults involving two cells. They are divided into two types (see Fig. 10): the $pPF2_a$ and the $pPF2_v$. The $pPF2_a$ is sensitized in cell c_v by applying p simultaneous operations to the same cell c_a (solid arrows in the figure); while the $pPF2_v$ is sensitized by applying p simultaneous operations to cell c_v , and cell c_a has to be in certain state. A taxonomy of all realistic pPF s is also given in Fig. 10. A similar explanation can be given as that given for 3PFs.

V. SIMULATION RESULTS

The simulation has been done first for SDs in 2P SRAMs. Thereafter, the simulation has been redone only for MFDs (i.e., SD causing 1PFs as well as 2PFs) in 3P SRAM design for one SD from each group (a group is a set of SDs which has a similar and/or complementary and/or interchanged, and/or interchanged complementary behavior; see Section II). The behavior of the other SDs within a group has been derived based on the found results. For the opens, the first simulation has been done for the case that $R_{op} = \infty$; while for shorts (bridges), the first simulation has been done for the case that $R_{sh} = 0$ ($R_{br} = 0$). If no fault occurs in these cases, then it does not make sense to simulate other cases for smaller values of R_{op} or bigger values of R_{sh} (R_{br}). If the fault occurs, then the simulation has been repeated for smaller values of R_{op} and bigger

values of R_{sh} (R_{br}). The boundary between the different behaviors of the cell (i.e., proper operation, strong fault, weak fault) is searched by stepping through the resistor value range. Each faulty behavior is reported in terms of a fault primitive (FP); if a strong fault is sensitized, then the FP notation introduced in Section IV is used to describe it. If a fault is only partially sensitized (e.g., weak fault) then the fault is denoted as wF .

In order to save space, only simulation results of some SDs for the 3P SRAM will be presented here; the results of other SDs are given in [13]. Table IX lists the simulation results for one open, one short, two bridges within a cell, and two bridges between cells. The first column in the table gives the name of the simulated SD; see also Table I through IV. The second column gives the resistance regions² ordered in an increasing values; the third and the fourth columns list the FP sensitized by the simulated SD and the derived complementary FP (if applicable), respectively. Remember that SDs with an interchanged behavior cause similar FPs, while SDs with an interchanged complementary behavior cause complementary FPs. The fifth column gives the class of the sensitized fault; i.e., single-port faults involving a single cell (1PF1s), single-port faults involving two cells (1PF2s), two-port faults involving a single cell (2PF1s), two-port faults involving two cells (2PF2s), three-port faults involving a single-cell (3PF1s), and three-port faults involving two cells (3PF2s). The table shows clearly that the sensitized fault is *strongly dependent* on the resistance value of the SD; e.g., the SC2 can sensitize seven different FPs.

VI. FAULT PROBABILITIES

In order to determine the importance of each FFM, their probabilities of occurrence have been calculated for an industrial 2P SRAM and a 3P SRAM. For the 2P SRAM, the probabilities have been calculated by using two approaches [13], [16]: first by assuming that all SDs are equal likely (E.L.) to occur and then by using *inductive fault analysis* (IFA). IFA has been performed for two different layouts ML and WL, with sizes of 32 Kbits and 64 Kbits, respectively. The two layouts implement the same electrical memory circuit of Fig. 1 for $p = 2$. The results are shown in Table X. It should be noted that the used IFA tool does not deal with partial opens; i.e., opens with a resistance value $R_{op} < \infty$; therefore, only shorts and bridges (see Section II) have been considered with IFA. Since DRFs are caused only by opens, their probabilities cannot be determined for ML and WL; it is given in the table as “not applicable (n.a.)” It is clear from the table that the probability of occurrence of a FFM is layout dependent. An FFM which is not realistic for a certain layout can have a considerable probability for another one; e.g., the $wCF_{ds} \& wIRF$ has a probability of 0.725% for ML and of 0% for WL (using IFA). That means that in order to reach a very high fault coverage, a test algorithm designer has to take all FFMs into consideration. Note that for ML, 94.409% of the faults are 1PFs and 5.591% are 2PFs; while for WL, 2PFs consists of 1.387% (that is $\simeq 4$ times smaller than 2PFs for ML).

For the 3P SRAM, the probabilities have been calculated only by assuming the all SDs are equal likely to occur; see

TABLE X
PROBABILITIES OF FFMS FOR 2P SRAMS

FFM	SD E.L.	IFA ML	IFA WL
SAF	29.921	29.636	10.737
TF	10.697	16.513	24.035
RDF	5.418	11.561	13.041
DRDF	0.623	0.141	0.048
IRF	7.517	11.264	25.336
RRF	2.606	1.275	1.667
NAF	1.048	1.795	6.460
USF	0.944	9.071	5.785
DRF	0.598	n.a	n.a
Total 1PF1s	59.372	81.256	87.109
CF _{ds}	6.819	5.227	5.661
CF _{ir}	3.758	5.657	3.051
CF _{rr}	0.681	2.245	1.221
CF _{st}	11.805	0.022	1.439
CF _{rd}	0.453	0.002	0.089
CF _{dr}	0.101	0.001	0.015
Total 1PF2s	24.456	13.153	11.504
Total 1PFs	83.828	94.409	98.613
wRDF&wRDF	0.554	2.835	0.969
wDRDF&wDRDF	1.573	0.944	0.323
wRDF&wTF	0.371	0.704	0.000
Total 2PF1s	2.498	4.483	1.292
wCF _{ds} &wRDF	3.302	0.118	0.000
wCF _{ds} &wIRF	6.003	0.752	0.000
wCF _{ds} &wRRF	1.485	0.236	0.000
wCF _{ds} &wCF _{ds}	2.234	0.000	0.000
wCF _{rd} &wRDF	0.132	0.001	0.076
wCF _{dr} &wDRDF	0.617	0.001	0.019
Total 2PF2s	13.674	1.108	0.095
Total 2PFs	16.172	5.591	1.387

Table XI. The table shows that the occurrence probability of 1PFs is 80.333%, that of 2PFs is 15.791%, and that of 3PFs is 3.876%. That means that if only conventional SP tests are used to test 3P memories, the fault coverage cannot be more than 80.333%, which is not acceptable. Therefore, the 2PFs as well as the 3PFs have to be considered. That requires (in addition to SP tests) 2P tests as well as 3P tests which will detect the 2PFs and the 3PFs, respectively.

VII. TEST PROCEDURE

As mentioned in Section V, memory cell array faults for a p -port MP memory are divided into p classes: 1PFs, 2PFs, 3PFs, ..., and p PFs.

For the detection of 1PFs, which consist of the conventional faults occurring in SP memories, a test such as MATS+, March C-, etc. [15], [17]–[19] can be used. The test has to be applied in the *worst case* p times, once via each port.

For the detection of p PFs with $p > 1$ (i.e., 2PFs, 3PFs, etc.) special tests are required. By inspecting the p PFs introduced in Section VI, it can be seen that the p PF1, p PF2_a, and p PF2_v faults require p simultaneous operations to the same location in order to be sensitized; therefore, the required tests for such faults will be single addressing (i.e., all ports use the same address). If we assume that the memory cell array consists of n locations, then the time complexity of such tests will be $\theta(n)$.

²The exact resistance values for each region are process specific and Intel proprietary.

TABLE XI
PROBABILITIES OF THE FFM FOR 3P SRAM

Class	FFM	Prob. %
1PFs (80.333%)	SAF	29.315
	TF	10.312
	DRDF	0.448
	RDF	4.455
	IRF	7.231
	RRF	2.507
	DRF	0.575
	NAF	1.008
	USF	0.908
	CF _{ds}	6.466
	CF _{st}	11.355
	CF _{ir}	3.373
	CF _{rr}	1.042
	CF _{dr}	0.097
	CF _{rd}	0.435
	CF _{tr}	0.806
2PFs (15.791%)	wRDF&wRDF	0.944
	wDRDF&wDRDF	0.926
	wRDF&wTF	0.357
	wCF _{ds} &wCF _{ds}	2.536
	wCF _{dr} &wDRDF	0.127
	wCF _{rd} &wRDF	0.593
	wCF _{ds} &wRDF	3.105
	wCF _{ds} &wIRF	5.775
	wCF _{ds} &wRRF	1.428
3PFs (3.876%)	wDRDF&wDRDF&wDRDF	0.814
	wRDF&wRDF&wRDF	0.172
	wCF _{ds} &wCF _{ds} &wCF _{ds}	2.142
	wCF _{dr} &wDRDF&wDRDF	0.574
	wCF _{rd} &wRDF&wRDF	0.197

On the other hand, the 2PF_{2av} faults are the only faults requiring the access of two different locations at a time in order to be sensitized (i.e., one operation to a-cell and one to v-cell); therefore, the test for such faults requires double addressing (i.e., it accesses two different addresses at a time). It has been shown with IFA that the SDs can only occur between adjacent cells [13], [16]. Therefore, for a given v-cell, the test has to access only the limited number of v-cell's neighbors which are the possible a-cells. As a consequence, the required test has a worst time complexity of $\theta(n)$.

The question that arises now is the following: In order to test a p -port memory, do we need to test each p PF class (i.e., 1PF, 2PF, 3PF, etc) separately? That is, apply the following.

- 1) Test(s) to detect 1PFs p times.
- 2) Test(s) to detect 2PFs $C_2^p = (p^2 - p)/2$ times.
- 3) Test(s) to detect 3PFs C_3^p times.
- ...
- p . Test(s) to detect p PFs once.

The answer to the above question is "no". The above test procedure can be optimized by taking into consideration the nature of each p PF class; this will be discussed below.

The p PF class consists of p PF1 and p PF2. The p PF1s for $p > 2$ consists of two FFMs that are extensions of two FFMs of 2PF1s; see Figs. 7 and 10. The sensitization of the p PF1s for $p > 2$ requires the application of p simultaneous read operations to the same location. This will also sensitize 2PF1s, 3PF1s, ..., and $(p-1)$ PF1s; except the 2PF1 wRDF&wTF, since that fault is a unique 2PF and has no extension for p PFs with

$p > 2$. Therefore, a test detecting p PF1s will also detect all $(p-1)$ PF1s, ..., 3PF1s, and 2PF1s; except wRDF&wTF. That fault, caused by bridges between bit lines belonging to the same column and to *two different ports* [13], [16], is sensitized by applying a simultaneous read and write to the same location using the two ports; the write operation will fail due to the defect. The first assumption is to apply a test for such faults C_2^p times. However, this can be reduced only to p times as follows.

1. Apply a test detecting wRDF&wTF by performing a write operation via the first port (P_a) and read operations via the other $(p-1)$ ports. In that case, the fault will be detected if it is caused by a bridge between bit lines of P_a and port $P_i \neq P_a$.
2. Apply a test detecting wRDF&wTF by performing a write operation via P_b and read operations via the other $(p-1)$ ports. In that case, the fault will be detected if it is caused by a bridge between bit lines of port P_b and port $P_i \neq P_b$.
- ...
- p . Apply a test detecting wRDF&wTF by performing a write operation via P_p and read operations via the other $(p-1)$ ports. In that case, the fault will be detected if it is caused by a bridge between bit lines of port P_p and port $P_i \neq P_p$.

On the other hand, p PF2s for $p > 2$ are divided into p PF2_a and p PF2_v; both are extensions of 2PF2_a and 2PF2_v; see Figs. 7 and 10. The sensitization of the p PF_a requires the application of p simultaneous operations to the a-cell. This will also sensitize 2PF2_a, 3PF2_a, ..., and $(p-1)$ PF2_a. A similar explanation can be given for p PF2_v. Therefore, a test detecting p PF2_a will also detect all $(p-1)$ PF2_a, ..., 3PF2_a, and 2PF2_a; while a test detecting p PF2_v will also detect all $(p-1)$ PF2_v, ..., 3PF2_v, and 2PF2_v. Since the 2PF2_{av} faults have no extension for p PFs (see Figs. 7 and 10), they are unique 2PFs and require being considered separately for their testing. Such faults are caused by bridges between bit lines belonging to *two different ports*, to the same (or adjacent) column(s) [13], [16]. Their detection requires the application of a write operation to the a-cell and a read operation to the v-cell simultaneously. In order to detect the 2PF2_{av} faults in a p -port memory, the first assumption is to apply a test for such faults C_2^p times. However, this can be reduced to p times; this can be done in a similar way as for wRDF&wTF.

Based on the above, one can conclude that testing a p -port memory can be done by applying the following.

- 1) Test(s) to detect 1PFs p times.
- 2) Test(s) to detect p PFs with $p > 1$ one time; this includes p PF1s (except wRDF&wTF), p PF2_as and p PF2_vs.
- 3) Test(s) to detect the wRDF&wTF faults p times
- 4) Test(s) to detect the 2PF2_{av} faults p times.

It should be clear from the above that the test procedure for an MP memory has a time complexity of $\theta(p.n)$, whereby p is the number of ports and n is the size of the memory cell array.

VIII. CONCLUSIONS

In this paper a complete analysis of all spot defects in a p -port SRAM design has been performed, based on circuit

simulation and IFA. The simulation has been done for two-port and three-port SRAMs. The transformation of the electrical faults, caused by the defects, into realistic functional fault models (FFMs) has been presented. It has been shown that the FFM is strongly dependent on the resistance value of the defect. The results show that the fault models for p -port memories consist of p classes: single-port fault (1PFs), two-port faults (2PFs), ..., p -port faults (p PFs). The 1PFs are faults that can be sensitized using single-port operations. On the other hand, p PFs are faults that *cannot* be sensitized using single-port operations; they require the use of the p ports of the memory *simultaneously*. A precise notation for all faults has been presented, such that ambiguities and misunderstanding will be prevented.

Furthermore, the probability of occurrence of such faults has been determined for two-port memories by using two approaches, first by assuming that all defects are equal likely to occur and then by performing IFA to two different layouts implementing the same circuit function. The probabilities have been also calculated for a three-port memory, while assuming that all defects are equal likely to occur. The results show that a high fault coverage can not be reached with single-port tests; special tests for multiport faults (i.e., 2PFs, 3PFs, etc) are required. Therefore, a test algorithm designer has to take all realistic faults into consideration in order to obtain a high fault coverage.

Finally, the test procedure for p -port memories has been discussed. The time complexity of the tests required for the detection of the introduced realistic p PFs is of $\theta(n)$ in the worst case, and that of the test procedure required to test any multiport memory is $\theta(n.p)$; whereby n is the size of the memory, irrespective of the number of ports of which the multiport memory consists. This is very attractive industrially.

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Said Hamdioui (S'97–M'01) received the Baccalaureate with honors in 1991, in Morocco. He received the MSEE degree with honors from Delft University of Technology, The Netherlands, in 1997. He additionally received the Ph.D. degree with honors from the same university in 2001.

From October 1998 until July 1999, and from January 2000 until September 2000, he had internships with Intel Corporation at Santa Clara and Folsom, CA, respectively. Currently he is a Visiting Faculty at Intel in CA. His research interests concern fault modeling, test design, circuit simulation, DFT, etc. for single-port and multiport SRAM's. He has published more than 15 papers in these areas.

Ad J. van de Goor (M'87–SM'98–F'00) obtained the MSEE degree from the Delft University of Technology, Delft, The Netherlands. He additionally obtained the MSEE and a Ph.D. degree from Carnegie-Mellon University, Pittsburgh, PA.

He worked for Digital Equipment Corporation, in Maynard, MA, as the Chief Architect of the PDP-11/45 computer, and for IBM in The Netherlands and in the USA, being responsible for the architecture of the embedded systems. Currently he is a Professor of Computer Engineering at the Delft University of Technology. His main research interest is testing logic and memories. He has written two books and over 120 papers in the areas of computer architecture and testing.

Dr. van de Goor is a member of the editorial board of the *Journal of Electronic Testing: Theory and Practice*.