A Very Wide Bandwidth Digital VCO Using Quadrature Frequency Multiplication and Division Implemented in AlGaAs/GaAs HBT's

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***Abstract*— A digital voltage-controlled oscillator (VCO) is described which uses frequency multiplication and division to achieve very wide bandwidth. The VCO uses current-mode logic and does not require reactive elements such as inductors, capacitors or varactors. A novel, fully symmetric exclusive-OR (XOR) circuit was developed which uses product pairs and emitter-coupled logic. To achieve the highest performance possible, the critical path is symmetric and special physical design techniques were developed to promote matched-capacitance. The maximum measured frequency was 13.66 GHz. The chip occupies 1.9 mm $\times$ 1.6 mm and dissipates 2.45 W at a supply voltage of -6.0 V. With a measured frequency range from 1.25 to 13.66 GHz, this circuit has the widest bandwidth reported in the literature for any VCO, digital or analog.**

***Index Terms*—Current-mode logic, exclusive-OR gate, heterostructure bipolar transistors, matched-capacitance layout, phase-locked loop, quadrature frequency multiplication, ring-oscillator, variable-delay element, voltage-controlled oscillators.**

I. Introduction

OVER the past decade there has been an explosion in high-speed communications and electronics, most notably the advent of fiber-optic and wireless communications and the ever-increasing clock speeds of microprocessors. As the trend continues, high-speed clock synchronization and generation will become increasingly critical. Furthermore, advances in device integration leads to larger chips that require the distribution of accurate clock signals. Because the distribution tree may have radically different lengths and parasitics, synchronization of the clock signals at the receivers can be difficult and has been the subject of much interest [1], [2], [9].

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To date, complementary metal–oxide–semiconductor (CMOS) technology has been the dominant throughout the industry, but it has not displaced other technologies for extremely high-speed designs. The use of non-CMOS and even nonsilicon technologies is often in pursuit of higher performance, either due to material properties (such as the improved electron mobility of gallium arsenide) or device technology (such as heterostructures). This improvement in performance typically has a significant cost in terms of price, reliability, or device yield.

The fast RISC (F-RISC) project at Rensselaer Polytechnic Institute, Troy, NY, was founded to investigate whether low-yield, high-speed processes could be used to create a computer with significantly higher performance. The F-RISG/G processor uses small chips on a multichip module (MCM) [3]. With a cycle time of 1 ns and a clock frequency of 2 GHz, the distribution of clock signals to all chips on the MCM is one of the most critical aspects of the design. The voltage-controlled oscillator (VCO) was developed in part to investigate the upper limits of the fabrication process selected for F-RISC/G. It also has applications in wideband phase-locked loops, communications, signal synchronization and clock generation/deskew.

II. Device and Material Characteristics

The VCO was fabricated in the Rockwell 50 GHz baseline GaAs/AlGaAs process. Gallium arsenide (GaAs) has significantly higher electron mobility when compared to Silicon, reducing the transistor base-transit time and increasing the device performance. The use of GaAs does come with significant drawbacks such as low device integration levels and material fragility.

Heterostructure bipolar transistors (HBT's) offer significantly higher performance than homojunction bipolar transistors (BJT's). This improvement in speed is due primarily to a heterojunction at the base-emitter interface that reduces the back-injection of carriers from the base to the emitter and improves the device gain significantly. The base doping is often increased to reduce resistance at the expense of the gain and improves the performance of the device. Emitter doping can also be dropped in order to reduce the base-emitter junction capacitance C_{je}.

III. Interconnect Characteristics and Performance

Capacitive coupling for GaAs and other semi-insulating substrates presents a different situation than in silicon. Because the substrate is semi-insulating, the groundplane is relatively far away, reducing the capacitance to ground but increasing

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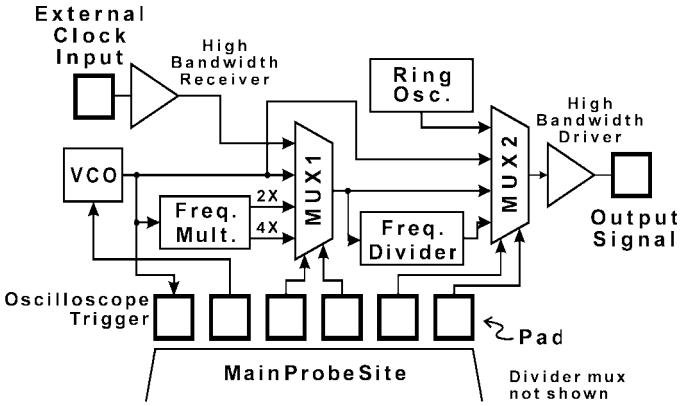

Fig. 1. Voltage-controlled oscillator (VCO) architecture.

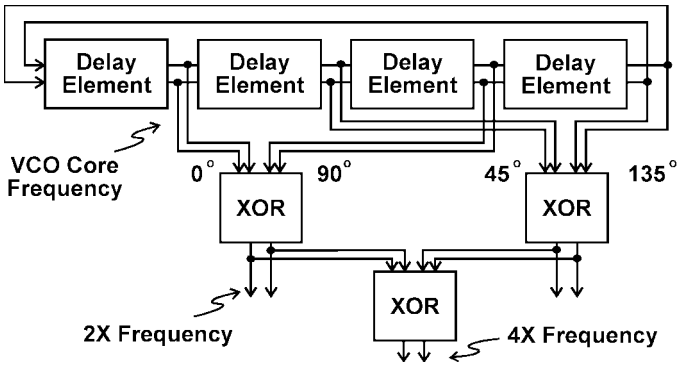

Fig. 2. VCO core signal generator and frequency multiplier.

the coupling between adjacent nodes. The anisotropic properties (larger dielectric constant in the horizontal direction) of some low K dielectrics like polyimide can also increase the wire–wire coupling, further increasing the design complexity. To avoid the large computational and memory requirements of conventional field solvers, we have used QuickCap [4] that employs random walks to extract parasitic capacitance and has significantly lower resource requirements.

IV. Circuit Design

The VCO (Fig. 1) is based upon a ring-oscillator composed of variable-delay elements from which multipliers generate signals at two and four times the core frequency [5]. A divider chain has been added which provides divisors of two, four, and eight. An ordinary ring-oscillator composed of 16 inverter stages is included on the chip as a process monitor.

Multiple signal paths have been provided through the circuit using multiplexers to allow the testing of partially functional chips. Only the main probe site and the high-speed output site are required for testing while the divider and external clock probe sites assume a default value when not in use. Current-mode logic (CML) is used throughout the VCO to reduce switching noise and jitter.

A. Core Oscillator and Frequency Multiplier

The core oscillator (Fig. 2) is composed of four voltage-controlled variable-delay elements that are connected in a circular fashion with one inversion along the path. The frequency is doubled and quadrupled using a novel exclusive-OR gate that is perfectly symmetric in order to reduce phase error.

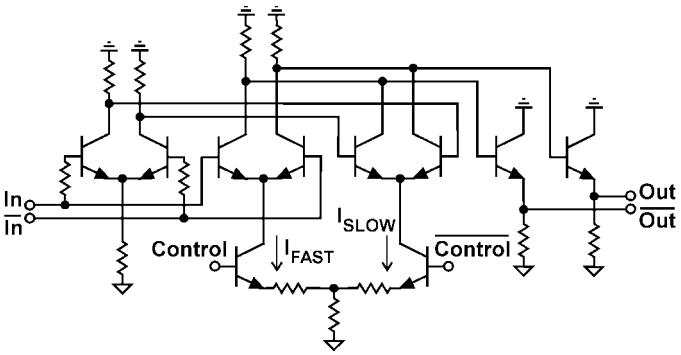

Fig. 3. Voltage-controlled variable-delay element.

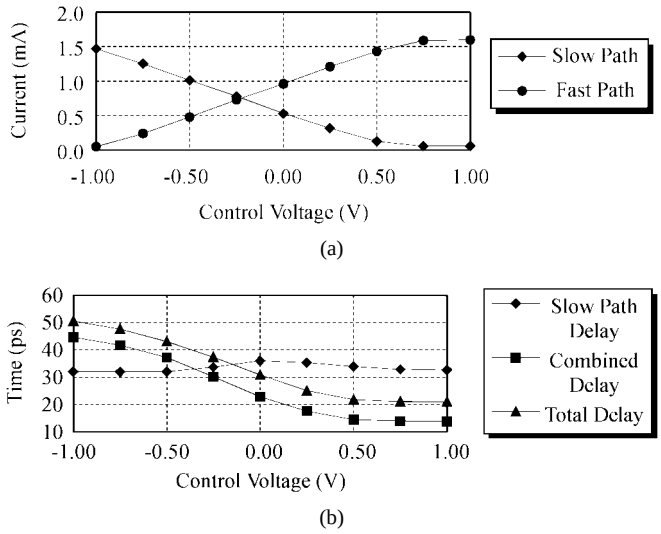

Fig. 4. Delay element signal path charactersitics. (a) Slow and fast path device currents. (b) Signal delay for slow, combined (slow + fast), and total paths.

Because the signal has to propagate through the circuit twice to complete one oscillation, the delay of each stage is 45°. Signals separated by two stages are 90° out-of-phase and are said to be in quadrature. With the use of a multiplier, these two signals may be combined to generate a new signal at twice the original frequency. The four separate taps provide two sets of quadrature outputs that may be used to double the core frequency. Because the shift between successive stages is 45°, the phase shift between the doubled-frequency signals are also in quadrature and may be combined to produce a signal at four times the core frequency.

B. Variable-Delay Element

The core frequency is adjustable due to the use of variable-delay elements [6] (Fig. 3). Switching the current between slow and fast paths within the element varies the delay. Fig. 4(a) shows the simulated shift in current between the slow and fast paths while Fig. 4(b) shows the delay through the slow path, the combined paths (slow + fast), and the total delay including the output emitter-followers.

C. Frequency Divider

Frequency division is accomplished using sequential toggle flip-flops, each providing a successive division factor of two. Since the frequency is cut in half after every stage, only the

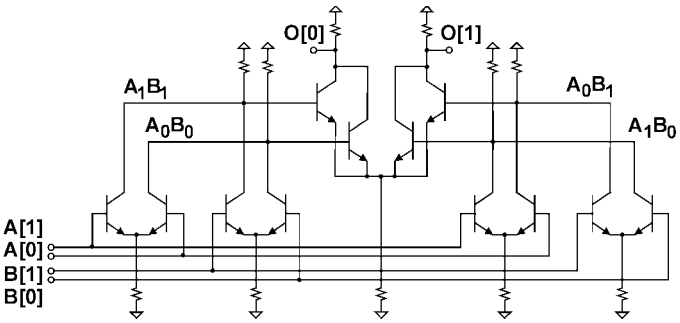

Fig. 5. Novel, fully symmetrical exclusive-OR circuit.

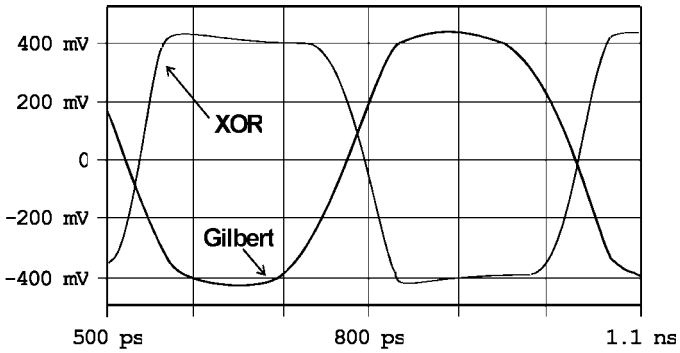

Fig. 6. Comparison of simulated waveforms from balanced Gilbert multiplier and novel XOR.

first stage requires careful design. A buffer is used between the first and second stages to ensure the quality of the signal, after which no additional buffers are required.

D. Frequency Multiplier/Novel XOR Circuit

Typically, signal multiplication is performed using analog circuits such as the Gilbert multiplier [7], which is capable of four-quadrant operation. However, in order to generate a high-quality signal at twice the input frequency, the delay for both input signals must be the same, a characteristic that the Gilbert multiplier does not possess. To compensate, Schmidt [8] combined two Gilbert cells with inverted signal connections to cancel out the input phase shift.

Our circuit does not use analog signal multiplication. Instead, the product pairs for the exclusive-OR logic function $(a_0b_0, a_0b_1, a_1b_0,$ and $a_1b_1)$ are generated and combined to realize the function (Fig. 5). Although it requires the same amount of devices as the dual-multiplier approach, SPICE simulations have indicated that our circuit has higher rise times at lower frequencies (Fig. 6). Due to the perfect symmetry, the circuit has low phase error and is used as a phase detector in a 2 GHz clock deskew circuit that reduces skew to less than 5 ps [9].

V. Physical Design and Layout

To produce robust multi-GHz circuits, the physical layout must be considered to be nearly as important as the circuit design itself. Mismatched parasitic loading can have disastrous effects upon the circuit performance; consequently the VCO physical layout was handcrafted. To compensate, special techniques were developed to produce layouts with closely matched capacitance in order to reduce skew.

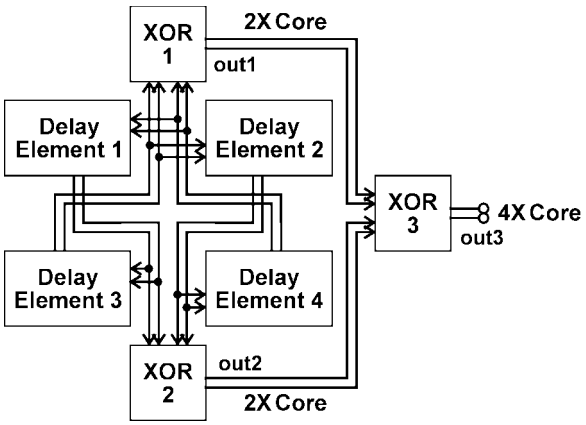

Fig. 7. Closely balanced layout of VCO core, 2× and 4× multipliers with both inputs to one multiplier imbalanced.

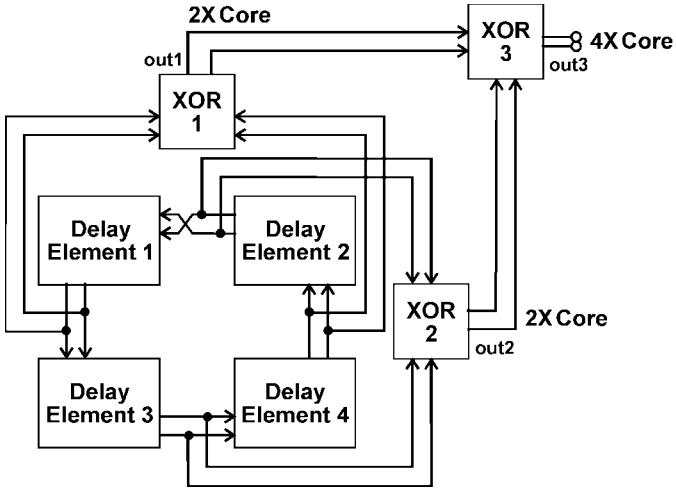

Fig. 8. Closely balanced layout of VCO core, 2× and 4× multipliers with one input to both multipliers imbalanced.

Because symmetry is essential in order to reduce phase error, the four delay elements are arranged in a square to equalize the interconnect parasitics. Two alternative arrangements for routing the signals between the delay elements and the multipliers were developed in order to investigate the effects of phase shifts upon the output signals (Figs. 7 and 8).

Assuming a sinusoidal signal generated by the core oscillator, the input to the multipliers will have a phase shift depending upon the configuration used. For the layout in Fig. 7, one set of multiplier inputs has a phase shift δ, hence the 2× and 4× multiplier outputs are (arbitrarily assigning the phase shift δ to the first set of inputs)

$$\text{OUT1} = \sin(\theta + \delta) * \sin(\theta + \pi/2 + \delta) \quad (1)$$

$$\text{OUT2} = \sin(\theta + \pi/4) * \sin(\theta + \pi/4 + \pi/2) \quad (2)$$

$$\text{OUT3} = (1/8) * [\sin(4\theta + 2\delta) + \sin(2\delta)]. \quad (3)$$

For the layout in Fig. 8, the multiplier outputs are

$$\text{OUT1} = \sin(\theta) * \sin(\theta + \pi/2 + \delta) \quad (4)$$

$$\text{OUT2} = \sin(\theta + \pi/4) * \sin(\theta + \pi/4 + \pi/2 + \delta) \quad (5)$$

TABLE I
VCO STATISTIC

Chip Area	1.9 mm X 1.6 mm	Supply	V_{EE}=-6.0
Emitter Area	1.4 μm X 3.0 μm	Control V	± 1.0 V
Freq. Range	2.04 - 13.66 GHz	HBTs	412
Wafer Size	4-inch	Power	2.45 W

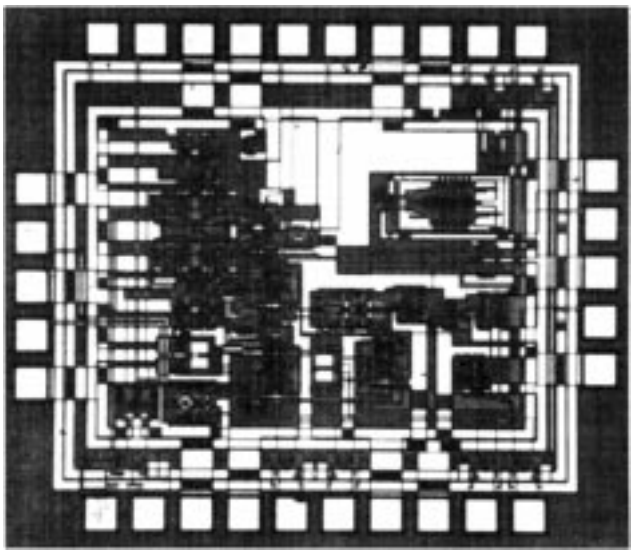

Fig. 9. Microphotograph of fabricated VCO chip.

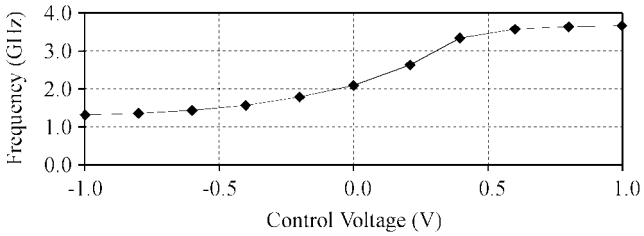

Fig. 10. Measured VCO core tuning range (nonmultiplied).

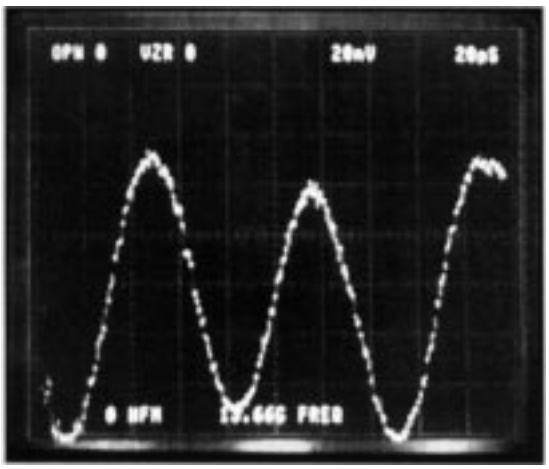

Fig. 11. Oscilloscope photograph of 13.66 GHz VCO output.

$$\begin{aligned}\text{OUT3} = (1/4) * [&(1/2) * \sin(4\theta + 2\delta) - \sin(\delta) \\ &* (\sin(2\theta + \delta) + \cos(2\theta + \delta)) \\ &+ \sin^2(2\delta)]. \end{aligned} \tag{6}$$

In (8), the phase shift is transferred to the output signal and a DC offset is generated while (11) has a subharmonic component at $2\times$. Consequently a phase shift on both inputs to one multiplier is preferable to a phase shift on one input of both multipliers, and the arrangement in Fig. 7 was selected for the VCO layout.

VI. RESULTS

A microphotograph of the fabricated chip is in Fig. 9, and the measured tuning range for the core oscillator is shown in Fig. 10. The minimum (undivided) frequency was 1.25 GHz which should result in a divided output frequency of 0.156 GHz (the divider was not tested due to a limited number of probes). The maximum measured frequency was 13.66 GHz and is shown in Fig. 11. Simulation results have indicated that the speed should be 13.9 GHz for a control voltage of 0.6 V, an error of 1.76%.

VII. SUMMARY

A voltage-controlled oscillator (VCO) with a very wide measured bandwidth of 1.25 GHz (undivided) to 13.66 GHz has been described. The circuit has the widest bandwidth reported in the literature for any VCO, digital or analog. A novel fully symmetric exclusive-OR circuit was presented and discussed along with the variable-delay frequency generation mechanism. The VCO and its subcircuits have application in high-speed communications, phase-locked loops, signal synchronization and clock generation/distribution.

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