Reliability of Space-Grade vs. COTS SRAM-Based FPGA in N-Modular Redundancy

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***Abstract*—In this paper, we evaluate the suitability of different SRAM-based FPGAs for harsh radiation environments (e.g., space). In particular, we compare the space-grade and radiation-hardened by design *Virtex-5QV* (XQR5VFX130) with the commercial off-the-shelf *Kintex-7* (KC7K325T) from *Xilinx*. The advantages of the latter device are: 2.5 times the resources of the space-grade FPGA, faster switching times, less power consumption, and the support of modern design tools. We focus on resource consumption as well as reliability in dependence of single event upset rates for a geostationary earth orbit satellite application, the *Heinrich Hertz* satellite mission. For this mission, we compare different modular redundancy schemes with different voter structures for the qualification of a digital communication receiver. A major drawback of the *Kintex-7* are current-step single event latchups, which are a risk for space missions. If the use of an external voter is not possible, we suggest triple modular redundancy with one single voter at the end, whereby the *Virtex-5QV* in this configuration is about as reliable as the *Kintex-7* in an N-modular redundancy configuration with an external high-reliable voter.**

I. Introduction

Radiation-hardened integrated circuits (ICs) and field-programmable gate arrays (FPGAs) are specially made for space missions and have a wide distribution there. However, also commercial off-the-shelf (COTS) ICs and FPGAs were already used in space to achieve higher speed, transfer rates, and advanced I/O capabilities with less power consumption for less money. On the other hand, expensive testing is needed [1] to satisfy the requirements for using them in space without risking the whole space mission. Without extensive testing the mission requirements should be downscaled.

For the project *Fraunhofer On-Board Processor* (FOBP) [2] on the *Heinrich Hertz* satellite mission , scheduled for the geostationary earth orbit (GEO), is the need to choose well between radiation-hardened and COTS electronic parts. For the latest *UltraScale Xilinx* FPGAs, to the best of our knowledge, there is no radiation data published yet. Therefore, a lack of information exists to establish their usability for space missions. In this article, we compare FPGAs from the space-grade type *Xilinx Virtex-5QV* with the *Xilinx Kintex-7* family through a radiation and redundancy analysis.

After a related work section, we introduce single event upset (SEU) effects, their mitigation on FPGAs and compare space-grade with COTS SRAM-based FPGAs. We analyze the radiation sensitivity of both kinds and describe in detail the current-step single event latchup problem of the *Xilinx Kintex-7*. The next section shows the used reliability model. In the evaluation section some results concerning cost (usage of resources) and reliability calculations are presented, using a receiver design and different N-modular redundancy (NMR) schemes as test cases. Conclusions about the reliability of the compared FPGA families are drawn in the last section of this article.

978-1-4673-7501-6/15/$31.00

II. Related Work

Previous research has studied the impact of SEUs on SRAM FPGA devices [3]. Many techniques have been proposed to provide highly reliable FPGA devices, e.g., radiation-hardened FPGAs [4], to lower the effect of radiation-induced SEUs. However, radiation-hardened SRAM FPGAs typically have a low density, and they only may lower the probability of SEUs but not completely avoid them. Therefore, also non radiation-hardened FPGAs, like the Xilinx *Kintex-7*, are evaluated for an appliance in a harsh radiation environment [5]. Even on radiation-hardened FPGAs, the SEU rate in a low-earth orbit flight experiment can be up to 16 events per day [6]. In this paper, we focus on a broadband satellite application, whose possible upset rates are analyzed in [7]. Hence, in space missions, SEU correction mechanisms become essential to avoid the accumulation of latent faults and ensure correct operation of an FPGA.

A wide variety of SEU fault mitigation techniques for SRAM-based FPGAs have been proposed during the past years. These techniques can be categorized into module redundancy techniques such as triple modular redundancy (TMR) [8] and techniques that use *scrubbing* of the FPGA configuration memory [9], [10]. Also, the combination of both techniques has been shown to be able to increase the reliability of FPGA modules significantly [11]. FPGA-based TMR approaches replicate a given module, which shall be protected either statically or dynamically [8]. The different granularities of voted replicas are evaluated in [12]. However, no upset rates and consequential no reliability figures are provided. Nevertheless, TMR techniques are known to often cause an excessive and unacceptable overhead in terms of power consumption and area.

Since the intensity of cosmic rays is not constant but may vary over several magnitudes depending on the solar activity, a worst-case radiation protection is far too expensive in most cases. A self-adaptive system is proposed in [13], which monitors the current SEU rate and exploits the opportunity of partial reconfiguration of FPGAs to implement redundancy such as TMR on demand.

III. Comparison of *Virtex-5QV* vs. *Kintex-7*

As space-grade FPGA, we chose the *Xilinx Virtex-5QV* series, which is also used in the FOBP. The *Virtex-5QV* series

TABLE I: Overview of the *Virtex-5QV* and *Kintex-7* series with the used *XC7K325T*.

	Virtex-5QV	*Kintex-7* (*XC7K325T*)
Technology	65 nm, copper CMOS	28 nm, copper CMOS
Maximum clocking	up to 450 MHz	up to 741 MHz
Resources factor	1	0.5 ... 3.7 (2.5)
Power consumption (high-speed ref. design)	28 W	7 W ... 12 W (12 W)
Radiation hardening	12T-SRAM-cell, TMR configuration controller, SET filter option, epitaxial layer, lid	no hardening
Design tool	*ISE* (13.2 fix)	*ISE* (update-capable) and *Vivado* (update-capable)

includes only one FPGA type, the XQR5VFX130. On the other hand, the *Xilinx Kintex-7* series, which is a suitable choice for the non-hardened FPGA, comes with seven different FPGA devices. In this paper, we choose the KC7K325T for the analyses. Tab. I provides a short comparison of both FPGA series in general and especially for the used KC7K325T (see values in brackets).

An important issue of the comparison is the amount of provided resources. The resource range of the *Kintex-7* series reaches from 0.5 up to 3.7, compared to the *Virtex-5QV*. Furthermore, the *Kintex-7* series allows a higher maximum clocking frequency, due to advanced technology and architecture. Also, the power consumption (example is calculated with a high-speed reference design) is reduced because of the smaller process technology.

Beside these advantages of the *Kintex-7* series, the disadvantage arises when the FPGA shall be used for space application. The *Virtex-5QV* uses radiation hardening techniques on the hardware and package level. These special techniques to increase the reliability are: 12-transistor SRAM cells for the configuration memory and latches, TMR for the configuration controller, a single event transient (SET) filter option for the configuration logic blocks (CLBs), an epitaxial layer and a protective lid. This results in a higher total ionizing dose (TID) immunity against single event latchups (SELs) and robustness against other SEEs in contrast to the *Kintex-7* series without any hardening techniques. Nevertheless, the radiation hardening of the *Virtex-5QV* comes at the price of higher power consumption in comparison to the COTS equivalent.

A further advantage to motivate the usage of a *Kintex-7* FPGA is the availability of improved design tools. On one hand, the design tools for the *Virtex-5QV* are limited to *Xilinx Integrated Software Environment (ISE) 13.2*. Newer design tools and thereby updates are not supported. The frontend synthesis (netlist generation) can also be done using alternative tools (e.g. *Synplify* from *Synopsis*), but the backend (implementation: translate, map, place and route) requires *ISE 13.2* caused by the necessary *Virtex-5QV* overlay. On the other hand, the *Kintex-7* series profits from the new design tools (*Xilinx Vivado*) and updates. This allows a more flexible usage of sophisticated design tools with possible improvements through the *Xilinx* support.

Note, that a substantial effort is needed to harden and validate the design of a COTS in contrast to space-grade FPGA. This is application and design depended. In general, the design and validation efforts are lower for the space-grade device as several problems are resolved by the device itself and are no longer under the responsibility of the designer.

A. Radiation Analysis

Total ionizing dose (TID) is one main degrading radiation caused effect of silicon-based devices in space. The TID tolerance of the *Virtex-5QV* is at least 1000 krad. Unfortunately, TID figures of the *Kintex-7* are not published yet. A very simple and effective mitigation of TID caused degrading of a device is the increase (a few mm) of the metal shielding surrounding the FPGA that results in a higher weight, too. [14]

The other main degrading effect, which cannot be mitigated by increased shielding, are single event effects (SEEs). The *European Cooperation for Space Standardization* (ECSS) divides SEE into the group of temporary (soft) and permanent (hard) faults [15]. The main concerns are permanent faults such as single event latchups (SELs) and single event snapbacks (SESs). SELs and SESs are covered by the radiation-hardened technology of the *Virtex-5QV* but not in the *Kintex-7* [16]. Therefore, we focus on the permanent SEEs in the *Kintex-7* as well as temporary SEEs for both types of FPGAs. In this section, we discuss current-step SELs, single event functional interrupts (SEFIs), single event upsets of the configuration RAM (CRAM) and SEUs in general.

We use the *Weibull* parameters of the *Virtex-5QV* [16], the *Weibull* parameters of the *Kintex-7* [17], the characterization of the orbit as GEO of the *Heinrich Hertz* satellite mission as well as the shielding of 7 mm aluminum (6.5 mm due to box shielding and additional 0.5 mm due to the satellite *Kapton* envelope) of the FOBP as input of our upset rate calculation. Note that the *Weibull* parameters reported for the *Kintex-7* [17] are statistically inaccurate (may alter by an order of magnitude), caused by the small existing amount of radiation test data. So far, only heavy ion radiation data are published of the *Kintex-7*, which lead us to some assumptions in Subsection V-D. We processed all inputs with the CREME96 tool [18]. For a detailed description of the upset rate calculation, see [13].

In Tab. II and Fig. 1, we depict the results of our upset rate calculation. Even the (maybe destructive) current-step SEL upset rate of the *Kintex-7* (no SEFI data available) is more than two orders of magnitude higher than the temporary SEFI upset rate of the *Virtex-5QV* configuration controller. We discuss this critical current-step SEL in the next subsection. The flip flop (FF) and the Block RAM (BRAM, in the radiation test mode without an error correcting code) heavy ion upset rate of both FPGAs are in the same range. The FFs of the *Virtex-5QV* are implemented with master-slave dual-node cells and are very hard to direct hits [16]. Most probably the smaller overall semiconductor area of the *Kintex-7* compensates the smaller cells (caused by the smaller process), which are more sensitive to lower particle energies.

The upset rates of the CRAM differ in three orders of magnitude, due to the fact that the CRAM of the *Virtex-5QV* is based on a 12-transistor SRAM cell, whereas the *Kintex-7* uses only a 6-transistor SRAM cell. This property of the space-grade FPGA is important to distinguish (without complex analysis) between upsets in the different primitives. In contrast to radiation-hardened FPGAs, the CRAM SEUs are dominant in non-hardened FPGAs. In other words, the configuration memory of the space-grade FPGA is more reliable.

B. Current-Step Single Event Latchup of the Kintex-7

Because of their high energy, only heavy ions may cause current-step SELs that are classified as permanent faults. The upset rate of the current-step SEL is low but not negligible

TABLE II: Overall upset rates λ_{prim} of the *Virtex-5QV* and heavy ion (HI) upset rate only of the *Kintex-7* (XC7K325T) in GEO with a 7 mm aluminum shielding according to CREME96.

Device: Primitive (prim)	Count	*Solar Min.*	*Solar Max.*	*Worst Week*	*Worst Day*	*Peak 5 Minutes*
	$n_{\mathrm{device,prim}}$	λ_{prim} in $upsets/day/device$				
V-5QV: CRAM	34,087,072 Bit	$1.75 \cdot 10^{-03}$	$3.35 \cdot 10^{-04}$	$6.04 \cdot 10^{-02}$	$1.46 \cdot 10^{-01}$	$5.27 \cdot 10^{-01}$
V-5QV: BRAM Primitive 512×72 Bit	298	$3.44 \cdot 10^{+00}$	$1.11 \cdot 10^{+00}$	$2.33 \cdot 10^{+02}$	$8.58 \cdot 10^{+02}$	$3.12 \cdot 10^{+03}$
V-5QV: FF SET Filter off	81,920	$3.02 \cdot 10^{-03}$	$7.42 \cdot 10^{-04}$	$1.53 \cdot 10^{-01}$	$4.92 \cdot 10^{-01}$	$1.79 \cdot 10^{+00}$
V-5QV: FF SET Filter on	81,920	$1.06 \cdot 10^{-04}$	$2.06 \cdot 10^{-05}$	$9.91 \cdot 10^{-03}$	$3.35 \cdot 10^{-02}$	$1.22 \cdot 10^{-01}$
V-5QV: DSP M-Register	320	$1.22 \cdot 10^{-01}$	$4.34 \cdot 10^{-02}$	$8.75 \cdot 10^{+01}$	$3.26 \cdot 10^{+02}$	$1.18 \cdot 10^{+03}$
V-5QV: DSP other Register	1,280	$2.70 \cdot 10^{-01}$	$9.60 \cdot 10^{-02}$	$1.92 \cdot 10^{+02}$	$7.13 \cdot 10^{+02}$	$2.59 \cdot 10^{+03}$
V-5QV: Configuration Controller	4	$3.51 \cdot 10^{-07}$	$9.89 \cdot 10^{-08}$	$3.57 \cdot 10^{-05}$	$1.25 \cdot 10^{-04}$	$4.56 \cdot 10^{-04}$
K-7 HI: CRAM	75,202,176 Bit	$8.96 \cdot 10^{-01}$	$1.84 \cdot 10^{-01}$	$1.92 \cdot 10^{+01}$	$4.23 \cdot 10^{+01}$	$1.53 \cdot 10^{+02}$
K-7 HI: BRAM Primitive 512×72 Bit	445	$3.93 \cdot 10^{+00}$	$1.37 \cdot 10^{+00}$	$6.43 \cdot 10^{+01}$	$1.96 \cdot 10^{+02}$	$7.15 \cdot 10^{+02}$
K-7 HI: FF	407,600	$4.40 \cdot 10^{-03}$	$1.18 \cdot 10^{-03}$	$9.31 \cdot 10^{-02}$	$2.38 \cdot 10^{-01}$	$8.66 \cdot 10^{-01}$
K-7 HI: FF Slice Rst	50,950	$1.39 \cdot 10^{-03}$	$3.89 \cdot 10^{-04}$	$2.63 \cdot 10^{-02}$	$6.76 \cdot 10^{-02}$	$2.45 \cdot 10^{-01}$
K-7 HI: Misc. - Current-Step SEL	1	$7.48 \cdot 10^{-05}$	$2.14 \cdot 10^{-05}$	$1.80 \cdot 10^{-03}$	$5.46 \cdot 10^{-03}$	$1.99 \cdot 10^{-02}$

(see Tab. II). The probability of occurrence of such a current-step SEL for our 15-year mission is 65 % (assuming only one reference solar particle event per year). This results in a probability of $8.1 \cdot 10^{-6}$ failures per hour compared to the SEFIs (temporary faults) of the *Virtex-5QV* with $5.2 \cdot 10^{-8}$.

Current-step SELs arise only at the auxiliary voltage of the power supply VCC_{aux}. This voltage powers: Configuration module, eFUSE programming, XADC (also know as system monitor), I/O pin optional functions and more. The nominal voltage of VCC_{aux} is 1.8 V and the nominal current is design dependent from below 100 mA to a few 100 mA with a dynamic variance of a few 10 mA.

Heavy ion induced current steps occur at this VCC_{aux} voltage with a distribution of 105 mA in average (25 mA standard deviation) at ambient temperature and 125 mA in average (40 mA standard deviation) at elevated temperature (above 90 °C). During the radiation test, no functional errors were observed and a power cycle restored the nominal current. The phenomena of these current steps are not completely understood. It is possible as well that these current steps are SESs. Additional tests are planned by the *Xilinx Radiation Test Consortium* (XRTC) to clarify the phenomena of VCC_{aux} current steps. [1]

Proving that these current steps are non-destructive is very difficult. For a reliable space design, a detection and mitigation of current steps is mandatory. An external reliable device could monitor the current of VCC_{aux} and power cycle the FPGA if necessary. The FPGA itself can also perform this task, if the current-step detection (XADC powered by VCC_{aux}) and the reset logic design are reliable and tested with a heavy ion accelerator.

IV. Reliability Model

The probability that an SEU in the FPGA leads to a failure of a module m obviously depends on the number of resources utilized by the module, e.g., the number of configuration bits $n_{\mathrm{e,cfg}}$, which are commonly referred to as *essential* or *sensitive* bits. This number may be determined by either fault injection tests [19], [20] or by tools provided by the FPGA vendor [21]. Furthermore, the number of used flip flops $n_{\mathrm{e,ff}}$, BRAMs $n_{\mathrm{e,bram}}$, and digital signal processing (DSP) slices $n_{\mathrm{e,dsp}}$ can be obtained from the placement report. In the following, we assume that the corruption of each single *essential* bit, used flip flop, or DSP slice may lead to a module failure if module m is not replicated. We consider further a BRAM protection by using error correcting codes. With this assumption, the module failure rate $\lambda_{\mathrm{M}}(m)$ can be estimated by

$$\lambda_{\mathrm{M,prim}}(m) = \lambda_{\mathrm{prim}} \cdot \frac{n_{\mathrm{e,prim}}(m)}{n_{\mathrm{device,prim}}} \tag{1}$$

$$\lambda_{\mathrm{M}}(m) = \sum_{\mathrm{prim}} \lambda_{\mathrm{M,prim}}(m) \tag{2}$$

where $n_{\mathrm{e,prim}}$ denotes to the number of used resources of type $\mathrm{prim} \in \{\mathrm{cfg}, \mathrm{ff}, \mathrm{bram}, \mathrm{dsp}\}$, e.g., the number of *essential* bits $n_{\mathrm{e,cfg}}$ of module m, and $n_{\mathrm{device,prim}}$ denotes the overall number of resources of type prim of the FPGA. With the module failure rate given by Eq. (2), we assume the reliability of each module to decrease exponentially over time t, which is expressed by the module reliability function $R_{\mathrm{M}}(m,t)$ with

$$R_{\mathrm{M}}(m,t) = e^{-\lambda_{\mathrm{M}}(m) \cdot t}. \tag{3}$$

The reliability $R_{\mathrm{M}}(m,t)$ of module m at time t denotes the probability that module m operates without any failure in the interval $[0,t]$. Using Eq. (3), the probability of failures per hour (PFH) of module m may then be calculated as

$$\mathrm{PFH}(m) = 1 - R_{\mathrm{M}}(m, T_{\mathrm{h}}) \quad \text{with} \quad T_{\mathrm{h}} = 3600 \text{ s}. \tag{4}$$

In order to achieve higher module reliability, respectively a smaller PFH for a given SEU rate λ_{prim}, a technique known as *majority voting* can be employed where the results of all n replicas are compared. The reliability function $R_{\mathrm{NMR}}(k,n,m,t)$ of such a *k-out-of-n* system is given as follows, if $k \geq \lfloor \frac{n}{2} + 1 \rfloor$:

$$R_{\mathrm{NMR}}(k,n,m,t) = \sum_{i=k}^{n} \binom{n}{i} \big(R_{\mathrm{M}}(m,t)\big)^{i} \cdot \big(1 - R_{\mathrm{M}}(m,t)\big)^{n-i} \tag{5}$$

In case of $k < \lfloor \frac{n}{2} + 1 \rfloor$, the voter only needs a relative majority in order to decide for the correct result. However, the probability that some equal false results might overrule the voter or lead to a situation where the voter is unable to decide the right results must be considered. This depends highly on the distribution of wrong results. We consider an equal distribution of wrong results on the erroneous modules. Therefore, the probability that i erroneous values are identical

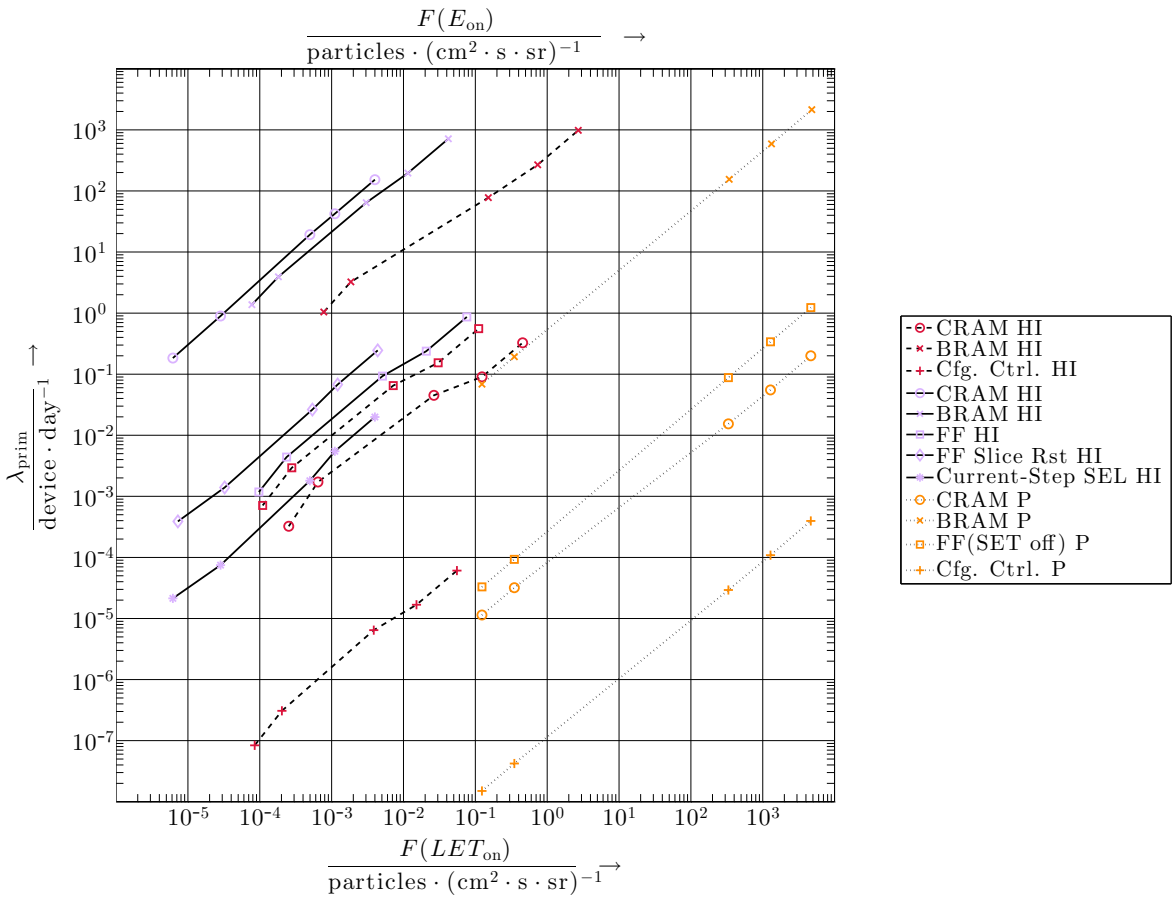

Fig. 1: Heavy ion (HI) upset rate as function of the integral flux $F(LET_{\text{on}})$ for *Kintex-7* (XC7K325T, purple marker and solid line) and *Virtex-5QV* (red marker) as well as proton (P) upset rate as function of the integral flux $F(E_{\text{on}})$ *Virtex-5QV* only (orange marker) for selected FPGA primitives in GEO and 7 mm Al shielding. The markers of all curves from left to right represents the upset rate at the onset of the *Solar Maximum*, *Solar Minimum*, *Worst Week*, *Worst Day* and *Peak 5 Minutes* condition.

is $\frac{2^b}{2^{bi}}$, where b is the word length in bits. The reliability of such a relative majority system can be calculated with:

$$R_{\text{NMR}}(k,n,m,t) = \sum_{i=k}^{n} \binom{n}{i} \left(R_{\text{M}}(m,t)\right)^i \cdot \left(1-R_{\text{M}}(m,t)\right)^{n-i}$$

$$- \sum_{i=k}^{\lfloor \frac{n}{2} \rfloor} \binom{n}{i} \left(R_{\text{M}}(m,t)\right)^i \cdot \left(1-R_{\text{M}}(m,t)\right)^{n-i} \cdot \frac{2^{b(m)}-1}{2^{b(m)\cdot i}} \quad (6)$$

Note that the -1 in the last fraction considers the case that the output of each erroneous module have the correct value by chance.

This reliability model assumes that SEUs cause permanent faults in the corresponding resources, which is true for the configuration memory without scrubbing. However, SEUs on flip flops and DSP slices may corrupt the module output only for few clock cycles if the error cannot manifest in the module, e.g., by using feedback paths. Therefore, we define an error time $t_{\text{err,prim}}$ for each resource. This error time denotes to the maximum time period which an SEU on a given resource may affect the output of the corresponding module. The average failure rate $\lambda_{\text{NMR,prim}}$ within this time period $t_{\text{err,prim}}$ for a replicated module can be estimated according to [20] for a given resource by

$$\lambda_{\text{NMR,prim}}(k,n,m) = \frac{1 - R_{\text{NMR,prim}}(k,n,m,t_{\text{err,prim}})}{t_{\text{err,prim}}}. \quad (7)$$

For calculating $R_{\text{NMR,prim}}$, only the corresponding $\lambda_{\text{M,prim}}$ is used in Eq. (3).

In the following, we assume the configuration memory to be scrubbed periodically with scrub cycle t_s. Then the average failure rate $\lambda_{\text{NMR,cfg}}$ within a scrub cycle for a replicated module can be estimated according to Eq. (7) by setting $t_{err,cfg}$ to t_s. The overall failure rate λ_{NMR} of the replicated module m can now be estimated by

$$\lambda_{\text{NMR}}(k,n,m) = \sum_{\text{prim}} \lambda_{\text{NMR,prim}}(k,n,m). \quad (8)$$

Using Eq. (7) and Eq. (3), the reliability function $R_{\text{NMR,s}}$ for NMR with scrubbing can be finally calculated as follows:

$$R_{\text{NMR,s}}(k,n,m,t) = e^{-\lambda_{\text{NMR}}(k,n,m)\cdot t} \quad (9)$$

The value of $\text{PFH}_{\text{NMR,s}}$ may be calculated analog to Eq (4).

In order to analyze the reliability of a complex design including a data path with a module stages, we consider three cases: Case 1 considers only a single voter v at the end of the

Fig. 2: Schematic overview of the receiver chain with the three sub modules: demodulator (demapper), deinterleaver and LDPC decoder.

module chain, whereas in Case 2 and 3, the outputs of every module stage are voted with a corresponding voter v_i. A single voter does this in Case 2 and the voter output is spread to all n_{i+1} inputs of the following stage $i+1$. In Case 3, this is done by replicating also the voters to the number of replicated modules n_{i+1} of the following stage $i+1$.

The system-level reliability function of Case 1 can be described as follows:

$$R_{\text{sys}}(t) = R_{\text{NMR,s}}(k, n, m_1 \circ m_2 \circ \cdots \circ m_a, t) \cdot R_{\text{M}}(v, t) \tag{10}$$

where $R_{\text{M}}(m_1 \circ m_2, t) = R_{\text{M}}(m_1, t) \cdot R_{\text{M}}(m_2, t)$. According to [22], the following equation can be used for Case 2:

$$R_{\text{sys}}(t) = \prod_{i=1}^{a} R_{\text{NMR,s}}(k_i, n_i, m_i, t) \cdot R_{\text{M}}(v_i, t) \tag{11}$$

Finally, the reliability of Case 3 can be evaluated as follows [22]:

$$\begin{aligned} R_{\text{sys}}(t) = & R_{\text{NMR,s}}(k_1, n_1, m_1, t) \cdot R_{\text{M}}(v_a, t) \cdot \\ & \prod_{i=2}^{a} R_{\text{NMR,s}}(k_i, n_i, v_{i-1} \circ m_i, t) \end{aligned} \tag{12}$$

V. Evaluation

In this section, we apply the above analysis results to a real application consisting of a receiver chain and different voter structures, quantitatively.

A. Receiver Design

We examine a real communication receiver design and determine the reliability of both FPGA types for space missions. The design is transferred between the *Kintex-7* and *Virtex-5QV* FPGA. This allows a comparison of the results. Sec. V-B describes the different configurations for NMR. This results in the requirement for the receiver design, which shall fit at least three times (for TMR, $N = 3$) into the *Virtex-5QV*. Fig. 2 shows the signal processing chain and the modules of the receiver design. Each module includes a 16-bit input and output vector ($b = 16$).

First, the demodulator processes a digital input signal. This includes a frequency conversion (down sampling), filtering, and demapping of a Quadrature Phase-Shift Keying (QPSK) modulation. The deinterleaver follows the demodulator and is realized as block-deinterleaver. It is parameterizable and includes a RAM and a FIFO to buffer data. A Low-Density-Parity-Check (LDPC) decoder supplements the receiver chain. To complete the receiver, time and frequency synchronization is necessary. Because of the resource limitation of the FPGA, we have not implemented these features. This may be done in a second FPGA.

A configuration memory scrubber is essential for an SRAM-based FPGA, since it increases its availability. We realize this scrubber as an external component (other FPGA) or with the soft error mitigation core [21] from *Xilinx*. We do not consider resources needed to implement the scrubber in this evaluation.

B. Voter Design

In contrast to TMR voters using tri-state buffers (BUFTs) [23], the voters developed for this approach are designed to vote on 16-bit words and are implemented using look-up tables (LUTs). We decided to utilize LUTs in order to be able to generate an error signal indicating which incoming data differs from the majority and therefore indicate the part of the FPGA that should be scrubbed. This LUT-based design also allows us to build more advanced voters, which could find a higher number of correct solutions. As an example, a *2-out-of-4* voter can be created, which still finds a valid solution in the case that two inputs are equal and correct, and the remaining ones differ. A schematic overview of such a *2-out-of-4* voter is depicted in Fig. 3. Note that the multiplexer only selects between the first $n-1$ inputs. It is not necessary to forward the last input in case it is part of the majority, there is an equal signal on one of the inputs 0 to $n-1$.

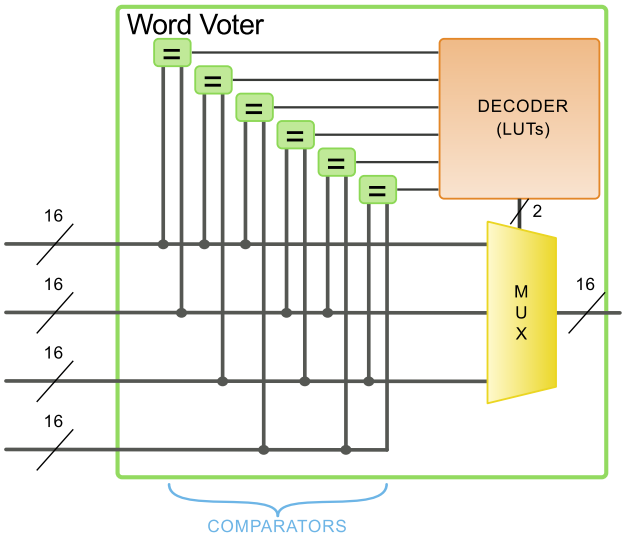

Fig. 3: Schematic overview of an NMR voter with four inputs. First, each pair of two inputs is compared. The results of the comparators are then fed into multiple LUTs to generate the select signal controlling the multiplexer that selects which input to forward.

Our voters are generated by a program creating VHDL code allowing us to create N-channel voters implementing different majority strategies like *3-out-of-4* ($k = 3$, $n = 4$) or *2-out-of-4* ($k = 2$, $n = 4$). Therefore, all voters are built in the same way. After the comparator stage where each pair of two inputs is compared, each result is fed into one or more LUTs. Depending on their content, the voting function is realized and the select signal for the multiplexer is generated.

As LUT-based voters consume more slices, and therefore, are more prone to errors themselves, we also investigate the use of redundant voter configurations (Case 3 in Section IV).

In Subsection V-A, we already introduced the receiver chain and the three modules building the receiver were depicted. Different redundancy configurations can be implemented with this receiver chain. The syntax describing each

analyzed configuration is defined as follows: n_m x n_v, where n_m is the number of replicas of module m and n_v is the number of voters v used to vote the results of these replicas. More modules are concatenated by using - as separator.

Fig. 4 depicts such a kind of configuration using redundant voters after the *Demodulator* and after the *Deinterleaver*. In this configuration, the outputs of the LDPC Decoder will be sent to FPGA output pins. We assume that if more then one output is generated, an ideal hardware voter outside the FPGA is present.

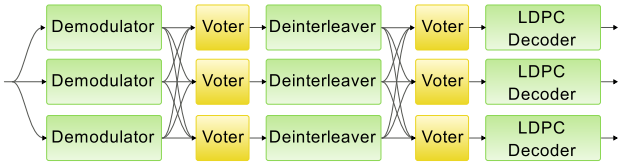

Fig. 4: Schematic overview of a 3x3-3x3-3x0 redundancy configuration. Besides the last tripled part of the receiver chain, the outputs are individually voted and fed into the next part. In this configuration, three outputs are generated and will be voted outside the FPGA.

The following configurations are analyzed in the reliability analysis below (for Case 1 to 3, refer to Section IV):

- *Virtex-5QV* and *Kintex-7*:
  - 1x0-1x0-1x0 (No Redundancy, noR)
  - 3x0-3x0-3x1 (TMR, Case 1)
  - 3x1-3x1-3x1 (TMR, Case 2)
  - 3x3-3x3-3x0 (TMR + TMR-voter, Case 3)
- *Kintex-7* only:
  - 4x3-3x4-4x0 (NMR, Case 3)
  - 6x5-5x4-4x0 (NMR, Case 3)

The first configuration uses no redundancy at all. To evaluate the reliability of each redundancy approach, each configurations introduces more or finer grained redundancy. At last, maximum redundancy, meaning all available resources where used to raise the level of redundancy, is implemented.

C. Implementation Results

The receiver design in Sec. V-A offers a good trade-off between the different FPGA primitives: LUTs, FF, DSP-Slices and BRAM. These primitives are roughly uniformly distributed and are used in typical satellite communication applications. The aimed system clock for the receiver chain is 51 MHz. The design shall be implemented without timing errors on both FPGAs. We use *Xilinx ISE 13.2* (respectively *PlanAhead*) for the *Virtex-5QV* implementation and the *Xilinx* tool *Vivado2014.4* for the *Kintex-7* implementation. An advantage of the *Xilinx* 7-series design tools is the faster implementation time. Netlist synthesis and backend implementation require about 14 min (3x3-3x3-3x0 configuration without IP core generation time). In comparison, the implementation time for the *Virtex-5QV* results in about 104 min.

We use physical constraining for the implementation to ensure one module is implemented only in a designated partition. This constraining protects the different modules against module-overlapping multiple bit upsets (MBUs) of the FPGAs. Tab. III summarizes the resources and the essential bits n_e for the different configurations, defined in Sec. V-B, for both FPGAs.

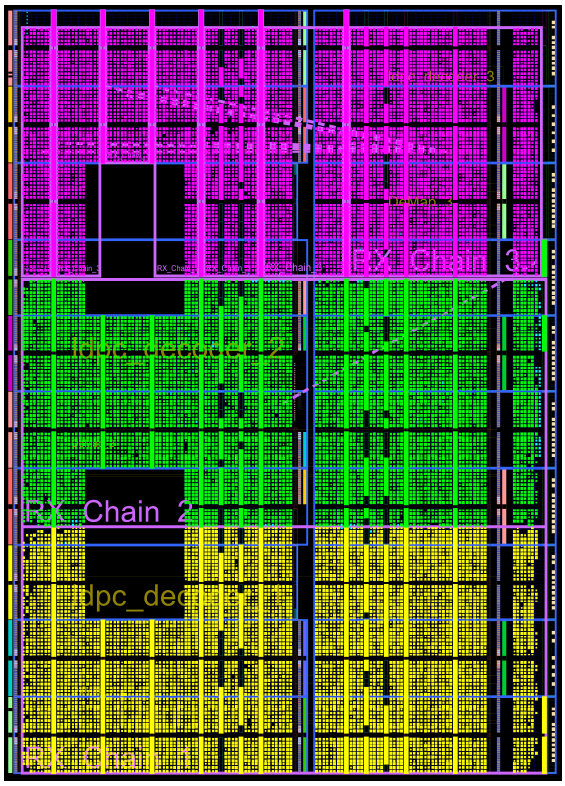

Fig. 5: Implementation results of *PlanAhead* for the 3x3-3x3-3x0 configuration on *Virtex-5QV* according to Fig. 4. Each color represents one receiver chain in a defined partition requiring roughly 30 % of the FPGA resources.

In our case study, *Vivado* generated comprehensible and deterministic results even without physical constraining. The ISE tool generates less then 3 times the essential bits n_e and LUTs of the noR configuration compared to the TMR configurations, which differs from the expectation. All types of primitives are used and are more or less uniformly distributed. The implementation of the *Kintex-7* with *Vivado* uses less DSP48 resources. *Vivado* truncates unused bits and implements multiplications of operands with a just a few bits in LUTs which saves DSP48 resources. Note the high resource consumption (over 90 %) of the LUTs and BRAMs in the *Virtex-5QV* (see Tab. III).

Fig. 5 gives an impression for the utilization of the TMR 3x3-3x3-3x0 configuration of the *Virtex-5QV* FPGA. Each color of the *PlanAhead* result represents one receiver chain, implemented in a defined partition with approximately 30 % FPGA resources.

D. Reliability Analysis

Finally, we compare the space-grade *Virtex-5QV* and the *Kintex-7* regarding the reliability of the implemented case study. The implementation results of Sec. V-C are used to calculate the reliability based on the FPGA upset rates of Tab. II. To ensure a suitable comparison we made the following decisions and assumptions for the reliability calculation:

- *Virtex-5QV*:
  - Upset rate for FF with SET Filter on
- *Kintex-7*:

TABLE III: Results of the resource utilization and the number of essential bits of different configurations. Comparison: no Redundancy (noR), TMR and NMR with different voter configurations for the *Virtex-5QV* and the *Kintex-7*.

Configuration	LUTs	FFs	DSP48	BRAMs	n_e
V-5QV Available	81920	81920	320	298	34087072
V-5QV 1x0-1x0-1x0 (noR)	25535 (31.2 %)	13143 (16 %)	69 (21.6 %)	98 (32.9 %)	6208083 (18.2 %)
V-5QV 3x0-3x0-3x1	74713 (91.2 %)	39430 (48.1 %)	207 (64.7 %)	294 (98.7 %)	17578928 (51.6 %)
V-5QV 3x1-3x1-3x1	74791 (91.3 %)	39448 (48.2 %)	207 (64.7 %)	294 (98.7 %)	17611037 (51.7 %)
V-5QV 3x3-3x3-3x0	74927 (91.5 %)	39448 (48.2 %)	207 (64.7 %)	294 (98.7 %)	17697499 (51.9 %)
K-7 Available	203800	407600	840	445	75202176
K-7 1x0-1x0-1x0 (noR)	23112 (11.3 %)	14054 (3.45 %)	33 (3.93 %)	97.5 (21.9 %)	4738905 (6.3 %)
K-7 3x0-3x0-3x1	69460 (34.1 %)	42092 (10.3 %)	99 (11.8 %)	292.5 (65.7 %)	14115492 (18.8 %)
K-7 3x1-3x1-3x1	69507 (34.1 %)	42092 (10.3 %)	99 (11.8 %)	292.5 (65.7 %)	14134446 (18.8 %)
K-7 3x3-3x3-3x0	69626 (34.2 %)	42092 (10.3 %)	99 (11.8 %)	292.5 (65.7 %)	14170356 (18.8 %)
K-7 4x3-3x4-4x0	92511 (45.4 %)	55831 (13.7 %)	132 (15.7 %)	373 (83.8 %)	18973264 (25.2 %)
K-7 6x5-5x4-4x0	106928 (52.5 %)	67633 (16.6 %)	198 (23.6 %)	407 (91.5 %)	21996559 (29.2 %)

  - DSP data upset rate equals to *Virtex-5QV*
  - Double heavy ion upset rates (no proton data available)

- *Virtex-5QV* and *Kintex-7*:
  - Whole BRAM with ECC protection correspond to 300 unmitigated bits
  - No explicit BRAM scrubbing (user task)
  - No DSP correction because of streaming and FIR filter
  - $t_s = 60\,\mathrm{s}$
  - $t_{\mathrm{err,ff}} = t_{\mathrm{err,bram}} = 60\,\mathrm{s}$
  - $t_{\mathrm{err,dsp}} = 2.7\,\mu\mathrm{s}$

The DSP and BRAM of the *Virtex-5QV* are not hardened and the heavy ion upset rates for BRAM and FFs resemble. Due to this fact, we are able to assume the DSP upset rate data of the *Virtex-5QV* for the *Kintex-7* DSPs (scaled to the quantity) as well. For all other upset rates, we assume a double heavy ion upset rate for the *Kintex-7* because there is no proton data available for this device (assumption with respect to the behavior of the *Virtex-5QV*). Furthermore, we use BRAM ECC, which results in 300 unmitigated bits corresponding to all BRAM bits [24]. This reduces the impact of the unprotected BRAM (see upset rate in Tab. II). BRAM memory scrubbing is necessary while using BRAM with ECC because the ECC only corrects the data at the output and not in the BRAM cell. The BRAM scrubbing can be done within the regular processing by updating the data. The user has to take care of the BRAM size and BRAM update rate respectively the error time. Otherwise, a BRAM memory scrubbing with additional hardware must be implemented (see BRAM scrubber in [13]). In general, current steps and SEFIs (configuration controller upsets) are design independent and therefore not considered. The receiver of Sec. V-A is designed only with finite impulse response (FIR) filters using DSPs. In combination with streaming processing the manifestation of errors due to feedback paths is prohibited.

The PFH value is a suitable qualifier to evaluate the reliability. For its calculation, we use the equations of Section IV, which also considers TMR with scrubbing. We distinguish between the scrubbing time $t_s = 60\,\mathrm{s}$ of the CRAM and the error time $t_{\mathrm{err,prim}}$ of the BRAM, FFs and DSPs. The error time $t_{\mathrm{err,prim}}$, which indicates that an error is shifted out of the module in this time, of the FFs and BRAMs is as well 60 s. The error time $t_{\mathrm{err,prim}}$ for the DSPs (only streaming processing in FIR filter), which is 2 times (input and output register) the maximum DSP slices per module in series (69) with a clock at 51 MHz, results in 2.7 µs.

With each upset rate for each resource type according to Eq. (1), we apply NMR for the corresponding configurations using Eq. (5) and Eq. (6). We include the error time $t_{\mathrm{err,prim}}$ according to Eq. (7) and sum it up with Eq. (8). These user design upset rate for each solar condition will be used to calculate the reliability $R_m(t)$ using Eq. (9) and the PFH using Eq. (4). Tab. IV shows the PFH values for the different configurations according to Eq. (10) - (12).

Because of the higher resource utilization (especially DSPs), the noR design PFH of the *Virtex-5QV* without redundancy is worse than in the *Kintex-7*. In the TMR configurations, the *Virtex-5QV* achieves a better PFH factor from 147 to 35,783 compared to the *Kintex-7*, because here, the CRAM upset rate is dominating. As expected, the TMR configuration 3x3-3x3-3x0 with triplicated voter and an external voter delivers the best reliability among all TMR configurations. The higher order NMR schemes 4x3-3x4-4x0 and 6x5-5x4-4x0 of the *Kintex-7* improve the PFH factor form 122 to 1,836 respectively from 135 to 27,586 compare to the most reliable *Kintex-7* TMR configuration (3x3-3x3-3x0). The obtained PFH values of the two higher order NMR scheme configurations differs only marginally in the *Peak 5 Minutes* condition, because the upset rate of the last module (LDPC decoder) is dominant and the number of replicas of this module is not changed.

VI. Conclusion

In our comparison of SRAM-based FPGAs for harsh radiations environments, we considered the space-grade and radiation-hardened by design *Virtex-5QV* (XQR5VFX130) and a COTS *Kintex-7* (KC7K325T) from *Xilinx*. Advantages and drawbacks of both families were discussed. We analyzed and calculated the radiation effect upset rates for a GEO satellite mission. N-modular redundancy schemes with different voter and segmentation were applied to a communication receiver FPGA design.

If a high-reliable external voter is an option, we suggest the 3x3-3x3-3x0 configuration for both types of FPGAs or a higher order NMR for the COTS FPGA. The 4x3-3x4-4x0 configuration offers a good reliability to resource trade-off for the *Kintex-7*. In most cases, this external voter is, however, difficult to implement. For the case that the usage of an external voter is not possible, we suggest the 3x0-3x0-3x1 configuration.

Also, we have shown that a *Virtex-5QV* in the triple modular redundancy configuration 3x0-3x0-3x1 without an

TABLE IV: Reliability results for the *Virtex-5QV* and the *Kintex-7*. Values for the probability of failures per hour (PFH) for different configurations and solar conditions.

Configuration	PFH_{sys} *Solar Min.*	PFH_{sys} *Solar Max.*	PFH_{sys} *Worst Week*	PFH_{sys} *Worst Day*	PFH_{sys} *Peak 5 Minutes*
V-5QV 1x0-1x0-1x0 (noR)	$3.53 \cdot 10^{-03}$	$1.25 \cdot 10^{-03}$	$9.19 \cdot 10^{-01}$	$1.00 \cdot 10^{+00}$	$1.00 \cdot 10^{+00}$
V-5QV 3x0-3x0-3x1	$1.70 \cdot 10^{-08}$	$3.27 \cdot 10^{-09}$	$3.10 \cdot 10^{-07}$	$2.14 \cdot 10^{-06}$	$9.18 \cdot 10^{-06}$
V-5QV 3x1-3x1-3x1	$5.11 \cdot 10^{-08}$	$9.80 \cdot 10^{-09}$	$1.48 \cdot 10^{-06}$	$4.94 \cdot 10^{-06}$	$1.89 \cdot 10^{-05}$
V-5QV 3x3-3x3-3x0	$7.51 \cdot 10^{-12}$	$3.13 \cdot 10^{-13}$	$1.20 \cdot 10^{-08}$	$3.83 \cdot 10^{-07}$	$3.81 \cdot 10^{-06}$
K-7 1x0-1x0-1x0 (noR)	$4.65 \cdot 10^{-03}$	$1.21 \cdot 10^{-03}$	$7.17 \cdot 10^{-01}$	$9.90 \cdot 10^{-01}$	$1.00 \cdot 10^{+00}$
K-7 3x0-3x0-3x1	$4.41 \cdot 10^{-06}$	$4.76 \cdot 10^{-07}$	$2.81 \cdot 10^{-04}$	$1.15 \cdot 10^{-03}$	$1.32 \cdot 10^{-02}$
K-7 3x1-3x1-3x1	$1.16 \cdot 10^{-05}$	$1.98 \cdot 10^{-06}$	$3.58 \cdot 10^{-04}$	$1.11 \cdot 10^{-03}$	$9.46 \cdot 10^{-03}$
K-7 3x3-3x3-3x0	$2.65 \cdot 10^{-07}$	$1.12 \cdot 10^{-08}$	$1.22 \cdot 10^{-04}$	$5.88 \cdot 10^{-04}$	$7.59 \cdot 10^{-03}$
K-7 4x3-3x4-4x0	$1.53 \cdot 10^{-10}$	$6.10 \cdot 10^{-12}$	$1.82 \cdot 10^{-07}$	$1.56 \cdot 10^{-06}$	$6.24 \cdot 10^{-05}$
K-7 6x5-5x4-4x0	$1.87 \cdot 10^{-11}$	$4.06 \cdot 10^{-13}$	$1.16 \cdot 10^{-07}$	$1.22 \cdot 10^{-06}$	$5.62 \cdot 10^{-05}$

external voter may achieve an equal PFH as the *Kintex-7* in the N-modular redundancy configuration 4x3-3x4-4x0 with an external high-reliable voter.

Note that the current-step SEL is not understood completely and, therefore, the *Kintex-7* is a potential risk for space missions. The presented figures are based on our case study and have to be analyzed individually for other applications.

For future work, we want to verify our redundancy schemes using fault injection. Furthermore, we want to apply adaptive mitigation using our BRAM radiation sensor to these redundancy schemes [13]. In addition, we want to optimize the parameters k, n (*k-out-of-n*) and the number of modules in a chain m for a general applicability.

ACKNOWLEDGMENT

The work has been partially supported by EFRE funding from the *Bavarian Ministry of Economic Affairs* (*Bayerisches Staatsministerium für Wirtschaft, Infrastruktur, Verkehr und Technologie*) as a part of the *ESI Application Center* project.

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