# An Energy-Efficient Quad-Camera Visual System for Autonomous Machines on FPGA Platform

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Abstract—In our past few years' of commercial deployment experiences, we identify localization as a critical task in autonomous machine applications, and a great acceleration target. In this paper, based on the observation that the visual frontend is a major performance and energy consumption bottleneck, we present our design and implementation of an energy-efficient hardware architecture for ORB (Oriented-Fast and Rotated-BRIEF) based localization system on FPGAs. To support our multi-sensor autonomous machine localization system, we present hardware synchronization, frame-multiplexing, and parallelization techniques, which are integrated in our design. Compared to Nvidia TX1 and Intel i7, our FPGA-based implementation achieves  $5.6\times$  and  $3.4\times$  speedup, as well as  $3.0\times$  and  $34.6\times$  power reduction, respectively.

#### I. INTRODUCTION

In the past few years, we have developed and commercialized autonomous machines, such as mobile robots and self-driving cars. During our deployment process, the affordable and reliable *visual frontend* is a critical challenge. With only cameras and IMUs, the visual frontend must precisely perceive the obstacles in unknown environments [1]. An efficient visual system is a prerequisite for localization and exploration tasks.

Autonomous machines are complex cyber-physical systems [2], [3]. Through detailed performance profiling, the visual frontend is the bottleneck and contributes significantly to system end-to-end latency. Based on our profiling result (Sec. II-A) of the localization task, the vision system accounts for 74% processing time and consumes more than 50% CPU resources. Thus, vision frontend is a lucrative acceleration target (Sec. II-B, II-C), especially for edge applications with strict real-time and power constraints.

Several prior works attempt to accelerate visual frontend on low-power platforms. [4] and [5] implement ORB feature extraction and feature matching on FPGA respectively, but they only accelerate part of the visual system. [6] designs an optical-flow based VIO (Visual-Inertial Odometry) on ASIC, but optical-flow may fail in variational illuminations and large motion conditions, limiting its application space. [7] presents an ORB-based visual SLAM (Simultaneous Localization and Mapping) design on FPGA, but it only reports results on low-resolution images. Moreover, all of them have not considered

large-scale 3D visual systems with multiple cameras, which will provide more robust perception but bring much higher compute intensity and design challenges.

In this paper, we present an FPGA-based quad-camera visual system design for reliable and real-time localization, the system has been commercially deployed in multiple markets around the globe. Specifically, four cameras (with 720p resolution) are integrated into one hardware module, and they create a 360-degree panoramic view of the environment. By utilizing hardware synchronizations (Sec. III-A) and framemultiplexing processing techniques (Sec. III-B), the most timeconsuming feature extraction (Sec. III-C) and feature matching (Sec. III-D) are accelerated on FPGA in a fully pipelined way. Our design achieves  $5.63 \times$  and  $3.38 \times$  speedup over Nvidia TX1 and Intel i7 CPU, with 3.03× and 34.63× power reduction, respectively (Sec. IV). It should be noted that visual odometry should never fail in our design since we can always extract 360-degree spatial information from the environment at any moment, and there are always enough overlapping spatial regions between consecutive frames. Moreover, the efficient use of cameras makes our design much more affordable than LiDAR and its computing systems.

The main contributions of this paper are as follows:

- We propose a novel ORB-based quad-camera 3D visual hardware architecture on an FPGA platform to accelerate the computational-intensive localization frontend.
- We present a hardware synchronization scheme to support multi-image channels and IMU for reliable localization.
- We demonstrate how to co-design an accelerator that significantly reduces the latency and energy by exploiting unique frame-multiplexing, parallelisms, and pipelines.

## II. ALGORITHM FRAMEWORK

Hardware design must target critical and compute-intensive blocks. We demonstrate that visual frontend is an universal acceleration target (Sec. II-A), and analyze its two main components, feature extraction (Sec. II-B) and matching (Sec. II-C).

## A. Visual Frontend Profiling

To understand the role of visual frontend, we analyze three popular localization algorithms, SLAM [8], VIO [9] and Registration [10], which are adaptable to different scenarios [11]. As shown in Fig. 1, localization usually consists of a visual

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To appear in IEEE International Conference on Artificial Intelligence Circuits and Systems (AICAS), June 6-9, 2021, Virtual

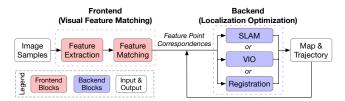


Fig. 1. Overview of localization task, including visual frontend and optimization backend.

TABLE I
LATENCY DISTRIBUTION OF FRONTEND AND BACKEND IN THREE
LOCALIZATION MODES.

	SLAM	VIO	Registration
Frontend	54.8%	86.7%	84.6%
Backend	45.2%	13.3%	15.4%

frontend and an optimization backend. The frontend extracts visual features to find correspondences in observations, while backend estimates the pose and updates the map. All three localization backends share the same ORB-based vision frontend, where ORB has been widely adopted in robotics and it is proven to provide a fast and efficient alternative to SIFT [12].

Tab. I shows the average compute time distribution between the visual frontend and optimization backend of localization systems. We notice that visual frontend is the system bottleneck and its time varies from 54.8% to 86.7% in three modes. Therefore, visual frontend is a lucrative acceleration target. Moreover, since different localization algorithms usually use the same image processing approach, accelerating the frontend would lead to a universal performance improvement.

The visual frontend consists of feature extraction and feature matching stages (Fig. 2). The algorithm details of each stage will be described in Sec. II-B and Sec. II-C, respectively.

#### B. Feature Extraction

We use ORB for feature extraction (Fig. 2). ORB is an efficient fusion of FAST (Feature from Accelerated Segment Test) feature detector and BRIEF (Binary Robust Independent Elementary Features) feature descriptor, describing as follows.

1) Feature Detection: Oriented FAST is used to detect feature points in the image and ensure their rotation invariant. First, the original image is resized to a multi-level image pyramid to enable scale invariance. Second, at each level of the image pyramid, points that differ greatly from the reference point in intensity are detected as feature points. Third, the orientation of feature points is computed as follows.

Assuming the patch of a feature point is the circle centered at itself, the moments of the patch,  $m_{pq}$ , are defined as

$$m_{pq} = \sum_{x,y \in r} x^p y^q I(x,y), \qquad p,q = 0 \text{ or } 1$$
 (1)

where I(x,y) is the intensity of the point (x,y) in the patch and r is the patch radius. With these moments, the intensity centroid of patch is defined as  $C = (m_{10}/m_{00}, m_{01}/m_{00})$ , and the orientation is calculated as  $\theta = \arctan(m_{01}/m_{10})$ .

2) Feature Description: Rotated BRIEF computes descriptors of feature points while maintaining their rotation invariance. The detailed steps are as follows. First, considering the

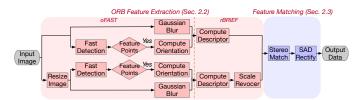


Fig. 2. Visual frontend framework, including feature extraction and matching.

circular patch, p, a pair of points (A,B) is selected, and a binary test,  $\tau$ , is defined as

$$\tau(p; A, B) = \begin{cases} 0 : p(A) \ge p(B) \\ 1 : p(A) < p(B) \end{cases}$$
 (2)

where p(A) is the intensity of patch p at point A.

Second, n pairs of points are selected from the patch p based on Gaussian distribution. Repeated the previous step n times, the descriptor is calculated as a vector of n binary tests as  $f_n(p) = \sum_{1 \le i \le n} 2^{i-1} \tau(p; A_i, B_i)$ .

Third, to ensure rotation invariant, pixels in the patch are rotated by a particular angle around the feature point. In light of the high computation complexity of rotating all points, we choose only to rotate the pairs used for computing descriptors. A  $2 \times n$  matrix consisting of these points is defined as

$$S = \begin{pmatrix} A_1, A_2, \dots, A_{n-1}, A_n \\ B_1, B_2, \dots, B_{n-1}, B_n \end{pmatrix} \tag{3}$$
 Using the patch orientation  $\theta$  and its rotation matrix  $R_\theta$ , the

Using the patch orientation  $\theta$  and its rotation matrix  $R_{\theta}$ , the rotated matrix is derived from  $S_{\theta} = R_{\theta}S$ . Then the feature descriptor is calculated as  $g_n(p,\theta) = f_n(p)|(A_i,B_i) \in S_{\theta}$ .

### C. Feature Matching

- 1) Stereo Matching: This module matches feature points in a stereo image pair. First, for a feature point, F, in left image, the strip-like searching region  $\mathcal R$  in right image is determined. Second, the Hamming distance  $\mathcal H$  of the descriptors between F and each feature point in  $\mathcal R$  is computed. Third, the feature point pair with the smallest  $\mathcal H$  is considered as the best match.
- 2) Rectification: Stereo matching with ORB feature is a local mapping algorithm with fast speed but a high mismatching rate. Thus, SAD (Sum of Absolute Differences) rectification is integrated by correcting the coordinates of feature points.
- Let (F,F') be a matched feature points pair in left and right images. First, patch windows centered at (F,F') are created respectively, as  $(F_w,F'_w)$ . The SAD is computed as  $SAD(F_w,F'_w)=\sum\sum|F_w-F'_w|$ , where smaller SAD value means higher similarity of F and F'. Second, fix  $F_w$  and slide  $F'_w$  within a range, repeat the former steps to compute SAD for each new location, find out the window with the lowest SAD, and F' will be relocated to its center. Third, the disparity and depth information is calculated based on adjusted positions.

#### III. HARDWARE ARCHITECTURE

The overall architecture of the proposed visual frontend accelerator is shown in Fig. 3a. Four cameras and IMU interface with on-board compute. The frontend is implemented in FPGA to accelerate feature extraction and matching, and the CPU is used for backend computations. To improve performance, we propose hardware-based synchronization, direct

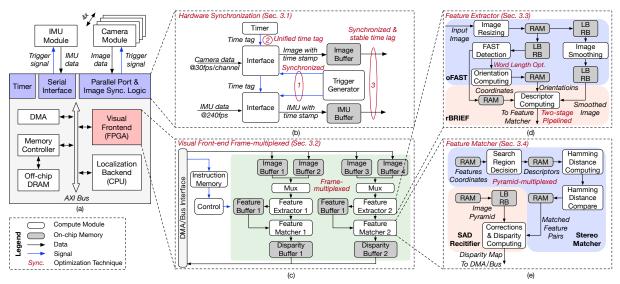


Fig. 3. Overview of proposed FPGA-based hardware architecture design.

I/O architecture (Sec. III-A) and frame-multiplexed schemes (Sec. III-B). The detailed architecture of feature extraction and matching are presented in Sec. III-C and III-D.

#### A. Hardware Synchronization Interface

The synchronized interface between sensors and computing modules is crucial for the autonomous machine to correctly perceive the surroundings and localize itself. However, in the whole system, the software synchronization in CPU leads to variable delay among the four images, making it impossible to achieve reliable localization results.

To solve this unstable synchronization issue, we propose a hardware-based synchronization (Fig. 3b). First, all captured images are directly sent to on-chip RAM through a direct IO architecture. The trigger generator module generates synchronized trigger signals for cameras and IMU. Second, both input images and IMU data are tagged by a unified time tag. Finally, images and IMU are synchronized at the interface with stable time tags and then sent to the computing modules, significantly helping achieve stable feature processing and localization.

## B. Frame-Multiplexed Visual Front-End

Fig. 3c overviews the architecture of vision frontend. We propose a frame-multiplexed scheme where two camera channels share one feature extractor. The rationale behind this is, based on the profiling result, feature extraction (FE) takes 7.28 ms and feature match (FM) takes 14.59 ms when processing 640×480 images, indicating that the latency of FM is twice of FE. Moreover, two identical hardware modules are designed to process two stereo cameras in parallel.

The utilized pipeline is shown in Fig. 4. Two images (left and right) are captured at each frame. During processing, at  $N_{th}$  frame, FE first processes left image and stores the result in buffer and then processes right image. After the extraction is finished, feature descriptors of image pyramid are sent to FM for disparity computation. When FM at  $N_{th}$  frame starts to work, FE is fired up to process images for  $(N+1)_{th}$  frame.

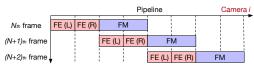


Fig. 4. Pipeline in visual front-end, where FE refers to feature extraction, FM refers to feature matching, L/R refers to left/right image. Two camera channels share one FE (frame-multiplexed).

With this frame-multiplexed scheme, FE and FM could be performed efficiently in pipelining. Visual frontend runs in parallel with optimization backend. This scheme significantly saves hardware resources and improves throughput.

## C. Hardware Architecture of Feature Extractor

The feature extractor block extracts features from images. It reads data from image buffer and calculates the ORB features with on-chip memory. After the task is finished, it sends the features to buffer and descriptors to feature matcher block.

The detailed architecture of feature extraction is shown in Fig. 3d. It consists of image resizing, FAST detection, orientation computing, image smoothing, and descriptor computing modules. RAM, line buffers (LB), and register banks (RB) are used to store intermediate results. The details are as follows.

**Image Resizing.** This module builds a two-layer image pyramid with bilinear interpolation. The size of an input image is  $1280 \times 720$  and a scaled image is  $1067 \times 600$ .

**FAST Detection.** The FAST Detection module takes a  $31\times31$  patch from RB as an input. It detects the feature point and computes the moments of patch (e.g.,  $m_{10}$  in Eq. 1). The coordinates of the feature point (x, y) are stored in RAM.

**Orientation Computing.** This module takes the intensity centroid of a patch as input, and calculates the orientation  $\theta$  of the patch that are stored in RAM.

**Image Smoothing.** The image smoothing module utilizes Gaussian filter to smooth  $7 \times 7$  pixels patch stored in RB. The smoothened images are used to compute feature descriptors.

**Descriptor Computing.** This module takes the smoothened images, coordinates and orientations of feature points as inputs, and determines their descriptors with  $32 \times 8$  bits.

TABLE II FPGA RESOURCE CONSUMPTION OF SYSTEM.

Resource	Modular Used (640×480)			Total Used		
	FE	FM	Ctrl.	640×480	720×1280	
LUT	96850	40034	1759	138643 (51%)	177196 (65%)	
Flip-Flop	54100	12694	479	67273 (12%)	82730 (15%)	
BRAM	271	0	0	271 (30%)	785 (86%)	
DSP	32	0	0	32 (1%)	109 (4%)	

**Design Techniques.** Orientation computing involves division and square root operations that require substantial costs. We adopt a word length optimization method and choose 8-bit to reduce hardware consumption. During descriptor computation, to avoid smoothened images occupying too much memory, we adopt synchronized two-stages shifting line buffers to compute Gaussian filtering and descriptor in a streaming way.

## D. Hardware Architecture of Feature Matcher

The feature matcher block aims to match feature points from stereo images and derive depth information. It contains two parts in our design, the stereo matcher for pre-match and the SAD rectifier for further rectification.

The detailed architecture of feature matcher is demonstrated in Fig. 3e, including region decision, distance computing and compare, correction and disparity computing modules. The design of each module is presented as follows.

**Search Region Decision.** Search Region Decision module takes the coordinates of feature points as inputs and determines whether the feature points locate within the searching field.

**Distance Computing and Compare.** This module obtains the descriptors from RAM and computes the Hamming distance of each pair of feature descriptors. It then finds out the best matching with the smallest value of Hamming distance.

Correction and Disparity Computing. This module is used for SAD rectification. It takes the coordinates of matched feature pairs obtained in stereo matcher and  $11 \times 11$  patch image pyramid from RB, and computes the corrections and disparity. The depth information will be sent for backend use.

**Design Techniques.** We utilize an image pyramid-multiplexed scheme during implementation where two resizing images share the same Feature Matcher block, significantly saving hardware resources costs.

# IV. EVALUATION RESULTS

## A. Experimental Setup

Hardware Platform. The proposed visual front-end accelerator is implemented and evaluated on Xilinx Zynq Ultrascale+ XCZU9EG MPSoC. The FPGA is directly interfaced with the four cameras and IMU sensors. The max operated clock frequency is 203 MHz for feature extractor and 230MHz for feature matcher, respectively. The FPGA device has 274K LUTs, 548K Flip-Flops, 912 BRAMs, and 2520 DSPs in total.

**Resource Consumption.** The resource consumption of the proposed system is shown in Tab. II. We evaluate the design on two different image resolutions. Overall, the hardware architecture utilizes 51% LUT, 12% Flip-Flop, 30% BRAM, and 1% DSP resources when processing 640×480 images.

TABLE III
ACCURACY EVALUATION OF FPGA SYSTEM.

	# Feature Points	# Matched Pairs	# Effective Depth Value
Software	961.2	211.5	107
FPGA	961.1	211.7	107.3
Error	-0.1	+0.2	+0.3

TABLE IV
PERFORMANCE AND POWER COMPARISON.

	Perform. (fps)	Perform. (%)	Power (W)	Power (%)
	Image 1	Resolution: 640x4	80	
Our	69	-	1.63	-
[ <mark>7</mark> ]	56	81.16%	1.94	1.19×
<b>[4</b> ]	67	97.1%	4.56	$2.80 \times$
	Image R	Resolution: 1280x7	20	
Our	50.7	-	2.31	-
Nvidia TX1	9	17.75%	7	$3.03 \times$
Intel i7 Core	15	29.59%	80	$34.63 \times$

Particularly, in 640×480 images, it is observed that FE consumes over two-thirds of the frontend resource; the percentages in 720×1280 images are similar, corroborating our scheme to multiplex FE module between left and right frames.

## B. Accuracy Analysis

The accuracy of the system is evaluated by the results of feature extraction and matching between FPGA and software implementation (MATLAB) with processing 30 frames, shown in Tab. III. For the number of extracted feature points, matched feature points pairs and obtained depth values, the results of two approaches are almost the same (error<0.3%). For detailed coordinates, the accuracy is 99.7%, 98.2% and 96.8%.

## C. Performance and Power Evaluation

**CPU/GPU Comparison.** Tab. IV compares the performance and power of our FPGA design, Nvidia TX1 and Intel i7 CPU. Compared with TX1, the performance is raised by  $5.63 \times$  and power is reduced by 67%. Compared with i7 CPU, the performance is raised by  $3.38 \times$  and power is reduced by 97%.

Existing Accelerator Comparison. Tab. IV compares our proposed hardware with some existing accelerators. Compared to [4] (FPGA), we achieve a slight 1.03× speedup but 64% power reduction. Particularly, we propose extra stereo match modules for depth information, which is vital in 3D environments. Compared to [7] (FPGA), our design achieves 1.23× speedup and saves 16% power. Moreover, we support multichannel camera systems with proposed hardware synchronization scheme. Compared to [6] (ASIC), our design achieves 69 fps on more robust feature-based stereo-flow method, whereas they achieves 171 fps on optical-flow method that may fail in large displacements or inconsistent illumination conditions.

# D. Discussions

Our proposed design can be further improved in two directions. For high-performance scenarios, it can be improved by involving more aggressive pipelining and higher fan-out nets reduction. For embedded scenarios, power can be further reduced by optimizing supply voltage and clock frequency.

#### V. CONCLUSION

In this paper, the unified compute bottleneck of various localization system is identified. An ORB-based visual frontend architecture is presented for real-time and energy-efficient localization and evaluated on FPGA platform. To support multiple cameras and IMU, we propose hardware synchronization for stable localization. To accelerate feature extraction and matching, we utilize frame-multiplexing, parallelism and word length optimization. Compared with Nvidia TX1 and Intel i7, our design achieves  $5.6\times$  and  $3.4\times$  speedup in frame rate, and  $3\times$  and  $34.6\times$  improvement in energy efficiency, respectively.

#### ACKNOWLEDGEMENTS

This work was supported in part by C-BRIC, one of six centers in JUMP, a Semiconductor Research Corporation (SRC) program sponsored by DARPA.

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