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A 25-GHz Differential LC-VCO in 90-nm CMOS

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Abstract—A 25 GHz 90-nm CMOS differential voltage controlled oscillator is presented. Filtering is used at the common source node of the cross-coupled transistors to lower the phase noise. The frequency tuning is accomplished by a continuously tuned accumulation-mode MOS varactor. The oscillator measures a frequency tuning range of 8.7%, and a worst case phase noise over the tuning range of -106 dBc/Hz at 1 MHz offset, with a 1.1 V supply and a power consumption of 6.6 mW. The phase noise figure of merit, FOM, is between 185 dB and 187 dB over the tuning range.

I. INTRODUCTION

Local oscillator signals with low phase noise are needed in radio frequency (RF) transceivers, and the development of the complementary metal oxide semiconductor (CMOS) technology in the past decade has made it a viable technology for high frequency applications. The differential cross-coupled LC oscillator is well known for its good phase noise performance and ease of implementation [1]. This work presents measurement results of such an oscillator operating at 25 GHz, implemented in 90-nm CMOS, featuring a continuously tuned accumulation-mode varactor [2]. According to the measurements, the circuit is capable of generating low phase noise signals that could be used in e.g. a fully integrated 25 GHz CMOS wireless transceiver.

II. CIRCUIT DESIGN

The schematic of the voltage controlled oscillator (VCO) is shown in Fig. 1. It consists of two cross-coupled transistors that realize a negative resistance to compensate for the resonator losses, a source inductor, a FET current source, and a capacitor in parallel with the current source. The three latter components form a filtered current source [3], which improves the phase noise performance of the oscillator. The FET current source is used because the best phase noise performance is achieved when the amplitude in the resonance tank is on the limit of being current limited. The current source should ideally be noiseless, and have a high impedance at $2f_0$ to prevent the cross-coupled pairs triode resistance from loading the resonator in the switched state, i.e. when one transistor is off and the other one is in the triode region. A source inductor is therefore used to resonate the parasitics of the source node at $2f_0$. Also, a capacitor

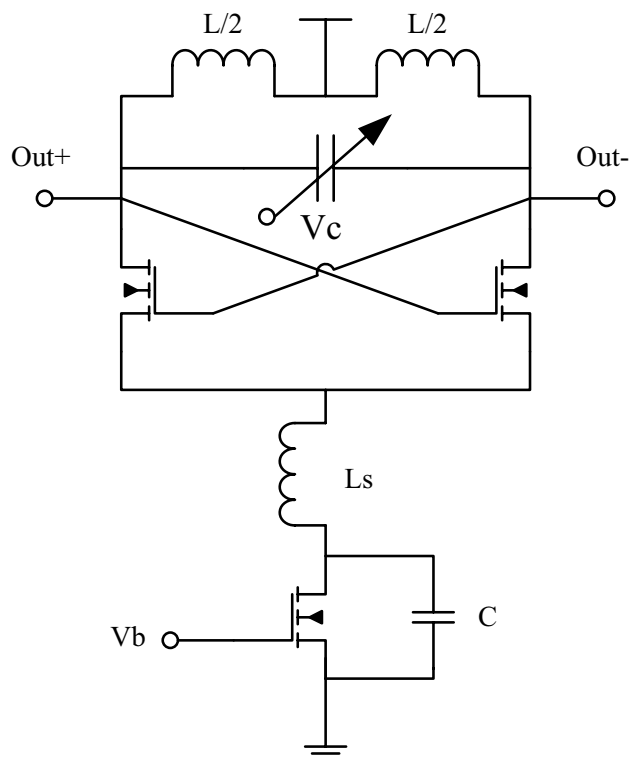


Fig. 1. VCO Schematic

itor in parallel with the current source shunts the high frequency noise from the current source to ground. The filtering technique thereby prevents tail current noise at $2f_0$ from creating phase noise, but low frequency tail current noise will still cause amplitude noise, which can be converted to phase noise by the nonlinearities of the varactor [4].

A major challenge in oscillator design is to simultaneously achieve a low phase noise and a wide frequency tuning range. In oscillators using continuous frequency tuning, a wide tuning range is obtained using a large varactor with a high C_{max}/C_{min} ratio. Unfortunately the losses of such a varactor will degrade the quality factor of the resonator, resulting in increased phase noise.

TABLE I
SIMULATED INDUCTOR DATA

Inductor	Turns	Inductance (pH)	Q	fs (GHz)
L @ f_0	2	315	26	82
Ls @ $2f_0$	1	90	18	157

An accumulation-mode varactor [2], [5] was used in this work since it offers low losses. It operates in the accumulation and depletion regions, and has a non-minimum channel length, L , of 110 nm. A compromise was made not to use minimum channel length (90 nm), since although it would have given the varactor a slightly larger quality factor, Q , it would also have resulted in a smaller tuning range. It can be shown that the Q of the varactor is proportional to L^{-2} in the accumulation region [6], and to L^{-1} in the depletion region [7]. Since the losses of the varactor are dominated by series resistance, Q is inversely proportional to frequency, and the varactor will limit the total Q of the resonator at high frequencies and tuning ranges. There are no extra process steps used in the fabrication of the accumulation-mode varactor, but its generally not supported by the foundries. An inversion-mode varactor was used during the simulation phase, since no model of a high frequency accumulation-mode varactor with short channel length was available.

The inductor geometries were found by using FastHenry in combination with the in-house inductor optimization tool, Indentro [8]. The tank inductor was realized as a two turn differential inductor, and the source node inductor as a single turn spiral. The simulated inductor data is shown in Table I. The capacitively coupled substrate losses are blocked by patterned ground shields in metal 1 used beneath the inductors.

To enable measurements the oscillator was connected to open drain buffers designed to drive 50 Ω loads, Fig. 2, which were implemented on the same chip.

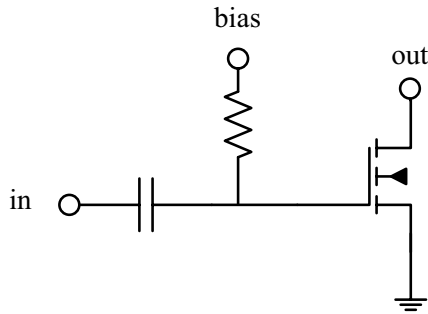


Fig. 2. Open drain buffer

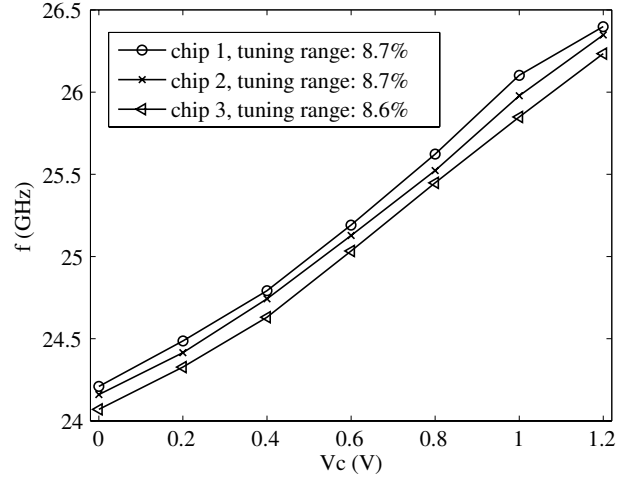


Fig. 3. Frequency vs. control voltage

III. LAYOUT

The die photo of the oscillator is shown in Fig. 8, where the padframe area measures 600 μm x 600 μm . The core area of the VCO measures just 120 μm x 310 μm , and is dominated by the two inductors. The entire layout was designed as symmetric as possible to minimize amplitude and phase errors. The pads on the top side are the RF-output signals (G-S-G-S-G) from the open-drain buffers. The pads on the bottom side are used for supply and bias voltages. The parasitic inductances of the wires to the inductors have been taken into account by adjusting the value of the tank inductor, L , and the source inductor, L_s , respectively. Also, all pads, except for the two RF outputs, are ESD protected. The ESD protection is realized using pn diodes for the pads, and multiple distributed clamps between the supply voltage and ground.

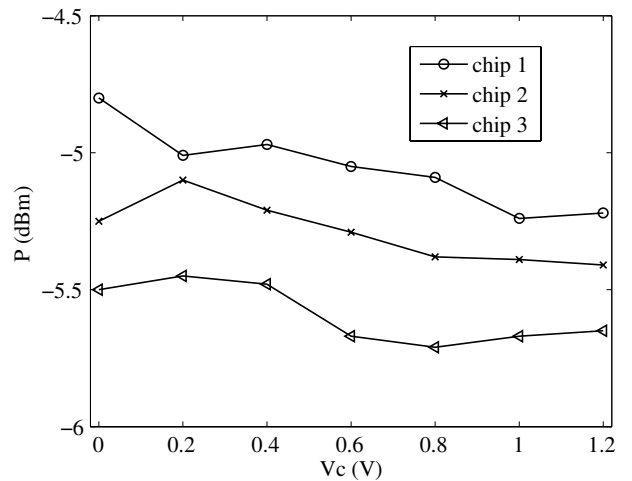


Fig. 4. Output power vs. control voltage

TABLE II
PERFORMANCE OF SOME PREVIOUSLY REPORTED CMOS VCOs AND THIS WORK

Ref.	Process	f_0 (GHz)	Tuning (%)	P_{DC} (mW)	PN @ 1 MHz (dBc/Hz)	FOM (dB)	FOM _T (dB)
This work	90nm CMOS	25.3	8.7	6.6	-105.8*	185	184
[9]	90nm CMOS	18	8.3	4.2	-116*	195	194
[10]	0.13 μ m CMOS	18	5.6	17.3	-117	190	185
[11]	0.13 μ m CMOS	11.55	5.5	8.1	-110.8	183	178
[12]	0.18 μ m CMOS	16	5.6	8.1	-111	186	181

*worst case phase noise over the tuning range

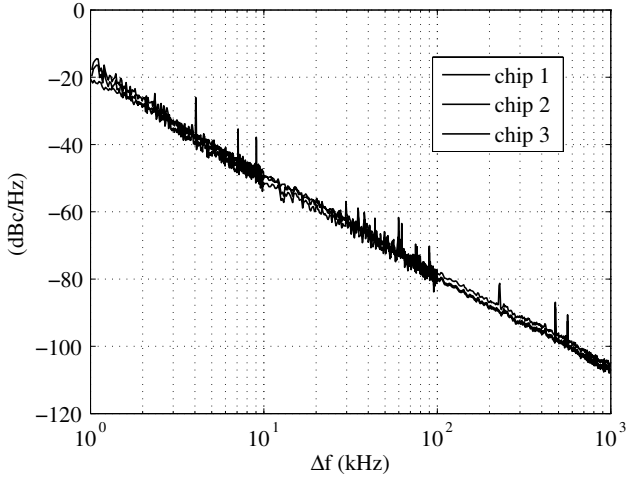


Fig. 5. Phase Noise vs. offset frequency, V_c=0.6 V

IV. EXPERIMENTAL RESULTS

Three different samples of the oscillator have been measured. The measurements were performed with a probe station using on-wafer probing with Infinity RF and Quadrant DC probes from Cascade Microtech. The best performance of the oscillator was found at 1.1 V supply and 6 mA current. This gives a power consumption of 6.6 mW for the oscillator core. The open-drain buffers were biased to a drain voltage of 1 V and a drain current of 6.5 mA per buffer. The following results were measured at this bias point.

A spectrum analyzer, Rhode & Schwarz FSU50, was used to measure the frequency tuning characteristic and the buffer output power. The results for the three different samples are shown in Fig. 3 and Fig. 4. As can be seen the tuning range measures 8.7%.

The phase noise of the three chips was measured using a Eurotest PN9000 phase noise measurement system together with an external downconversion mixer, Marki M90765. A signal generator, Agilent E8257D, was used to generate the LO signal for the mixer.

The phase noise was measured versus offset frequency (Δf) for a varactor control voltage (V_c) of 0.6 V, see Fig. 5. The phase noise was also measured versus the var-

actor control voltage, Fig. 6. As can be seen in the figure, there is a phase noise variation of about 3 dB over the tuning range. Also shown in the legend of Fig. 6 is the phase noise figure of merit, FOM, which is between 185 dB and 188 dB for the measured samples, calculated at 1 MHz offset frequency using

$$FOM = 10 \log_{10} \left(\left(\frac{f_0}{\Delta f} \right)^2 \cdot \frac{1}{10^{\frac{L(\Delta f)}{10}} P} \right) \quad (1)$$

,where P is the power consumption of the oscillator in mW, f_0 the oscillation frequency, Δf the offset frequency, and $L(\Delta f)$ the phase noise at Δf . To take also the tuning range into account, the expression (1) can be modified [13] to

$$FOM_T = 10 \log_{10} \left(\left(\frac{f_0 \cdot \text{tuning}(\%)}{10 \cdot \Delta f} \right)^2 \cdot \frac{1}{10^{\frac{L(\Delta f)}{10}} P} \right) \quad (2)$$

,which is between 184 dB and 187 dB for the measured samples at 1 MHz offset.

A performance comparison of some published state-of-the-art CMOS VCOs above 11 GHz and this work is shown in Table II. Some of the references in the table report only the best case value for the phase noise figure of merit, but to avoid sweet spots it is the worst case value over the tuning range that should be used for comparison. As can be seen in Table II the oscillator presented in this work compares well both in FOM and FOM_T. However, excellent performance is reported by Jacobsson et. al. [9], using post-processed high-Q inductors. This work instead uses standard CMOS without post processing or extra thick top metal options.

The oscillator pushing has also been measured and is shown in Fig. 7. As can be seen in the figure, there is approximately a 270 MHz frequency increase for a supply voltage change from 1.2 V to 0.9 V.

V. CONCLUSION

A differential 25 GHz LC VCO using an accumulation-mode varactor has been implemented in a 90-nm CMOS process. The oscillator measures a frequency tuning range of 8.7%. A good phase noise performance is measured over the entire tuning range, at worst -106 dBc/Hz at 1 MHz offset, with a power consumption of 6.6 mW for the oscillator core. This gives a phase noise figure of merit, FOM, of

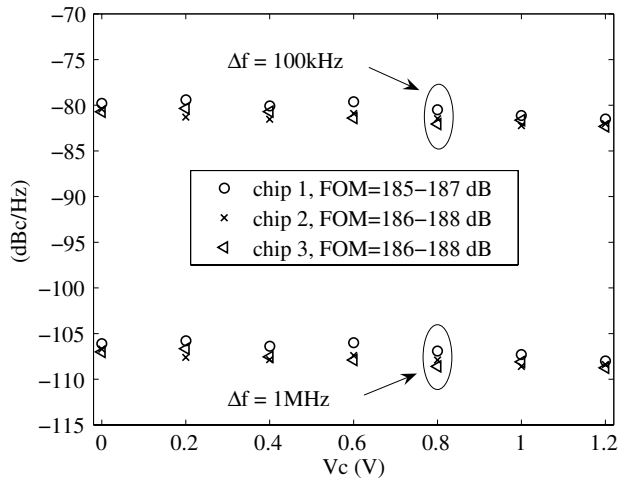


Fig. 6. Phase noise vs. control voltage

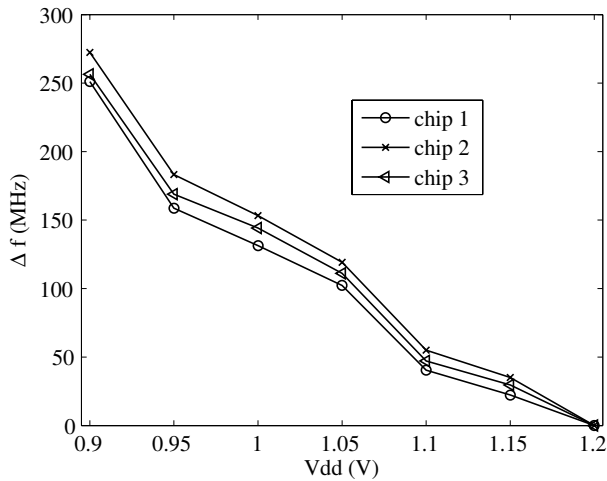


Fig. 7. Oscillator frequency pushing, $V_c=0.6$ V

185 dB. Taking also the tuning range into account gives a figure of merit, FOM_T , of 184 dB.

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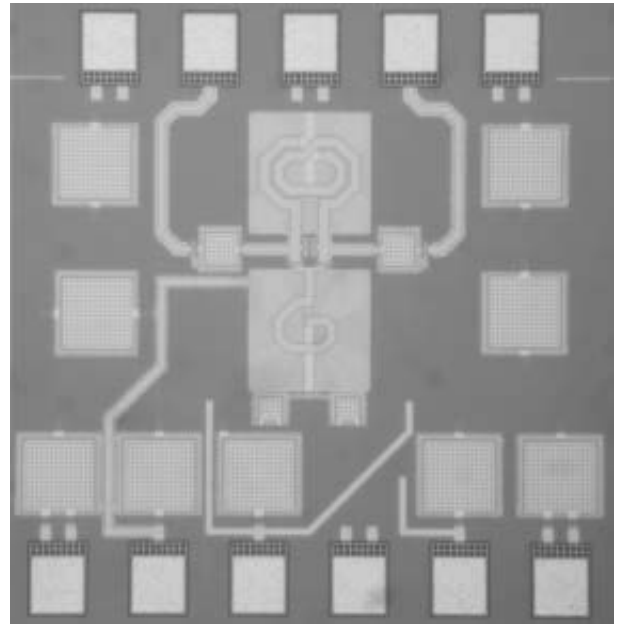


Fig. 8. Die photograph of the VCO ($600 \mu\text{m} \times 600 \mu\text{m}$).

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