Cooperative virtual channel router for adaptive hardwired FPGA network-on-chip

ABSTRACT

In this paper, the FPGA architecture having a hardwired network-on-chip (NoC) as system-level interconnect resource with adaptive router to support ranges of traffic condition. The proposed adaptive routers cooperatively allocate the virtual channel to minimizes the cost of supporting a wide range of traffic requirements from various FPGA application design instances. Simulation results show performance augmentation of 25% on average over an equal-size standard router, or achieve iso-performance using 50% less virtual channel buffer size.

Keyword: Adaptive; FPGA; Hardwired; NoC