Model Checker Execution Reports

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Abstract—Software model checking constitutes an undecidable problem and, as such, even an ideal tool will in some cases fail to give a conclusive answer. In practice, software model checkers fail often and usually do not provide any information on what was effectively checked. The purpose of this work is to provide a conceptual framing to extend software model checkers in a way that allows users to access information about incomplete checks. We characterize the information that model checkers themselves can provide, in terms of analyzed traces, i.e. sequences of statements, and safe cones, and present the notion of execution reports, which we also formalize. We instantiate these concepts for a family of techniques based on Abstract Reachability Trees and implement the approach using the software model checker CPAchecker. We evaluate our approach empirically and provide examples to illustrate the execution reports produced and the information that can be extracted.

I. Introduction

Software model checking [23] constitutes an undecidable problem and, as such, even an ideal tool will in some cases fail to give a conclusive answer. In practice, undecidability is not the only issue. The vast state spaces can lead to the complete exhaustion of system resources or impractically long execution times.

Software model checking has been making steady progress during the past decade and today's state-of-the-art software model checkers can handle specific industrial problems particularly well. For instance SDV [1] is highly successful in finding bugs in Windows device drivers.

Unfortunately, some instances take hours of computation, only to inform the user that no counterexample was found within the allotted time or memory limit. A user facing this situation is confronted with several high-level questions about what the verification attempt actually achieved. Should she retry with a longer time limit? How much longer? Is the tool making any progress on the instance? Maybe she should try another technique?

Our goal is to extend and complement existing work on partial verification by providing a different way for users to observe the work performed by the software model checker. An important step towards our goal is to be able to answer much simpler inquiries about incomplete verification attempts.

We believe answering the following informal questions would be valuable for a user after an inconclusive verification attempt:

Can partial safety assurances about the system be extracted from an incomplete verification attempt? For

- instance, a user that receives a report showing that a whole class of relevant behaviors has been exhaustively checked may use this as part of a dependability case.
- Can behavior that was not analyzed be explored by a user? For instance, a user that can observe that relevant classes of behavior have not even been looked at by the checker, let alone verified, may decide that what seemed like a sufficiently thorough analysis is not such (e.g., an inexperienced user would benefit from knowing that a tool based on BMC with a fixed bound can sometimes give up without ever exploring anything beyond an initialization loop[24]). Moreover, a more experienced user attempting full verification may decide that a drastic change in the verification strategy is needed (e.g., another tool, abstracting the system-under-verification, etc.).

By incomplete verification attempt we refer to a situation when a software model checker fails to confirm any counterexample as feasible and also fails to prove the instance safe.

In this paper we explore answering the first question using the notion of *safe cone*. A *safe cone* is a finite trace for which any extension has been analyzed in the incomplete verification attempt. A *minimal feasible safe cone* represents compactly a set of traces that have been successfully verified by the checker. For the second question we build on the notion of a *frontier*. A *frontier trace* is a feasible finite trace that was analyzed by the checker but none of its feasible extensions were. Frontier traces represent compactly classes of traces that were not explored by the checker.

Our hypothesis is that execution reports that under-approximate the set of minimal feasible *safe cones* and the set of maximal feasible *frontier traces* can be computed in reasonable time (with respect to the cost of verification) and can provide non-trivial feedback on incomplete verification attempts.

We will start by illustrating with examples the information we wish to extract and defining a possible formalization of the idealized properties it should have. Subsequently, we define and discuss Execution Reports, an under-approximation of the ideal output. Afterwards, we instantiate these concepts for the family of techniques based on Abstract Reachability Trees (ART) [21], and discuss a proof-of-concept implementation built as an extension of CPAchecker [7]. We also include an empirical evaluation of our implementation.

We conclude this paper with a discussion of related work and how our approach compares to existing techniques fol-

```
int nondet();
   int min(int a[], int n) {
      int res = a[0];
3
       for (int i=0;i<n;++i)</pre>
4
        if (a[i] < res) res = a[i];</pre>
5
       return res;
   }
7
   void init_vector(int a[], int n) {
      int i = 0;
9
       for (i=0;i<n;++i) {</pre>
10
11
        a[i] = nondet();
12
   }
14
   void test_min(int large) {
       int n;
15
       if (large) {
16
          n = 20;
        else {
18
19
          n = 1;
20
      int a[20];
       init_vector(a, n);
       int min_elem = min(a, n);
      assert(min_elem <= a[0]);
24
   }
25
```

Figure 1: Harness for method min

lowed by a few concluding remarks.

II. MOTIVATION: WHAT HAS AND HAS NOT BEEN ANALYZED?

We frame our work in the context of a verification attempt being interrupted before its completion.

Many verification techniques work by incrementally exploring the state space. This is the case for software model checking techniques and implementations like BMC [11], lazy predicate abstraction [21], inlining and unrolling based-techniques like Corral [25], DSE [12] and, in general, ART-based implementations of various techniques, including explicit value analysis [8] and CEGAR variants of some of the previous among other.

In these techniques and implementations one can understand that incremental exploration leads to an incremental but silent increase of *analyzed* traces, i.e. sequences of statements, as depicted in the examples that follow. Moreover, certain statement traces will reach a portion of the behavior space that has been fully verified, implicitly defining a *safe cone* containing all possible ways of extending such traces.

Understanding that partial explorations provide safety assurances, we are particularly interested in the *frontiers* defined by minimal *safe cone* traces and maximal *analyzed* statement traces.

We illustrate these concepts with a verification attempt of the instance in Figure 1 with bounded model checking.

Example 1 (Analyzed behaviors in BMC). The code snippet in Figure 1 corresponds to a parametric test harness exercising the method min. The harness input as well as the result of

method nondet are interpreted by the verification technique as non-deterministic. Our verification attempt, in this example, is not interrupted due to reaching a resource limit but instead due to using a bounded model checker [11] with a bound on the number of loop iterations set to 3.

Using this configuration, the tool would perform an exhaustive exploration but would disregard any executions involving the fourth loop iteration of the for-loop in init_vector.

Any sequence of statements reaching line $19 \, (n=1;)$ will necessarily satisfy the safety property, since the incomplete verification attempt would not find any assertion failures and the loop within init_vector can be exhaustively analyzed. That means the sequence of statements consisting of lines 15 (int n;), $16 \, (if \, (large))$ and $19 \, (n=1;)$ defines a safe cone, because every continuation of the statement trace is also safe. The former trace is also minimal in the sense that the trace resulting from removing the last statement, line 19, is not a safe cone.

Moreover, any execution that carries out line 10 (for (i=0; i < n; ++i)) at most 4 times (3 full iterations and 1 bound check) is also analyzed by the incomplete verification attempt. In contrast, any sequence containing line 10 at least 5 times is ignored by BMC and therefore will not be examined. Therefore, analyzed does not contain traces exercising line 10 5 times or more. That is, the trace composed of lines 15, 16, 17, 21, 22, 9 and then 4 repetitions of lines 10 (for (i=0;i < n;++i)) and 11 (a[i]=nondet();) is a maximal analyzed trace.

We will now revisit these concepts from an entirely different technique: lazy predicate abstraction [21].

Lazy predicate abstraction, the algorithm used by BLAST [21], consists of two alternated phases. The first phase generates, on-the-fly, a reachability tree whose nodes correspond to vertices of the Control Flow Automaton¹ (CFA) of the program. This process goes on until exhaustively exploring the tree or until reaching a node that corresponds to an assertion failure. Each node is associated with a predicate, initially true, that must hold for any path reaching that node and helps prune the successors that are not reachable. If, and when, a node that represents an error is reached, the second phase deals with analyzing the potential counterexample to determine whether the path reaching the error node is feasible. If the latter phase determines the potential counterexample is infeasible, the reachability tree is refined by strengthening the predicates associated to the appropriate nodes so that the path reaching the error node is pruned. Lastly, when a counterexample is produced, it can be checked with a more precise analysis to ensure its feasibility. However, if this additional check fails, the search is abandoned.

Example 2 (Analyzed behaviors in lazy predicate abstraction). *The code presented in Figure 2, reproduced from the paper*

¹A Control Flow Automaton, similar to a Control Flow Graph, captures the control flow of the program, where nodes correspond to locations and edges are labeled with statements.

```
int nondet();
   int main() {
    int p = nondet();
    if (p) {
4
        int i;
        for (i = 0; i < 1000000; i++);
       assert(i >= 1000000);
    } else {
        int x = 5;
        int y = 6;
11
        int r = x * y;
       assert(r >= x);
    }
14
    return 0;
15
```

Figure 2: Non-linear arithmetic. Reproduced from CMC papers [5], [6].

presenting Conditional Model Checking [5], [6], contains a non-linear safety property. As explained, the construction of the reachability tree will reach the error node and the second phase would attempt to verify the feasibility of the path leading to it. The feasibility check is usually implemented by creating a verification condition to be checked by an underlying SMT solver and, therefore, inherits the latter's limitations. In particular, SMT solvers usually cannot handle non-linear arithmetic and, instead, model multiplication as uninterpreted functions. Concretely, the SMT solver would not be able to prove the path infeasible. However, the subsequent counterexample feasibility check would prove the path is actually infeasible, causing the exploration to stop.

Given the failure to analyze the assertion, the following is a maximal analyzed trace: lines 3 (int p = nondet();), 4 (if (p)), 9 (int x = 5;), 10 (int y = 6;) and 11 (int r = x * y;).

On the other hand, the then branch of the if-statement can be successfully verified with this technique, since tracking the predicate i < 1000000 suffices to prove the assertion always holds when execution leaves the for-loop.

The successful verification of the then branch would make the trace composed of lines 3 (int p = nondet();), 4 (if (p)) and 5 (int i;) a safe cone.

A. Execution Reports (ERs)

We now formally define execution reports as an underapproximation of the set of *safe cones* and *frontier* traces. These definitions rely on two predicates (*analyzed*? and isSafeCone?) whose definition depends greatly on the underlying verification technique used in the incomplete verification attempt. Consequently, in this section we simply provide properties that predicates analyzed? and isSafeCone? ought to satisfy. In the next section we ground the definition of these predicates for Abstract Reachability Tree based verification techniques [21].

Examples 1 and 2 illustrate how the notions of analyzed

and *safe cone* apply to diverse techniques. We will capture these notions as predicates over traces in the following definitions.

Let the alphabet Σ contain all statements in a program, making $\pi \in \Sigma^*$ a sequence of statements.

Property 1. The predicate analyzed? : $\Sigma^* \to Bool$ satisfies the following property, where \cdot stands for concatenation: $\forall \pi, \pi' \in \Sigma^*$. $\neg analyzed?(\pi) \to \neg analyzed?(\pi \cdot \pi')$

Property 1 aims to formalize the notion of incrementality that we implicitly used throughout the examples. Note that this property is logically equivalent to its contrapositive, that is, $analyzed?(\pi \cdot \pi') \rightarrow analyzed?(\pi)$, as expected of an incremental exploration.

Property 2. The predicate $isSafeCone?: \Sigma^* \to Bool$ satisfies the following property, where \cdot stands for concatenation: $\forall \pi, \pi' \in \Sigma^*$. $isSafeCone?(\pi) \to isSafeCone?(\pi \cdot \pi')$

Property 2 reflects our notion of *safe cone* as a trace reaching a fully analyzed portion of the behavior space. Any trace extension will necessarily also be a *safe cone*.

Property 3. The predicate is SafeCone? : $\Sigma^* \to Bool$ satisfies the following property:

```
\forall \pi \in \Sigma^*. \ is SafeCone?(\pi) \rightarrow analyzed?(\pi)
```

Property 3 formalizes the connection between the two predicates, in particular how $isSafeCone?(\pi)$ subsumes $analyzed?(\pi)$.

Definition 1. Given a trace $\pi \in \Sigma^*$ and a program \mathcal{P} , we introduce the following predicate:

 $feasible_{\mathcal{P}}(\pi)$ holds iff there exists a concrete execution of the program \mathcal{P} that executes π .

Given that we will always refer to a single program at a time, the system-under-analysis, we will omit the subscript.

Property 4. Given $\varphi: \Sigma^* \to Bool$, a boolean predicate that captures the safety property of interest, the predicate analyzed? : $\Sigma^* \to Bool$ satisfies the following property:

$$\forall \pi \in \Sigma^*. \ analyzed?(\pi) \land \ feasible(\pi) \rightarrow \varphi(\pi)$$

Property 4 is at the core of interpreting analyzed traces as providing safety assurances. This property also holds for isSafeCone? due to Property 3. The predicate $feasible(\pi)$ in the antecedent places the focus of safety assurances on feasible traces, that is, traces that correspond to actual behaviors of the system-under-analysis.

Recall that we provide properties that constrain the predicates analyzed? and isSafeCone? but not concrete definitions of these predicates as specific definitions depend on the underlying verification technique. We now define the set of $safe\ cones$ and $frontier\ traces$ of an incomplete verification attempt.

Definition 2. The set SafeCone is defined as follows: $SafeCone = \{\pi \cdot s | \pi \in \Sigma^*, s \in \Sigma, \neg isSafeCone?(\pi) \land feasible(\pi \cdot s) \land isSafeCone?(\pi \cdot s)\}$

Definition 3. The set Frontier is defined as follows:

Frontier = $\{\pi \cdot s | \pi \in \Sigma^*, s \in \Sigma, analyzed?(\pi) \land feasible(\pi \cdot s) \land \neg analyzed?(\pi \cdot s)\}$

Definitions 2 and 3 are related to Properties 2 and 1 respectively, since the incrementality of the analysis is key to the search for maximal analyzed traces, as in the set Frontier, and minimal safe cone traces, as in SafeCone.

The set SafeCone can provide safety assurances about the system, as in Example 2, where the *then* branch of the if-statement has been fully verified.

Conversely, Frontier can suggest shortcomings in the incomplete verification attempt. For instance, in Example 1, the existence of a trace $\pi \in Frontier$ that did not even go past the initialization loop suggests an important part of the test harness was not sufficiently analyzed.

The conclusions obtained from inspecting both sets can be useful to assess the progress achieved throughout the incomplete verification attempt.

We anticipated the intuitive notion captured by these definitions in Examples 1 and 2, but there is one important consideration that we omitted so far and now included in the definitions: feasibility.

Feasibility is relevant because, by definition, infeasible traces do not correspond to system behaviors. Without feasibility guarantees, interpreting each trace would require careful analysis, because it could mislead a user into either increasing or decreasing her confidence in the system-under-analysis.

Definition 4. An execution report is a tuple (S, F) where $S \subseteq SafeCone$ and $F \subseteq Frontier$.

Definition 4 defines *execution reports* as under-approximations of the sets SafeCone and Frontier, allowing empty sets as valid *execution reports*.

The sets SafeCone and Frontier can grow quickly, making it extremely inefficient to compute the full sets. Furthermore, some of the traces can be redundant, in a sense, if they only differ in a few statements, making it sensible to under-approximate.

Ideally, it would be desirable to characterize these underapproximation. However, we opted in this work for a notion of *completeness* with respect to statements in the code that does not fully characterize the sets S and F but does not allow, in the general case, empty sets as valid *execution reports*: For both sets, SafeCone and Frontier, we require that if a trace $\pi \in SafeCone$ (resp. Frontier) ending in a specific location l exists, then there exists $\pi' \in S$ (resp. F) and π' also ends in l. This completeness guarantee does not force extremely large sets of paths to be reported and loosely resembles a notion of coverage. Our algorithm to generate *execution reports* guarantees this completeness criterion.

III. REPORTS FOR ART-BASED IMPLEMENTATIONS

Throughout this section we will explain how we generate Execution Reports for Abstract Reachability Tree (ART)-based [21] techniques.

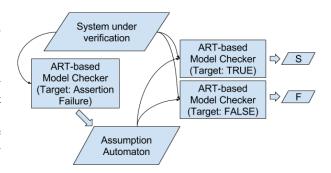


Figure 3: Architecture of ER generation.

ARTs constitute a relevant intermediate data structure used in verification. The variety of techniques implemented using ARTs makes them ideal for our proof-of-concept implementation. ART-based implementations comprise a wide range of dissimilar techniques, encompassing lazy abstraction [21], BMC [11], explicit value analysis [8] and CEGAR variants of some of the previous [8], among other.

In order to explain how we generate Execution Reports for ART-based techniques, we first define analyzed? and isSafeCone? for these techniques in subsection III-A.

We will use Assumption Automata, an existing machine-readable abstract representation of ARTs, for our implementation. In subsection III-B we briefly explain Assumption Automata and their two states most relevant to us, TRUE and FALSE, which we will use to obtain *safe cones* and *frontier* traces, respectively.

Finally, in subsection III-C we will explain how we compute Execution Reports using an Assumption Automaton, produced by an earlier incomplete verification attempt, and the system-under-verification as input, as depicted in Figure 3.

A. ARTs as intermediate data structures

We have discussed how the concepts of analyzed and safe cone, captured by predicates analyzed? and isSafeCone? respectively, apply to example techniques. In this sub-section we will instantiate these concepts to Abstract Reachability Trees (ARTs) [21].

An ART is a tree whose nodes correspond to vertices of the CFA of a program and each node is associated to an element of an abstract domain. In the case of BLAST, that abstract domain is a lattice of predicates.

ART-based algorithms consist of two phases, the first one comprises an incremental generation of the ART and the second phase involves a more thorough counterexample check.

For the purpose of stating which traces can be considered analyzed we can ignore the abstract domain elements associated to each node. We can then think of an ART as a tuple $(G,W,q_0,covered)$ where $G=(S,\Sigma,\delta)$ is a graph, $W\subseteq S$ represents a wait list, $q_0\in S$ is the initial state, $covered:S\to S$ captures subsumption between nodes, and $\delta:S\times\Sigma\to S$ is a transition function. The graph G captures the structure of the partially built ART. W is the wait list

that contains elements to be analyzed in order to continue the construction of the ART. The function covered is necessary to represent subsumption between nodes but is not total. We say that a node e is covered by e' iff covered(e) = e'. Analogously, we consider that a node e is not covered iff covered(e) is undefined. Successors of a subsumed node e are not explored because the state space captured by e is also represented by covered(e). Hence, subsumption is relevant to defining which parts of the state space can be considered explored.

To make the definitions easier to read, we will assume the following invariant holds for ARTs relative to *covered*:

Property 5. $\forall e \in S$. such that covered(e) is defined, then covered(covered(e)) is not defined.

Informally, this means that no node is covered by another covered node.

In ART-based algorithms, a node e covered by e' need not be further analyzed because any error state found from e will also be found from e'. However, a sequence of statements that reaches e might not be a safe trace if it is possible to reach an assertion failure from e'. In other words, the sub-tree rooted in e cannot be considered exhaustively built unless that is also the case for the sub-tree rooted in e'. This observation is crucial to define what can be regarded as analyzed or $safe\ cone$.

We will extend δ as $\delta': (S \cup \{None\}) \times \Sigma \to S \cup \{None\}$, with $None \notin S$ to make it total and resolve the *covered* function transparently as follows:

$$\delta'(q,s) = \begin{cases} \delta(q,s) & \text{if } \delta(q,s) \text{ is defined and} \\ & covered(\delta(q,s)) \text{ is not} \\ covered(\delta(q,s)) & \text{if both } \delta(q,s) \text{ and} \\ & covered(\delta(q,s)) \text{ are defined} \\ None & \text{otherwise} \end{cases}$$

Due to Property 5, $\delta'(q,\pi)$ is never a covered node. Moreover, we will adapt δ' to traces with $\hat{\delta'}: S \cup \{None\} \times \Sigma^* \to S \cup \{None\}$ as follows:

Given $q \in S \cup \{None\}$, $s \in \Sigma$ and $\pi \in \Sigma^*$:

$$\hat{\delta'}(q,s) = \delta'(q,s)$$

$$\hat{\delta'}(q,s \cdot \pi) = \hat{\delta'}(\delta'(q,s),\pi)$$

We will consider that $analyzed?(\pi)$ holds for a trace π iff no prefix of π reaches a node in W from the initial node. That is:

analyzed?(
$$\pi$$
) iff $\neg \exists \pi' \in \Sigma^*.isPrefix(\pi', \pi) \land \hat{\delta'}(q_0, \pi') \in W$

Informally, we consider π analyzed when no prefix of π reaches one of the states pending exploration, i.e. those in W. The predicate analyzed? is clearly monotonic, satisfying Property 1: $\neg analyzed$?(π) means there exists a prefix that reaches W, therefore any extension $\pi \cdot \pi'$ will also share that prefix.

Similarly, we will consider that $isSafeCone?(\pi)$ holds for a trace π iff any prefix of π leads, from the initial node, to a sub-tree already exhaustively built. Intuitively, a sub-tree is exhaustively built when none of its nodes are in W, the set containing states pending exploration. More precisely:

$$isSafeCone?(\pi) \ \textit{iff}$$

$$\exists \pi' \in \Sigma^*.isPrefix(\pi',\pi) \land \forall \pi'' \in \Sigma^*.\hat{\delta'}(q_0,\pi' \cdot \pi'') \notin W$$

Analogously, the predicate isSafeCone? is monotonic, satisfying Property 2: isSafeCone? (π) means there exists a prefix from which W is unreachable and consequently any extension $\pi \cdot \pi'$ will also share that prefix.

B. Assumption Automata

We now briefly explain Assumption Automata [5] because our implementation takes an Assumption Automaton as part of its input instead of ARTs.

An Assumption Automaton is essentially an abstraction of an ART where the elements of the abstract domain associated to each node are removed. Additionally, the structure is compressed by collapsing sub-trees which have been entirely verified into a single node TRUE and every node covered by another node is merged with the latter. Finally, nodes in the wait list are only connected to a single node FALSE. An Assumption Automaton encodes the progress achieved throughout an earlier incomplete verification attempt in a machine-readable format [4], which is the fundamental reason why we use it.

The definition of predicate $analyzed?(\pi)$ can also be stated in terms of Assumption Automata. The predicate holds *iff* no prefix of π reaches FALSE. Once again, understanding an Assumption Automaton as a graph, the predicate is defined as follows:

$$analyzed?(\pi) iff$$

$$\neg \exists \pi' \in \Sigma^* \text{ such that } isPrefix(\pi',\pi) \land \hat{\delta'}(q_0,\pi') = \mathtt{FALSE}$$

Similarly, $isSafeCone?(\pi)$ holds iff a prefix of π reaches the node TRUE. That is:

$$isSafeCone?(\pi)\ i\!f\!f$$

$$\exists \pi' \in \Sigma^* \ \text{such that}\ isPrefix(\pi',\pi) \wedge \hat{\delta'}(q_0,\pi') = \texttt{TRUE}$$

It is worth noting that, even though one Assumption Automaton can correspond to several ARTs, applying the predicates isSafeCone? and analyzed? to the former or to any of the latter will yield the same result.

C. Generating reports for CPAchecker

We built a proof-of-concept implementation, consisting of two verification tasks, capable of generating execution reports for ART-based techniques on top of CPAchecker.

The input for our implementation is an Assumption Automaton and the original system-under-analysis. Our output are the sets S and F, composed of the counterexamples, i.e. traces, generated by two independent verification tasks, as shown in Figure 3.

We resort to the conceptual framework of Configurable Software Verification [7] to formalize how our algorithm is parametric, allowing different reachability analyses to be used. It is worth mentioning that the algorithm used to generate an Execution Report is in no way related to or restricted by the technique used for the original verification attempt, as long as the latter generates an Assumption Automaton.

Informally, we augment an existing ART-based algorithm by adding an Assumption Automaton state to the abstract domain element associated with each node. That is, in Figure 3, the process that produces F will attempt to find feasible traces that reach the state FALSE in the Assumption Automaton, whereas TRUE will be the target state in the case of the process generating S.

We already explained the basics of ART-based algorithms, but some more detail is necessary to define our extension. The framework of Configurable Software Verification allows us to define a Configurable Program Analysis (CPA) $\mathbb{P} = (D_{\mathbb{P}}, \leadsto_{\mathbb{P}}, \mathtt{merge}_{\mathbb{P}}, \mathtt{stop}_{\mathbb{P}})$ in terms of an abstract domain $D_{\mathbb{P}}$, a transfer relation $\leadsto_{\mathbb{P}}$, a merge operator $\mathtt{merge}_{\mathbb{P}}$, and a termination check $\mathtt{stop}_{\mathbb{P}}$.

Moreover, we can define a CPA as a composition of other CPA. CPA composition formalizes how we can plug our set-specific analysis, e.g. SafeCone or Frontier, into existing reachability analyses, such as explicit value analysis or predicate abstraction.

A CPA, either simple or composite, can be analyzed with one of the several variants [7], [10] of the basic algorithm used in Configurable Software Verification, which we reproduced in Algorithm 1.

```
input: A configurable program analysis \mathbb{P} = (D, \leadsto, \texttt{merge}, \texttt{stop}), \text{ a set waitlist of elements of } E, \text{ denoting the set of elements of the semi-lattice of } D, \text{ a set reached of reachable abstract states.}
```

output: An updated reached and waitlist.

```
1 while waitlist \neq \emptyset do
       pop \ e \ from \ waitlist
2
       for each e' with e \rightsquigarrow e' do
3
           for each e'' \in \text{reached do}
4
               // Combine with existing abstract state
5
               e_{new} := merge(e', e'')
               if e_{new} \neq e'' then
7
                   waitlist := (waitlist
8
                    \cup \{e_{new}\}) \setminus \{e''\}
                   reached := (reached \cup \{e_{new}\}) \setminus \{e''\}
           if \neg stop(e', reached) then
10
               waitlist := waitlist \cup \{e'\}
11
               reached := reached \cup \{e'\}
12
               if isTargetState(e') then
13
                   return (reached, waitlist)
14
       return (reached, ∅)
```

Algorithm 1: Basic algorithm (from Configurable Software Verification [7], [10])

Algorithm 1 differs only slightly from the one in the original presentation of Configurable Software Verification [7]. We added lines 13 and 14, because we want to stop the exploration and return as soon as a target state is found. We also consider the sets waitlist and reached as inputs, making the core analysis more amenable to extensions [8], [10], such as CEGAR [17] or finding multiple counterexamples, which requires a similar approach.

The check performed in line 13, isTargetState (e'), as mentioned, will verify whether TRUE (respectively FALSE) is part of the composite state e'. TRUE captures the portions of the state space which have been exhaustively verified, whereas FALSE corresponds to nodes in the ART pending analysis at the time the verification attempt was interrupted. In other words, the check evaluates whether any path π leading to e' satisfies $isSafeCone?(\pi)$ (resp. $\neg analyzed?(\pi)$). Any prefix of π will necessarily satisfy the negation of the check, otherwise it would have triggered the generation of a counterexample. Therefore, if the check isTargetState (e') is positive, as long as $feasible(\pi)$ holds, $\pi \in SafeCone$ (resp. $\pi \in Frontier$) since Property 2 (resp. Property 3) is satisfied by any such trace π .

If such a trace π is found, phase two collects π if its feasibility is confirmed. Regardless, Algorithm 1 is executed from where it left off, since the full internal representation, the sets reached and waitlist, was returned at the end of the previous call. This alternation between phase one and two produces a number of traces which will constitute S (resp. F) in the *execution report*.

In order to preserve the properties of ER, we require the underlying analysis to be precise, that is, it does not produce spurious counterexamples. Precise variants of different analyses, such as predicate abstraction and explicit value analysis, have been expressed as CPA [10], [8]. The actual algorithms for these techniques are based on Algorithm 1 and contain additional modifications but in both cases the composition with other CPA is still supported.

Let's now define our CPA $\mathbb{P}(A)$ $(D_{\mathbb{P}}, \leadsto_{\mathbb{P}}$ $, merge_{\mathbb{P}}, stop_{\mathbb{P}})$ with $D_{\mathbb{P}}$ based on the flat lattice for the set of all the states in the Assumption Automaton A taken as input. For the transfer relation, $e \stackrel{stm}{\leadsto}_{\mathbb{P}} e'$ if there exists a transition labeled stm from state e to state e' of the Assumption Automaton A taken as input and $e \xrightarrow{stm} \bot$ otherwise. Finally, merge_P = merge^{sep} and $stop_{\mathbb{P}} = stop^{sep}$, where $merge^{sep}(e,e') = e'$ and $\operatorname{stop}^{sep}(e,R) = (\exists e' \in R : e \sqsubseteq e')$. The operator $\operatorname{merge}_{\mathbb{P}}$ and stopp affect the precision and performance of the analysis [7]. The proposed definitions for these operators aim to increase the former possibly at the cost of the latter. In any case, the analysis can be made entirely precise by checking the feasibility before reporting any counterexample. Therefore, we define these operators for completeness but other options are entirely possible and might be desirable for performance.

We are now ready to define a composite program analysis

 $\mathcal{C}=(\mathbb{A},\mathbb{P},\leadsto_{\times},\mathtt{merge}_{\times},\mathtt{stop}_{\times}),$ where \mathbb{P} is the one just defined and \mathbb{A} is an arbitrary analysis. We will use $\mathtt{merge}_{\times}=\mathtt{merge}^{sep},$ $\mathtt{stop}_{\times}=\mathtt{stop}^{sep}$ and define the transfer relation \leadsto_{\times} such that $(l,r)\overset{g}{\Longrightarrow}_{\times}(l',r')$ iff $l\overset{g}{\Longrightarrow}_{\mathbb{A}}l'$ and $r\overset{g}{\Longrightarrow}_{\mathbb{P}}r'$.

In order to satisfy the completeness guarantees with respect to locations in the program that we put forth in subsection II-A, we only require that the underlying analysis does not merge different location states. Neither of the analyses we tried, lazy predicate analysis nor explicit value analysis, do.

It is worth emphasizing that the predicates analyzed? and isSafeCone? only play a conceptual role to make sure our implementation preserves the informal semantics of frontier traces and $safe\ cones$ discussed in Section II. We merely mapped the intuitions to the specific case of ART-based algorithms and computed the sets S and F directly from the Assumption Automaton.

IV. EVALUATION

This section aims to evaluate if our approach is capable of generating informative ERs within a reasonable time (with respect to the time budget invested in the original verification attempt). We analyze the performance of our proof-of-concept implementation with a set of standard benchmark instances. We also discuss the insights that we extracted from the output on this set of benchmarks.

All the files necessary to reproduce the experiments are available online: https://github.com/rcastano/cpachecker-1/tree/submission_ase.

A. Performance

We evaluated our algorithms using the families SystemC and DeviceDrivers of the SV-COMP [3] set of benchmarks, which were used previously to evaluate CMC. Our experiments consisted of two different phases: 1) a verification attempt with a predefined time limit of 900 seconds; 2) production of ERs for the instances which ended the first phase with inconclusive results.

We used an Ubuntu 16.04 system equipped with an Intel® CoreTM i7-3770 CPU clocked at 3.40GHz with 16GB of DDR3 memory for the experiments in a system without a swap partition running. We used BenchExec [9] to run the experiments and only allowed access to a single CPU core and 12GB of RAM.

We ran the verification phase over all the SV-COMP instances included in the reproduction package² of the original CMC presentation [6]. These benchmarks include instances from the sets SystemC and DeviceDrivers, comprising a total of 68 instances. We used explicit value analysis (EV) and predicate abstraction (PA), leaving 9 and 16 instances, respectively, with inconclusive results.

In the second phase, for each of these executions interrupted due to reaching the time limit, we generate the corresponding ER. To do so, we also experimented with both techniques, leading to 4 combinations of techniques, namely, EV-EV, EV-

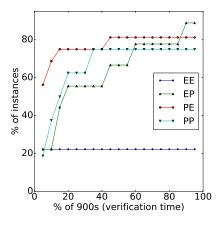


Figure 4: Time until first element of S or F is produced

PA, PA-EV and PA-PA, where EV-PA denotes using EV for the first phase and PA for ER generation. For each combination, we considered two configurations, one that finds a single trace for each of S and F, to assess how early the second phase can produce output, and another one where we configure CPA-checker to continue listing counterexamples until exhausting its abstract state space, to determine the performance when generating the components to completion.³

Tables I to IV include the full results of the second phase when running to completion. The number of traces is ommitted for instances that did not yield conclusive results (for instance due to reaching the time limit or limitations of the analysis), as indicated with the dash. The column labeled "Full?" indicates with a checkmark (\checkmark) when the component (either S or F) was generated to completion within the time limit.

We will mostly focus on the number of full components generated, that is, the number of instances for which the component, either S or F, is generated to completion within the allotted time, as indicated by the fraction below the second column for each combination of techniques.

Tables II and IV show that both generating the component S and the component F to completion seems possible for a significant number of instances when the Assumption Automaton was produced by lazy predicate abstraction. Furthermore, using either lazy predicate abstraction again (right) or explicit value (left) for the generation of S shows similar performance results, with a slightly better performance of the latter.

In the case of F, there seems to be a greater difference in performance when using explicit value analysis (left) with respect to using lazy predicate abstraction (right) again for ER generation.

Table IV suggests that using a different technique to generate the F component than the one used for verification could yield greater performance. This pattern also shows up in Table III, where using lazy predicate abstraction (right)

²Available online: https://www.sosy-lab.org/~dbeyer/cpa-cmc/

³It is worth noting that a full ER component will satisfy the completeness guarantee with respect to locations in the program but will most likely not contain all valid traces.

	Safe: explicit from explicit-AA		Safe: predicate from explicit-AA				
	# traces	Full?	CPU time	# traces	Full?	CPU time	
gigaset.BUG.c	-		927.44s	1	✓	417.08s	
farsync.BUG.c	-		926.65s	1	✓	280.36s	
loop.BUG.c	-		901.08s	-		135.17s	
synclink_gt.BUG.c	1	✓	883.54s	2	✓	534.85s	
ppp_generic.BUG.c	1	✓	894.03s	1	✓	855.15s	
lirc_imon.BUG.c	-		901.05s	-		911.77s	
token_ring.14.BUG.c	19	✓	25.93s	-		902.45s	
transmitter.16.BUG.c	7	✓	16.43s	-		901.97s	
toy.c	-		970.09s	0	✓	893.52s	
		4/9 Full			5/9 Full		

Table I: Complete results for S from an Assumption Automaton generated using Explicit Value analysis

	Safe: explicit from predicate-AA		Safe: predicate from predicate-AA			
	# traces	Full?	CPU time	# traces	Full?	CPU time
toy1_BUG.c	0	✓	14.15s	0	✓	52.47s
token_ring.06.c	0	✓	48.40s	0	✓	272.59s
pipeline.c	0	✓	7.66s	0	✓	10.93s
token_ring.09.BUG.c	-		901.05s	-		901.07s
token_ring.04.c	0	✓	20.60s	0	✓	78.64s
token_ring.05.c	0	✓	50.49s	0	✓	299.75s
token_ring.08.c	0	✓	367.83s	-		901.09s
token_ring.14.BUG.c	-		963.61s	-		901.07s
mem_slave_tlm.3.c	0	✓	8.72s	0	✓	27.59s
token_ring.07.c	0	✓	108.09s	-		901.08s
mem_slave_tlm.5.c	0	✓	15.80s	0	✓	145.01s
mem_slave_tlm.4.c	0	✓	9.00s	0	✓	27.56s
kundu.c	0	✓	16.90s	0	✓	135.16s
pktcdvd.BUG.c	-		900.97s	5	✓	166.12s
toy.c	0	✓	13.91s	0	✓	97.82s
token_ring.03.c	1	✓	16.43s	0	✓	68.03s
		13/16 Full			12/16 Full	

Table II: Complete results for S from an Assumption Automaton generated using Predicate analysis

	Frontier: explicit from explicit-AA		Frontier: predicate from explicit-AA			
	# traces	Full?	CPU time	# traces	Full?	CPU time
gigaset.BUG.c	-		930.02s	-		917.01s
farsync.BUG.c	- 1		918.63s	13	✓	98.98s
loop.BUG.c	-		937.49s	4	✓	153.23s
synclink_gt.BUG.c	-		917.86s	-		1000.97s
ppp_generic.BUG.c	-		901.01s	30	✓	94.69s
lirc_imon.BUG.c	-		901.05s	-		912.70s
token_ring.14.BUG.c	4	✓	12.65s	4	✓	16.58s
transmitter.16.BUG.c	10	✓	19.59s	10	✓	22.80s
toy.c	-		901.02s	-		931.81s
		2/9 Full			5/9 Full	

Table III: Complete results for F from an Assumption Automaton generated using Explicit Value analysis

	Frontier: explicit from predicate-AA		Frontier: predicate from predicate-AA			
	# traces	Full?	CPU time	# traces	Full?	CPU time
toy1_BUG.c	10	✓	20.44s	23	✓	133.11s
token_ring.06.c	153	✓	83.51s	-		910.96s
pipeline.c	1	✓	8.93s	1	✓	19.71s
token_ring.09.BUG.c	-		1000.85s	-		901.10s
token_ring.04.c	29	✓	37.28s	136	✓	527.54s
token_ring.05.c	85	✓	78.29s	-		900.90s
token_ring.08.c	871	✓	628.35s	-		905.49s
token_ring.14.BUG.c	-		1000.78s	-		939.53s
mem_slave_tlm.3.c	5	✓	14.97s	5	✓	25.82s
token_ring.07.c	337	✓	188.40s	-		910.68s
mem_slave_tlm.5.c	14	✓	45.17s	18	✓	302.88s
mem_slave_tlm.4.c	6	✓	16.07s	6	✓	27.05s
kundu.c	15	✓	32.30s	-		292.07s
pktcdvd.BUG.c	-		901.07s	39	✓	274.03s
toy.c	10	✓	19.93s	23	✓	137.26s
token_ring.03.c	2	✓	17.29s	3	✓	61.84s
		13/16 Full			9/16 Full	

Table IV: Complete results for F from an Assumption Automaton generated using Predicate analysis

Verification	explicit	predicate	explicit	predicate
ER	predicate	predicate	explicit	explicit
\overline{F}	55.56 %	50 %	22.22 %	75 %
S	22.22 %	75 %	22.22 %	81.25 %

Table V: Percentage of instances producing a full ER within 50% of the original verification time (900s)

for the ER generation phase outperformed using explicit value analysis for an Assumption Automaton generated using explicit value analysis.

Tables I and III show a lower number of instances for which the components were produced to completion within the allotted time, compared to the case when the Assumption Automaton was produced after an initial verification attempt using lazy predicate abstraction. This could be explained by the size of Assumption Automata produced when using explicit value analysis, which is usually significantly larger than those produced with predicate analysis.

We consider these results encouraging in general, taking into account that the instances considered are those for which the initial verification attempt already exceeded the time limit.

Table V aggregates these results and shows the percentage of instances for which a full ER was generated within 50% ($450\,\mathrm{s}$) of the original verification time ($900\,\mathrm{s}$). This table essentially measures how often the ideal condition holds, that is: both S and F are produced to completion within a fraction of the original verification time. While the first, second and last column, in our opinion, suggest that standard techniques can achieve good performance and generate full ERs for widely dissimilar verification techniques, the third column shows that producing full ERs can, in some cases, demand significant computation, relative to the original verification time. The latter finding comes as no surprise, since our approach to generating ERs constitutes a verification task in itself. Nevertheless, it seems clear to us that consistently generating full ERs requires further work.

However, we are also interested in understanding how fast, relative to the original verification time, our implementation starts generating output. Figure 4 shows the percentage of instances for which an element of either F or S is produced. Figure 4 suggests that a fraction of the original verification time can be sufficient to start generating traces.

We consider these performance results encouraging for a proof-of-concept implementation and discuss some promising ideas for further improvement in Section VI.

B. Number of traces

We mentioned a completeness criterion with respect to the statements of the system-under-verification, but this only provides a lower bound in the number of traces. Tables I to IV show the number of traces that each component (S and F) contains.

The numbers in Table II prompted us to investigate the cause for the lack of *safe cones*. The underlying reason seems to be that reverse post-order is used as the traversal strategy for lazy predicate abstraction. This strategy heavily deprioritizes nodes with no successors in the CFA. In particular, a final return statement is not analyzed unless no other option exists. This exploration, unless additional specific configuration options are used, causes the analysis to seldom produce *safe cones*.

This detailed inspection prompted by Table II allowed us to gain insights on the inner workings of the technique. Moreover, wider availability of Execution Reports could provide an incentive for tool implementers to make implementation decisions that lead to richer intermediate results, which would be reflected in the corresponding Execution Reports.

Tables II and III show that in many cases the number of traces produced remains manageable: within the few dozen and in many cases less than 5. We consider these number encouraging, since little effort on behalf of the user would be required to inspect the traces and assess their usefulness.

However, Table IV shows that for a few cases, the number of traces produced can exceed the hundreds. In these cases, depending on the particular instance, it could be possible to group traces or inspect only a few, in both cases still gaining non-trivial information about the incomplete verification attempt with minimal effort.

C. Discussion

This section aims to shed light on the insights that can be extracted from ERs in practice. With this goal, we manually inspected the Execution Reports produced for the families SystemC and DeviceDrivers of the SV-COMP benchmark and also for combined instances used to validate CMC [6] and gained some anecdotal insights worth discussing.

Extracting insights from the ERs required knowledge about the instances. However, a brief inspection of the code, guided by the output of our tool, yielded the necessary information. The following features appeared repeatedly throughout the benchmark instances.

In all instances where the Frontier component was finished we identified seemingly relevant behaviors that had not been analyzed. More precisely, both SystemC and DeviceDrivers instances consist of a main while-loop with a non-deterministic termination condition and a set of methods from which one is chosen also non-deterministically and subsequently called. In all of the instances the Frontier component contained traces that did not even reach the end of the first loop iteration. We exemplified this sort of output in Example 1, where the initialization loop could not be entirely analyzed under certain non-deterministic choices. These insights contrast starkly with a coverage metric provided by CPAchecker. Contrary to the indications of insufficient analysis reflected in the execution report, the coverage metric provided by CPAchecker reported over 85% line coverage for 11 out of the 16 instances when

```
void main () {
int x = nondet();
if (x) main0 ();
if (!x) main1 ();
}
```

Figure 5: Combined instance

applying lazy abstraction. This type of feedback could also be used to better understand the effects of either resource bounds or iteration bounds on the progress of the exploration.

Generating insight from an element $e \in S$ requires not only knowledge of the instance but also understanding how e constrains the execution from that point on. For some instances, further research is needed to properly evaluate the relevance of each element $e \in S$. However, for the combined instances, it was fairly easy to interpret ERs and they showed a relevant set of behaviors were safe. These instances have the structure shown in Figure 5, where method main 0 corresponds to the main method of a SystemC instance and main1 corresponds to the main method of a DeviceDrivers instance. Much like the setting we showed in Example 2, where one branch of an if-statement was easier to verify than the other, in this case main0 is significantly less challenging, for a specific technique, than main1. In these examples, S would contain the trace int x = nondet();, if (x), main 0(). The trace only constrains the value of x, which has to be positive, but x is a local variable, therefore main 0 is absolutely unconstrained and has been completely verified.

V. RELATED WORK

Conditional model checking [6] (CMC) is an approach where model checkers are extended to produce results even when the verification run could not be completed successfully. The output, in its general form, is a condition under which the program can be safely run. CPAchecker [7] instantiates CMC by generating an Assumption Automaton. We use this implementation to produce the ERs. ERs introduce the notions of frontier and safe cone to characterize the state space denoted by structures like Assumption Automata. The lack of any feasibility guarantees in Assumption Automata has significant consequences. A user might be misled by the size of the Assumption Automaton since a vast Automaton might correspond to a minuscule number of concrete feasible executions and also the other way around. We overcome this limitation by formally characterizing the properties of our output and adding explicit feasibility guarantees.

A slightly different approach [15], [16] to providing feed-back of partial verification results consists of a language extension to be used to annotate assumptions made during verification. This extension can be used to annotate the code and explicitly state conditions under which the program is guaranteed to run safely. These annotations are especially well-suited for local assumptions, sometimes used during manual verification, and for uniform assumptions, such as the absence of integer overflows, which are not affected by the context in

which they occur. However, these annotations are not well-suited to state assumptions made by some techniques, such as those based in unrolling loops [15] or those tackled by Assumption Automata, and as such, they are incomparable to our approach, which can provide value in these cases. One of the use cases of these annotations is to complement the verification efforts and produce a small test suite. This idea of testing to complement earlier verification efforts was later replicated [18] using Assumption Automata as input.

A recent extension of the Dafny IDE [26], [14] provides, as one of its many features, hints about parts of a specification that might cause timeouts. However, given the modular nature of the tool and the sort of specifications shown as examples, the approach tackles a different problem than ours and the feature might not be applicable in our setting.

There is also previous work on quantifying partial model checker explorations based on usage profiles [27]. These estimations are based on abstract models of behavior and heavily depend on the provided usage profile. A similar approach [20] works applying symbolic execution over the source code of a system, without the need for an abstract model, but in this case, the implementation requires finite domains for all input variables, as well as a usage profile for each of them. Reliability as they define it can be hard to interpret and, once again, could be extremely sensitive to the usage profile provided. Both techniques can be used in conjunction with ours providing different value.

The modeling language Alloy [22] enables its users to specify structural properties. An extension of the Alloy Analyzer [19] highlights parts of the specification that are "problematic" or "hard", in the authors' own words, by monitoring the activity of variables and clauses in the underlying SAT solver. The output is inherently heuristic, in contrast, our technique and proposed implementation provide strong guarantees backed by a formal definition of the semantics of the output generated. The ideas behind the Alloy Analyzer extension could also be applied in conjunction with our techniques to provide additional information.

Our work is heavily influenced by the ideas and tool support of witness validation [4], [2], which we leverage as a machine-readable representation of exploration progress. However, we aim at enabling a richer manual interaction whereas that line of work also attempts to increase tool automation and reduce the need for manual inspection.

VI. CONCLUSIONS AND FUTURE WORK

Software model checking is already capable of handling industrial instances and produce valuable results. However, some instances still remain intractable for full verification. Our work provides users with a different way to observe the progress achieved during an incomplete verification attempt by producing an execution report (ER).

We formulated the concepts of analyzed and safe cone traces and formalized the notion of ERs. We also discussed a proof-of-concept implementation to generate ERs and subsequently evaluated it both qualitatively and quantitatively with

benchmark instances.

One line of research we plan to follow involves exploring ways to abstract the traces included in the execution reports for easier visualization and understanding. In this setting, it could be useful to define both existential and universal semantics for abstract traces in the sense that some property applies to the some or every concretization of these abstractions. For instance, guaranteeing that every concretization has been analyzed, could be useful and would pose interesting challenges. In a similar line, to better assess the relevance of an element $\pi \in S$, we need to devise meaningful views and metrics of the possible continuations of e, e.g. statement coverage metrics of the cone defined by π .

We would also like to analyze how our technique performs for a specific verification technique and varying time limits.

It would be desirable to conduct a user study to assess the effectiveness of our approach once more competing output representations become available.

We intend to look into alternative usages of our output. For example, elements of an *execution report* can be leveraged as additional input to choose the right algorithm [28] to proceed after an incomplete verification attempt.

As mentioned in Section II, the partition of system behaviors into the subsets proposed is also applicable to verification techniques beyond those already implemented using ARTs: Corral, DSE, techniques based on inlining or loop unrolling among other. Several other verification systems already produce specification violation witnesses [2] in a machine-readable format closely related to that of Assumption Automata. Producing Assumption Automata for incomplete executions of many of these software model checkers seems possible, making our execution reports immediately available to them. Making the necessary changes to these tools and evaluating our approach could bring new insights and challenges worth looking into.

We also consider looking into performance improvements in the ER generation phase, for example using techniques that trade off soundness for efficiency. More precisely, instead of using a verification tool for ER generation, we could use simulation or graph exploration techniques that are not necessarily exhaustive.

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