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Nanoscale Devices for the end of the Roadmap

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Abstract

Future Nanoelectronic devices face substantial challenges, in particular increased power consumption, saturation of performance, large variability and reliability limitation. In this respect, novel device architectures using innovative materials will be needed for Nanoscale FETs.
This paper presents promising solutions for the end of the roadmap with Multigate NanoMOSFETs, Tunnel transistors, Ferroelectric FET, and Hybrid Nanocomponents using 2D and 1D nanostructures and other alternative materials, that will allow to boost the performance of these advanced nanotransistors.

1. Introduction

The significant increase of power consumption and heating is one of the main limitation of IC integration and performance [1,2].
Innovative technologies, materials, and devices are needed for the next technology nodes in the next 2 decades. In particular, NanoCMOS and Steep Switch Nanoelectronics Devices will require disruptive concepts, nanomaterials and architectures in order to reach the ambitious targets of the new IRDS Roadmap. The paper will focus on the main challenges and solutions for very low power and high performance nanoscale devices in the CMOS and Beyond CMOS domains.

2. NanoCMOS

Future ICs are facing dramatic challenges in performance as well as static and dynamic power consumption, which could be overcome using disruptive concepts, device architectures, technologies and materials. Promising solutions for nanoCMOS include III-V/Ge channels, 2D layers, Multi-gates structures, Nanowires (NW) and Carbon NanoTubes (CNT).
In this field, several very interesting advances have been recently shown. Device architectures allowing to almost reach the subthreshold slope limit S, of 60mV/dec at room temperature for MOSFETs, have been investigated for the end of the Roadmap.

The best MOSFET devices leading to S close to its minimum value are using fully depleted [3-6] channels (e.g. FD SOI with very thin buried oxide [6]) or fully inverted ones, with volume inversion [7], that is even better to optimize the control of the electrostatics [8] of the structure (e.g. Double-gate, Bulk or SOI Tri-gate/FinFET, Gate-All-Around MOSFET or Nanowire FET).
First Multi-Gate MOSFET with volume inversion was shown in 1987 [7]. These devices allow to greatly reduce short channel effects compared to single gate MOSFETs, whatever the doping of the channel is (Fig. 1) [8].

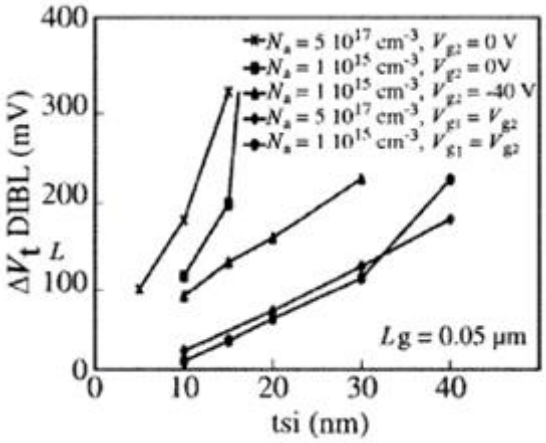
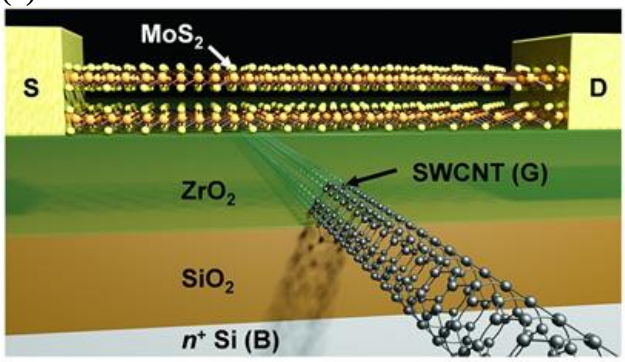


Figure 1. DIBL effect versus silicon film thickness for 50nm single gate SOI MOSFETs (tox2 = 380 nm tox1 = 3 nm) with high doping (Na = 5 × 10^{17} cm–3, Vg2 = 0 V), low doping (Na = 10^{15} cm–3, Vg2 = 0 V), back channel accumulation (Na = 10^{15} cm–3, Vg2 = –40 V), and for Double Gate SOI MOSFETs (tox1 = tox2 = 3 nm, Na = 10^{15} cm–3 and Na = 5 × 10^{17} cm–3 with Vg1 = Vg2).

Ultra short MOSFETs (1nm) have recently shown very good transfer characteristics. The electrical characteristics for a 1D gate 2D channel FET with a bilayer MoS2 layer (Fig. 2a) [9] show that the MoS2 extension regions (the underlapped regions between the SWCNT gate and S/D contacts) could be heavily inverted (i.e., n+ state) by applying a positive back-gate voltage of VBS = 5 V to the Si substrate. The ID-VGS characteristics for the device at VBS = 5 V and VDS = 50 mV and 1 V (Fig. 2b) demonstrate the ability of the 1-nm SWCNT gate to deplete the MoS2 channel and turn Off the device. The 1D2D-FET exhibited excellent subthreshold characteristics with a near ideal slope of 65 mV/dec at room temperature and On/Off current ratio of

10^6. The output characteristics and transfer characteristics vs VBS are also shown (Fig. 2b).

(a)



(b)

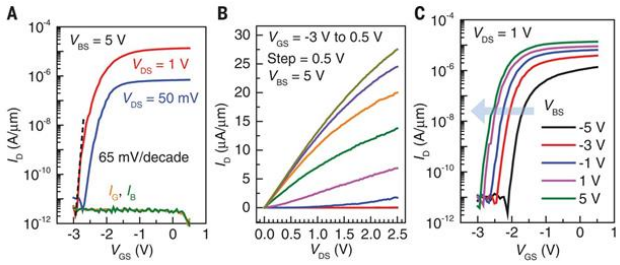


Figure 2. (a) Bilayer MoS2 1nm gate length controlled by a Single Wall Carbon NanoTube as the gate with ZrO2 gate oxide, (b) Electrical characterization of 1D2D-FET: (A) ID-VGS characteristics of a bilayer MoS2 channel SWCNT gated FET at VBS = 5 V and VDS = 50 mV and 1 V. (B) ID-VDS characteristic for the device at VBS = 5 V and varying VGS. (C) ID-VGS characteristics at VDS = 1 V and varying VBS illustrating the effect of back-gate bias on the extension region resistance

3. Tunnel FETs, Negative Capacitance MOSFETs and Hybrid Devices

-Tunnel FETs, Negative Capacitance MOSFETs:

In order to reduce static and dynamic power consumption in nanoscale FETs at the end of the Roadmap, sub-60mV/dec subthreshold swing (e.g. TFET, NC/FE-FET) are needed (Fig. 3) [10]. Figure 3 presents the comparison of the theoretical subthreshold swing for some of the most advanced nanoscale FET architectures and materials of the literature as the function of the gate length. The IRDS (International Roadmap for Devices and Systems) needs for logic devices are also shown vs time horizons. The best performance for the swing of CMOS devices at the end of the Roadmap close to 60mV/dec) are obtained for Multi-gate (Omega Gate in the figure) Nanowire FET with very small wire diameter (3nm) and Double Gate MOSFET with TMD (MoS2 in the figure) channel. However, at the end of the next decade, sub-60mV/decade swing could be needed, which can only be obtained with small slope switches (some examples with Tunnel FET with III-V or 2D channels in the figure).

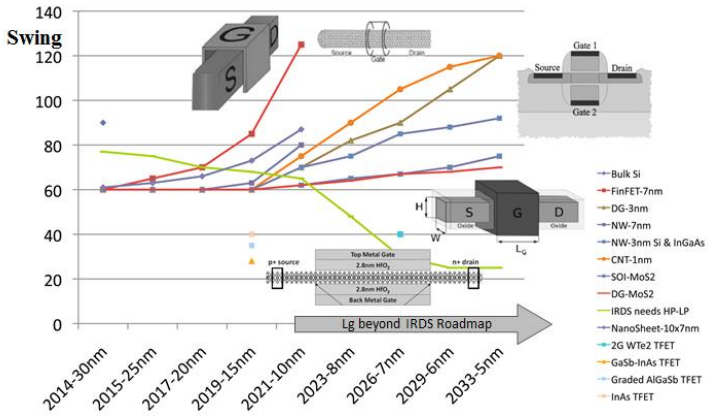


Fig. 3. Advanced simulations of subthreshold swing (mV/decade) vs. gate length (beyond the IRDS Roadmap for the gate length) or time horizon for various device architectures (Bulk Si, FinFET, Double Gate, Nanowire with various diameters, Carbon NanoTube, MOSFET on Insulator, Nanosheet) and channel materials (Si, InGaAs, InAs, Heterojunction GaSb-InAs, Graded AlGaSb, MoS2, WTe2), compared with IRDS needs (2017 Roadmap) for the next 15 years

The combination of a ferroelectric gate material and advanced MOSFET architectures also improves the subthreshold slope below the 60 mV / dec limit of traditional MOSFETs.
FinFETs using a ferroelectric gate ($HfZrO_2$) and a Ge channel, and therefore a negative capacitance (NC), have recently experimentally exhibited a sub-60 mV slope, down to 43 mV/dec, which could lead to larger driving current than TFETs (Fig. 4) [11].

SOI MOSFET realized with PZT and HfO2/SiO2 gate in order to obtain a non-hysteretic Ferroelectric SOI FET with positive Ctotal has also recently been fabricated. A swing down to 20mV/dec has been demonstrated (Fig. 5) [12].

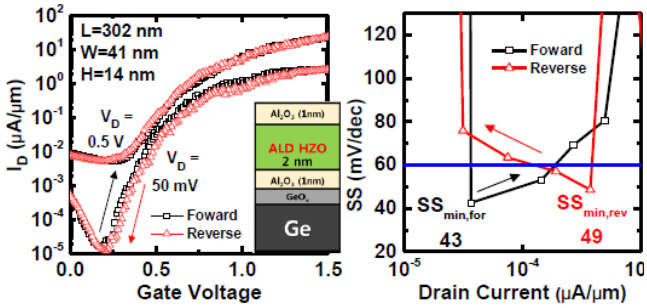


Fig.4. Ge channel FE-FET with HfZrO2 ferroelectric gate showing sub-60mV/dec subthreshold swing in forward and reverse modes

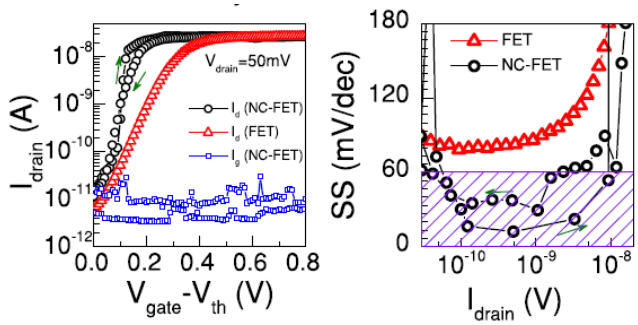


Fig. 5. Large surface SOI MOSFET, tsi=30nm, tox2=145nm, with PZT + HfO_2/SiO_2 gate for non-hysteretic FE SOI FET with positive Ctotal

GAA NanoSheet (NS) NC FET have shown promising performance compared with conventional Hf02 gate dielectrics (Fig. 6). A sub-60 mV/dec is demonstrated for 4 decades of Id in NC(HZO) NS-GAA [13].

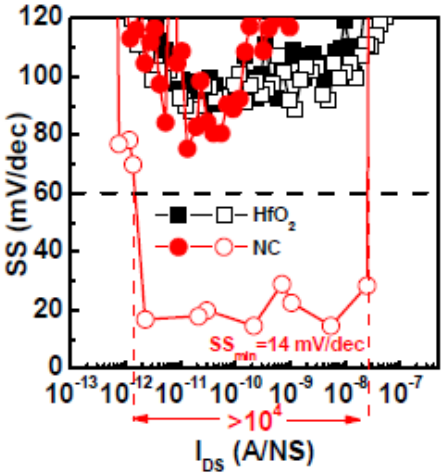
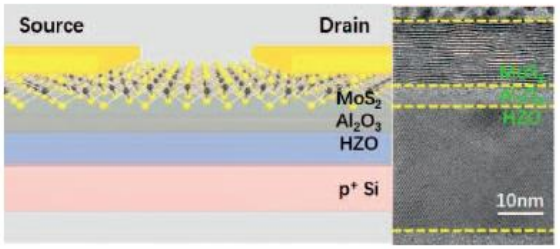


Figure 6. Swing of NC(HZO) NanoSheet-GAA compared with MOSFET on conventional Hf02 dielectrics. Vd=0.2V, TNS=20nm, WNS=90nm, Lg=450nm,

The combination of 2D MoS2 materials with NC FETs is also an interesting solution for very low voltage applications. Several layers of MoS2 have been used with an HZ0 NC material, highlighting sub-60mV/dec SS for several decades of current at 300 and 100K (Fig. 7) [14].



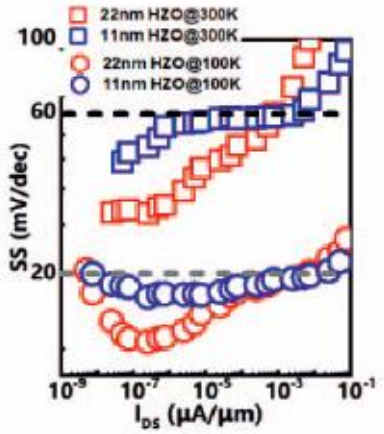


Figure 7. Subthreshold Swing of multilayer 2D MoS2 NC MOSFET vs Id at 300K and 100K for several HZO thicknesses

-Hybrid devices:

An Hysteresis-Free Negative Capacitance InGaAs Tunnel FET has recently been shown with a minimum swing of 40mV/dec, inducing a substantial improvement compared with the baseline TFET (Fig. 8), with an increase of I_{60} by 2 decades [15].

Other hybrid devices have also demonstrated interesting properties, such as a swing of 4 mV/dec in phase-change TFET with a vanadium dioxide layer in the gate undergoing a metal-insulator transition under electrical excitation (Fig. 9) [16].

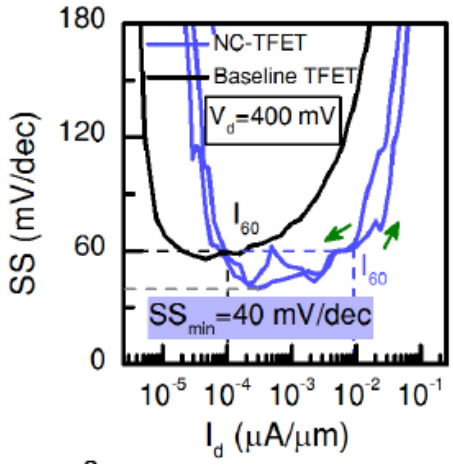


Figure 8. Comparison of SS vs Id for NC InGaAs TFET with baseline TFET.

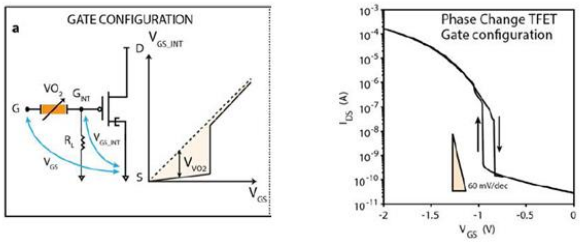


Fig. 9. Phase change Tunnel FET with S~4mV/dec at 300K for 3 decades of drain current, using a vanadium dioxide.

Another hybrid device using a metal filament (Ag or Cu) formed at the drain of a Si MOSFET under sufficient applied bias, led to a sharp subthreshold slope for several decades of drain current (Fig. 10) [17].

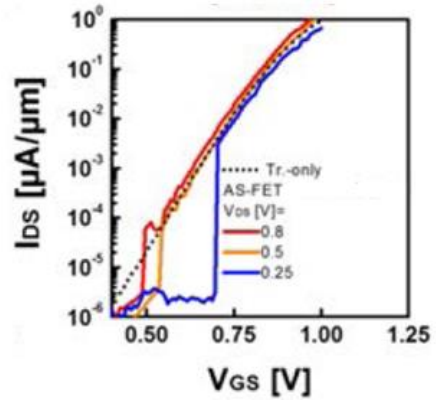


Fig. 10. Metal filament (Ag, Cu) formed in Si at the Drain with a sufficient bias ; S~5mV/dec for Atom Scale metal filament MOSFET at Vd=0.25V and 300K for several decades of Id

Acknowledgements

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Conclusion

In this paper, the main challenges and solutions for very low power and high performance nanoscale devices in the CMOS and Beyond CMOS domains have been highighted. In particular, ultimate MOSFET and Small Slope Switches using innovative 1D and 2D architectures and advanced alternative materials have been addressed for reaching the end of the Roadmap.

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