Tutorial Three

Trends and Challenges in VLSI Technology Scaling Towards 100nm

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Abstract

Moore's Law drives VLSI technology to continuous increases in transistor densities and higher clock frequencies. This tutorial will review the trends in VLSI technology scaling in the last few years and discuss the challenges facing process and circuit engineers in the 100nm generation and beyond. The first focus area is the process technology, including transistor scaling trends and research activities for the 100nm technology node and beyond. The transistor leakage and interconnect RC delays will continue to increase.

The tutorial will review new circuit design techniques for emerging process technologies, including dual Vt transistors and silicon-on-insulator. It will also cover circuit and layout techniques to reduce clock distribution skew and jitter, model and reduce transistor leakage and improve the electrical performance of flip-chip packages.

Another focus area is the circuit design and the techniques used to minimize capacitive and inductive noise. The tutorial will review models of electrical interconnects, including inductance and skin effect. These models are used to estimate the performance of electrical interconnects, including delays, data-rates and power consumption for on-chip and off-chip interconnects and for clock distribution.

Integrating analog circuits on large digital chips presents significant challenges, primarily due to substrate noise coupling. This tutorial will describe a strategy for making analog circuits less sensitive to substrate bounce, including examples for epi-type CMOS technology.

Finally, the tutorial will review the test challenges for the 100nm technology node due to increased clock frequency and power consumption (both active and passive) and present several potential solutions.

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on microprocessor design with focus on clock and power distribution, packaging, standard cell libraries, CAD and circuit design methodologies. He re-joined Intel Corp. in 1996 working on the clock and power distribution, cell library, I/O buffers and packaging of the first Itanium microprocessor. He is presently developing circuit design methodologies for Intel's 100nm process generation. He received the MSEE degree from the Polytechnic Institute in Bucharest, Romania. He has published numerous technical papers and has been an invited speaker at several conferences. Stefan currently holds 12 U.S. patents with several more pending. He is a Senior Member of IEEE and has been a member of the ESSCIRC Technical Program Committee since 1998.

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***Bram Nauta** was born in Hengelo, The Netherlands, in 1964. In 1987 he received the M.Sc. degree (cum laude) in Electrical Engineering from the University of Twente, Enschede, The Netherlands. In 1991 he received the Ph.D. degree from the same university on the subject of analog CMOS filters for very high frequencies. In 1991 he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, The Netherlands, where he worked on high speed AD converters. >From 1994 he led a research group in the same department, working on "analog key modules". In 1998 he returned to the University of Twente, as full professor heading the IC Design group in the MESA+ Research Institute and department of Electrical Engineering. His current research interest is analog CMOS circuits for transceivers. He is also part-time consultant in industry and in 2001 he co-founded Chip Design Works. His Ph.D. thesis was published as a book: Analog CMOS Filters for Very High Frequencies, Kluwer, Boston, MA, 1993. He holds 8 patents in circuit design and he received the "Shell Study Tour Award" for his Ph.D. Work. From 1997-1999 he served as Associate Editor of IEEE Transactions on Circuits and Systems -II; Analog and Digital Signal Processing, and in 1998 he served as Guest Editor for IEEE Journal of Solid-State Circuits. In 2001 he became Associate Editor for IEEE Journal of Solid-State Circuits.*