Robust Analytical Gate Delay Modeling for Low Voltage Circuits

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***Abstract*— Sakurai-Newton (SN) delay metric [1] is a widely used closed form delay metric for CMOS gates because of simplicity and reasonable accuracy. Nevertheless it can be shown that the SN metric fails to provide high accuracy and fidelity when CMOS gates operate at low supply voltages. Thus it may not be applicable in many low power applications with voltage scaling. In this paper, we propose a new closed form delay metric based on the centroid of power dissipation. This new metric is inspired by our key observation and theoretic proof that the SN delay is indeed Elmore delay, which can be viewed as the centroid of current. Our proposed metric has a very high correlation coefficient (≥ 0.98) when correlated with the actual delays got from the HSPICE simulations. Such high correlation is consistent across all major process technologies. In comparison, the SN metric has a correlation coefficient between $(0.70, 0.90)$ depending upon the technology and the CMOS gate, and it is less accurate for lower supply voltages. Since our proposed metric has high fidelity across a wide range of supply voltages yet a simple closed form, it will be very useful to guide low voltage and low power designs.**

I. Introduction

Accurate yet efficient delay modeling is important to guide design optimization, such as transistor and gate sizing, interconnect optimization, placement, and routing. Closed form delay equations with high accuracy is desirable since they are efficient and easy to implement. The alternative to the closed form delay metrics are the lookup tables. The lookup tables though accurate are less attractive since they are computationally expensive to use within an optimization loop and provide little insight [2]. The delay modeling consists of two distinct components, the gate and the interconnect delay modeling.

In the literature, significant amount of work has been devoted to *interconnect delay* characterization. The interconnects are often modeled as RC trees. The widely used Elmore delay is the first moment of the impulse response of the RC tree [3]. To improve the accuracy of the Elmore delay, models based on the higher order moment matching AWE [4] have been proposed. But AWE is expensive to use in optimization since it lacks closed-form expression. To improve the accuracy of Elmore delay and retain its simplicity, several works have proposed delay models that are functions of the higher moments of the impulse response of the RC tree [2], [5], [6]. Another fast approach is the matching the moments of the impulse response to a Probability Density Function (PDF) [7]–[10]. In the literature, the *gate delay* characterization has received lesser attention compared to the interconnect delay characterization. The Sakurai-Newton (SN) delay approximation [1] is a widely used closed-form delay metric for the CMOS gates because of simplicity and reasonable accuracy. Nevertheless the SN metric lacks accuracy when the CMOS gates operate at low supply voltages [11]. But for the nanometer SoC designs, delay modeling needs to address the heterogeneous nature, such as voltage scaling/voltage islands. Thus the delay model needs to be robust across a wide range of operating scenarios.

In this paper, we propose a new, robust closed form gate delay metric based on the centroid of power dissipation. This new model is inspired by our key observation and theoretic proof that the SN metric can be viewed as the centroid of current dissipated by the gate. The proposed metric has a very high correlation coefficient (≥ 0.98) when correlated with the actual delays got from the HSPICE simulations. Such high correlation is consistent across all major process technologies. In comparison, the SN metric has a correlation coefficient between $(0.70, 0.90)$ depending upon the technology and the CMOS gate, and it is less accurate for lower supply voltages. Since our proposed metric has high fidelity across a wide range of supply voltages yet a simple closed form, it will be very useful to guide low voltage and low power designs.

To summarize, we make the following contributions:

- We show that the Elmore delay can be expressed as the centroid of current dissipated.
- We prove that the SN delay approximation is the exact Elmore delay of a CMOS gate.
- We propose a high fidelity closed form metric for the delay of a CMOS gate based on the centroid of the power dissipated by the gate.

The rest of the paper is organized as follows. Section II presents the Sakurai and Newton approximation to the delay. Section III provides the background for the Elmore delay which leads to the proof that the SN delay approximation is the exact Elmore delay of a CMOS gate. In Section IV, we propose a new closed form formula inspired by our observation that the SN delay can be viewed as the centroid of current. The experimental results are presented in Section V, followed by conclusion in Section VI.

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II. Sakurai-Newton Delay Approximation

The Shockley model for MOSFET [12] fails in the short-channel region because it neglects the velocity saturation effects. Sakurai and Newton proposed a model that takes into account the short-channel behavior while retaining the simplicity of the Shockley model [1], [13]. They modified the quadratic dependence of the drain current on the driving voltage to a α-power dependence, where $1 \leq \alpha \leq 2$ is the called the velocity saturation index.

The drain current i_D according to [1] is,

$$i_D = \begin{cases} \frac{k}{2}(v_{GS} - V_T)^{\alpha} & \text{saturation,} \\ k(v_{GS} - V_T)^{\alpha} \frac{v_{DS}}{V_{DS_{SAT}}} & \text{linear,} \\ 0 & \text{cutoff} \end{cases} \quad (1)$$

where

- $k = \left(\frac{W}{L}\right) \mu_n C_{ox}$, where μ_n is the mobility of electrons and C_{ox} is the oxide capacitance.
- $V_{DS_{SAT}}$ determines the boundary between linear and saturation regions when $v_{GS} = V_{DD}$.

For the delay *approximation* of the CMOS inverter, we assume a step input to the inverter. Thus we are finding out the inherent delay of the gate ignoring the finite rise time of the input. The delay due to finite rise time can be incorporated using techniques such as PERI [14].

Since we assume a step input, the drain current equation in (1) simplifies to,

$$i_D = \begin{cases} \frac{k}{2}(V_{DD} - V_T)^{\alpha} & V_{DD} - V_T < v_{DS} \leq V_{DD}, \\ k(V_{DD} - V_T)^{\alpha} \frac{v_{DS}}{V_{DD} - V_T} & v_{DS} \leq V_{DD} - V_T \end{cases} \quad (2)$$

where $(V_{DD} - V_T)$ is the boundary between linear and saturation regions under step input.

The main assumption in the delay approximation is that a constant saturation current I_{D0} discharges the output voltage from $v_{DS} = V_{DD}$ to $\frac{V_{DD}}{2}$.

$$t_{sn} = \frac{\Delta Q|_{\left(v_{DS} = V_{DD} \rightarrow \frac{V_{DD}}{2}\right)}}{I_{D0}} = \frac{C_L \frac{V_{DD}}{2}}{\frac{k}{2}(V_{DD} - V_T)^{\alpha}}$$

Thus the Sakurai-Newton (SN) delay metric is [1],

$$\boxed{t_{sn} \approx \frac{C_L V_{DD}}{k(V_{DD} - V_T)^{\alpha}}} \quad (3)$$

Note that this metric is an *approximation* to the delay since the transistor is assumed to be in *saturation* from $v_{DS} = V_{DD}$ to $\frac{V_{DD}}{2}$. The assumption is *weak*, since under the step input the transistor is in *saturation* region only from $v_{DS} = V_{DD}$ to $(V_{DD} - V_T)$. From $v_{DS} = (V_{DD} - V_T)$ to 0, the transistor is in *linear* region. In this paper, we model the transistor operating in saturation and linear regions as a nonlinear resistor R [11]. Thus the inverter can be modeled as an RC circuit [15] as shown in Figure 1. For an RC tree, the Elmore delay is an upper bound on the actual delay for any input waveform [16]. The theory behind the Elmore delay is discussed in the next section.

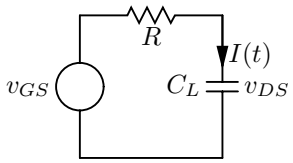


Fig. 1. The RC model of an inverter. Note that R is a nonlinear resistor modeling transistor and C_L is the load capacitance seen by the inverter.

III. Centroid of Current Based Delay

In this section, we first show that the Elmore delay of a CMOS gate is the centroid of current dissipated by it. Then we prove that the SN metric is the exact Elmore delay of the CMOS gate. This key observation will inspire us to propose a new delay metric in Section IV.

Lemma 1. *The Elmore delay of a CMOS gate is the centroid of the current dissipated by it when it is switching.*

Proof. The Elmore delay is defined as the centroid of the impulse response $h(t)$ of the system [17]. The centroid x_c of the function $f(x)$ is defined as,

$$x_c = \frac{\int_x x\ f(x)\ dx}{\int_x f(x)\ dx}$$

Thus the Elmore delay is given by,

$$t_{elmore} = \frac{\int_0^{\infty} t\ h(t)\ dt}{\int_0^{\infty} h(t)\ dt} \quad (4)$$

since $\int_0^{\infty} h(t)dt = 1$ for RC circuits with monotonic response [17] we can write (4) as,

$$t_{elmore} = \int_0^{\infty} t\ h(t)\ dt \quad (5)$$

Let $H(s)$ denote the Laplace transform of $h(t)$. The transfer function $H(s)$ is defined as the ratio of output to input voltages [18]. Since we assume a step input, the transfer function reduces to,

$$H(s) = \frac{V_{DS}(s)}{V_{GS}(s)} = \frac{V_{DS}(s)}{\frac{1}{s}} = sV_{DS}(s)$$

We apply the Inverse Laplace transform to get the impulse response, $h(t) = \frac{dv_{DS}}{dt}$. We know that the current discharged through the capacitor,

$$\begin{aligned} I(t) &= C_L \frac{dv_{DS}}{dt} \\ &= C_L h(t) \end{aligned}$$

Hence under the RC model with the assumption of step input,

$$I(t) \propto h(t) \quad (6)$$

$$t_{elmore} = \frac{\int_0^{\infty} t\ I(t)\ dt}{\int_0^{\infty} I(t)\ dt} \quad (7)$$

Thus the Elmore delay is shown as the centroid of the area under the current discharged through the load capacitor. □

We can now show the following result.

Theorem 1. *The Sakurai-Newton delay approximation is the exact Elmore delay of the CMOS gate under the following conditions:*

(i) *A step input is applied;*
(ii) *The CMOS gate is modeled as an RC circuit.*

Proof. We provide the proof when the gate is discharging. The proof is similar when the gate is charging.

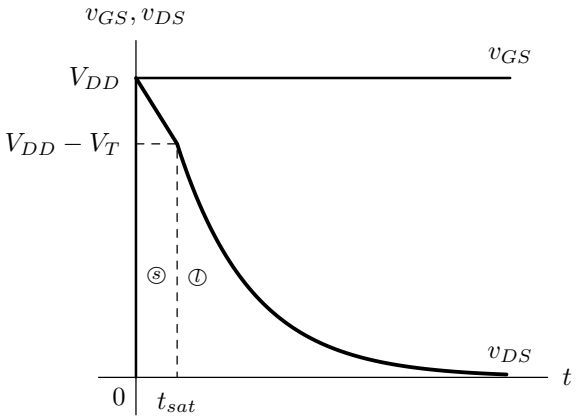


Fig. 2. Inverter waveforms when the output is discharging. The input v_{GS} is a step input. The output v_{DS} decreases linearly in the saturation region (till t_{sat}) and decays exponentially in the linear region (after t_{sat}).

The input and output voltage waveforms associated with the discharging inverter are shown in Figure 2. When a rising step input ($v_{GS} = V_{DD}\ u(t)$) is applied to the inverter, the NMOS is on while the PMOS is off. The NMOS operates in the saturation region when the output discharges from $v_{DS} = V_{DD}$ to $(V_{DD} - V_T)$ and it operates in the linear region when the output discharges from $v_{DS} = (V_{DD} - V_T)$ to 0. The time taken by the output v_{DS} to reach $(V_{DD} - V_T)$ is denoted as t_{sat}, the time at which the NMOS transistor switches from saturation to linear region of operation.

The Elmore delay integral in (7) can be written as,

$$t_{elmore} = \frac{\int_0^{t_{sat}} t\ i_{D_{SAT}}\ dt + \int_{t_{sat}}^{\infty} t\ i_{D_{LIN}}\ dt}{\int_0^{t_{sat}} i_{D_{SAT}}\ dt + \int_{t_{sat}}^{\infty} i_{D_{LIN}}\ dt} \quad (8)$$

To evaluate (8), we need closed form expressions for $i_{D_{SAT}}$, $i_{D_{LIN}}$, and t_{sat}.

When the NMOS is saturated, the output voltage v_{DS} decreases linearly from V_{DD} to $(V_{DD} - V_T)$, shown as ⓢ in Figure 2. The decrease is linear because the current is a constant during that period which is given by,

$$i_{D_{SAT}} = \frac{k}{2}(V_{DD} - V_T)^{\alpha} \quad (9)$$

When the output voltage v_{DS} goes below $(V_{DD} - V_T)$, the NMOS enters the linear region of operation, shown as ⓛ in Figure 2. The current in the linear region can be written as,

$$\begin{aligned} i_{D_{LIN}} &= k(V_{DD} - V_T)^{\alpha} \frac{v_{DS}}{V_{DD} - V_T} \\ &= \frac{v_{DS}}{R} \end{aligned}$$

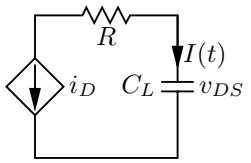


Fig. 3. RC model with discharging current as a controlled current source.

where $\frac{1}{R} = k(V_{DD} - V_T)^{\alpha - 1}$ is the resistance through which we discharge the load capacitor C_L as shown in Figure 3. We need an closed form expression for v_{DS} to evaluate $i_{D_{LIN}}$. The output voltage v_{DS} in the linear region is simply the voltage seen at the capacitor of a first order RC circuit under the step input. Thus the output voltage v_{DS} in the linear region can be written as,

$$v_{DS} = (V_{DD} - V_T) e^{\frac{-(t - t_{sat})}{RC_L}} u(t - t_{sat})$$

Thus the current during the linear region of operation can be written as,

$$i_{D_{LIN}} = k(V_{DD} - V_T)^{\alpha} e^{\frac{-(t - t_{sat})}{RC_L}} u(t - t_{sat}) \quad (10)$$

Finally we need t_{sat}, the time at which the NMOS switches from saturation to the linear region. Applying Kirchhoff current law to the output in Figure 3,

$$\begin{aligned} -C_L \frac{dv_{DS}}{dt} &= \frac{k}{2}(V_{DD} - V_T)^{\alpha} \\ -\int_{V_{DD}}^{V_{DD} - V_T} dv_{DS} &= \frac{\frac{k}{2}(V_{DD} - V_T)^{\alpha}}{C_L} \int_0^{t_{sat}} dt \end{aligned}$$

On integrating and simplifying we get,

$$t_{sat} = \frac{2C_L V_T}{k(V_{DD} - V_T)^{\alpha}} \quad (11)$$

Substituting the unknowns in (8), and evaluating the integrals we get,

$$\begin{aligned} t_{elmore} &= \frac{\frac{C_L^2 V_T^2}{k(V_{DD} - V_T)^{\alpha}} + \frac{C_L^2 (V_{DD}^2 - V_T^2)}{k(V_{DD} - V_T)^{\alpha}}}{C_L V_T + C_L (V_{DD} - V_T)} \\ \boxed{t_{elmore} = \frac{C_L V_{DD}}{k(V_{DD} - V_T)^{\alpha}}} \end{aligned} \quad (12)$$

which is the same as (3). Thus the SN delay *approximation* is the *exact* Elmore delay of the CMOS gate. □

In the nanometer regimes, the velocity saturation constant $\alpha \approx 1$. Thus (12) can be rewritten as,

$$t_{elmore} = \frac{C_L}{k\left(1 - \frac{V_T}{V_{DD}}\right)} \quad (13)$$

The SN metric (13) fails to track the delay when the supply voltages are low [11]. Taur and Ning [11] presented a simple curve fitting metric that works across a wide range of voltages. The Taur-Ning (TN) delay metric is given by,

$$\boxed{t_{tn} \propto \frac{C_L}{\left(0.7 - \frac{V_T}{V_{DD}}\right)}} \quad (14)$$

where 0.7 is a numerical fitting parameter. The TN metric suffers from the drawback of having high absolute errors compared to the actual HSPICE delays. This is further discussed in Section V. Another drawback is that it is applicable only when $\frac{V_T}{V_{DD}} \leq 0.5$ [11]. This means it may not be applied to very low V_{DD} designs.

IV. Centroid of Power Based Delay

In this section, we derive a new metric based on the centroid of power (CP) which overcomes the drawbacks of the SN and TN delay metrics.

The SN metric can roughly be thought of as a charge based delay since we integrate over current. The centroid of power can be thought of as an energy based delay since we integrate over power. The delay obtained by taking the centroid of the power at the output can be written as,

$$t_{cp} = \frac{\int_0^\infty t\ v_{DS}\ i_D\ dt}{\int_0^\infty v_{DS}\ i_D\ dt} \tag{15}$$

Since the NMOS transistor is operating in two different regions namely saturation and linear regions, (15) can be written as,

$$\begin{aligned} t_{cp} &= \frac{\int_0^{t_{sat}} t\ v_{DS_{SAT}}\ i_{D_{SAT}}\ dt + \int_{t_{sat}}^\infty t\ v_{DS_{LIN}}\ i_{D_{LIN}}\ dt}{\int_0^{t_{sat}} v_{DS}\ i_D\ dt + \int_{t_{sat}}^\infty v_{DS}\ i_D\ dt} \\ &= \frac{\frac{C_L^2(3V_{DD}-2V_T)V_T^2}{3k(V_{DD}-V_T)^\alpha} + \frac{C_L^2(V_{DD}+3V_T)(V_{DD}-V_T)^2}{4k(V_{DD}-V_T)^\alpha}}{\frac{1}{2}C_L(2V_{DD}-V_T)V_T + \frac{1}{2}C_L(V_{DD}-V_T)^2} \end{aligned}$$

which can be simplified to,

$$\boxed{t_{cp} = \frac{C_L(3V_{DD}^3 + 3V_{DD}^2V_T - 3V_{DD}V_T^2 + V_T^3)}{6kV_{DD}^2(V_{DD}-V_T)^\alpha}} \tag{16}$$

The correlation between the centroid of power (CP) delay metric and the HSPICE delay values is better than the correlation between the SN delay metric and the HSPICE delay values. The correlation attains near perfection with a modification in the Taur-Ning spirit.

We found out empirically that $\frac{1}{(V_{DD}-V_T)^2}$ tracks the delay better than $\frac{1}{V_{DD}^2}$. Substituting $(V_{DD}-V_T)^2$ for V_{DD}^2 in the denominator of (16), we get the modified centroid of power (CPM) metric,

$$\boxed{t_{cpm} \propto \frac{C_L(3V_{DD}^3 + 3V_{DD}^2V_T - 3V_{DD}V_T^2 + V_T^3)}{(V_{DD}-V_T)^2(V_{DD}-V_T)^\alpha}} \tag{17}$$

The correlation between the CPM delay metric and the HSPICE delay values is *almost perfect*. Also, the absolute error between the CPM metric and the HSPICE delay values reduces significantly compared to the other metrics discussed in this paper. A possible reason for this near perfect tracking of delay is that the gate overdrive is proportional to $(V_{DD}-V_T)$ and not to V_{DD}. An alternative way to reason about this is the fact that $\frac{1}{(V_{DD}-V_T)^2}$ has a faster rate of change compared with $\frac{1}{V_{DD}^2}$ when V_{DD} varies.

V. Experimental Results

We used the Berkeley Predictive Technology Model [19] for our simulations. The simulations were run on the INV, NAND2, NOR2, XOR2 gates for their worst case input. The load capacitance C_L was varied from $20fF$ to $50fF$. The supply voltage V_{DD} was varied from $2 \times V_{T0}$ to $6 \times V_{T0}$. The threshold voltage V_{T0} was varied within $\pm 10\%$ of its original value. The simulations were run on $45nm$, $65nm$, and $100nm$ technologies. Thus nearly 200 simulations were run on each gate for a given technology under its worst case input.

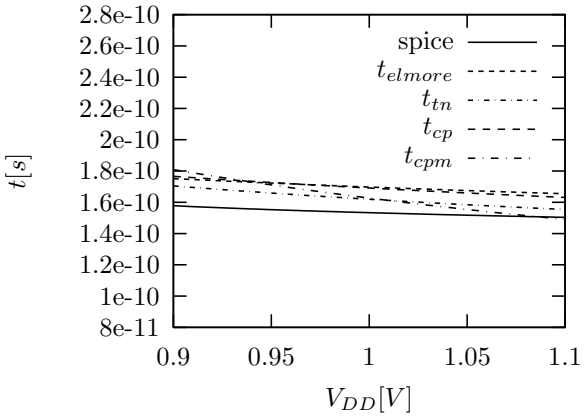


Fig. 4. HSPICE delay and the values predicted by the delay metrics for INV in $65nm$ technology under *nominal* supply voltages. The solid line is the HSPICE delay values and the dotted lines are the delays predicted by the various metrics. The V_{DD} was varied with load capacitance $C_L = 20fF$ and threshold voltage $V_{T0} = 0.22V$. Note that *all* the delay metrics track under *nominal* supply voltages.

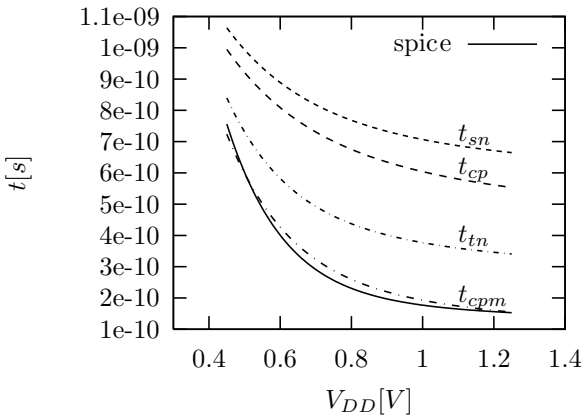
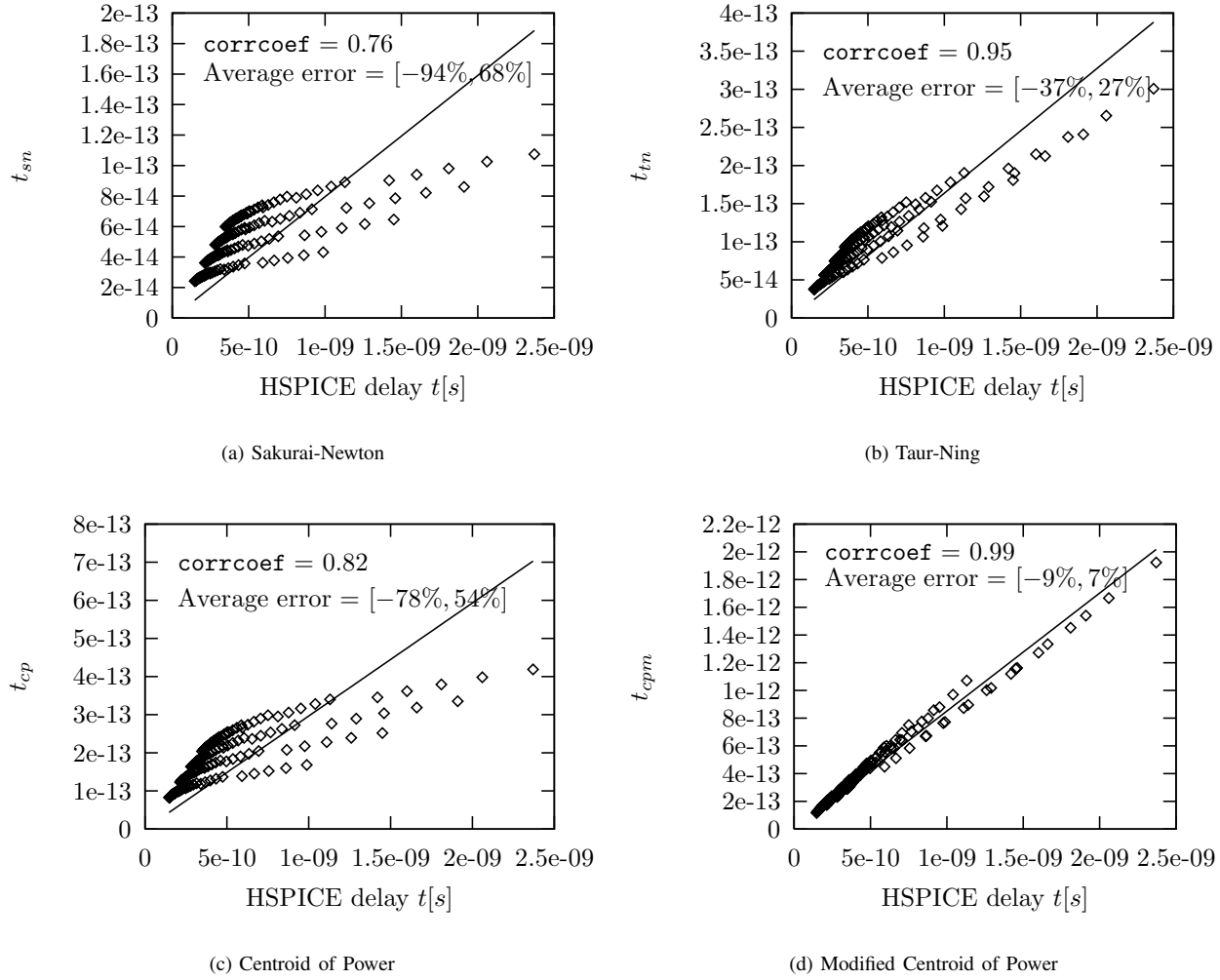


Fig. 5. HSPICE delay and the values predicted by the delay metrics for INV in $65nm$ technology. The solid line is the HSPICE delay values and the dotted lines are the delays predicted by the various metrics. The V_{DD} was varied with load capacitance $C_L = 20fF$ and threshold voltage $V_{T0} = 0.22V$. Note that only CPM can track the delay in the lower voltages while TN can track to quite an extent, the other two metrics SN and CP cannot track it.

The delay values predicted by the metrics were scaled by a constant value c. The constant c is obtained using linear regression. Suppose d_i is the delay obtained from HSPICE during the i th simulation and x_i is the delay predicted by the metric, c is obtained on minimizing $\sum_i (d_i - ax_i)^2$. Note that



(a) Sakurai-Newton

(b) Taur-Ning

(c) Centroid of Power

(d) Modified Centroid of Power

Fig. 6. Scatter plot of different delay metrics with the HSPICE delay for INV in $65nm$ technology. Since we have multiplied by the constant of proportionality, no units are provided for the y-axis.

TABLE I

THE CORRELATION OF HSPICE DELAY VALUES WITH THE DELAY METRICS ACROSS DIFFERENT TECHNOLOGIES AND GATES. THE HSPICE DELAY OF A GATE IS MEASURED FOR ITS WORST CASE INPUT COMBINATION.

Gate	$45nm$				$65nm$				$100nm$			
	SN	TN	CP	CPM	SN	TN	CP	CPM	SN	TN	CP	CPM
INV	0.76	0.97	0.81	0.99	0.76	0.95	0.82	0.99	0.90	0.99	0.94	0.98
NAND2	0.72	0.95	0.76	0.99	0.73	0.91	0.77	0.99	0.83	0.96	0.87	1.00
NOR2	0.73	0.96	0.78	0.99	0.75	0.92	0.80	0.99	0.90	0.99	0.93	0.99
XOR2	0.71	0.95	0.76	0.99	0.71	0.90	0.76	0.98	0.90	0.97	0.93	1.00

TABLE II

THE PERCENTAGE ERROR BETWEEN HSPICE DELAY VALUES AND THE DELAY METRICS ACROSS VARIOUS TECHNOLOGIES AND GATES. A *line* WAS FITTED TO THE DATA POINTS PREDICTED BY THE DELAY METRIC. IN THIS TABLE THE AVERAGE min, max ESTIMATION ERROR PERCENTAGE IS SHOWN.

Gate	$45nm$ (%)				$65nm$ (%)				$100nm$ (%)			
	SN	TN	CP	CPM	SN	TN	CP	CPM	SN	TN	CP	CPM
INV	$-161, 97$	$-41, 26$	$-139, 76$	$-14, 10$	$-94, 68$	$-37, 27$	$-78, 54$	$-9, 7$	$-24, 22$	$-7, 5$	$-19, 16$	$-7, 9$
NAND2	$-275, 137$	$-82, 45$	$-240, 112$	$-32, 14$	$-153, 91$	$-69, 43$	$-130, 76$	$-22, 11$	$-59, 43$	$-26, 19$	$-51, 35$	$-3, 4$
NOR2	$-209, 111$	$-59, 35$	$-181, 92$	$-19, 11$	$-112, 73$	$-50, 34$	$-96, 61$	$-13, 8$	$-31, 20$	$-9, 6$	$-23, 16$	$-7, 10$
XOR2	$-271, 141$	$-80, 47$	$-236, 115$	$-31, 15$	$-151, 94$	$-68, 45$	$-129, 79$	$-22, 13$	$-57, 43$	$-24, 19$	$-49, 35$	$-3, 4$

a changes as we take more samples of the parameters across a wider range. Thus a metric might be able to track the delay across small variations of supply voltage while it may not be able to track delay under large variations of supply voltage. This is illustrated in the Figures 4 and 5.

In Figure 4, the CMOS gates operate under *nominal* supply voltages, $V_{DD} = 4 \times V_{T0}$ to $6 \times V_{T0}$ all the delay metrics correlate to HSPICE reasonably well. However, when the supply voltage drops below $V_{DD} = 4 \times V_{T0}$, only the CPM metric is able to track the delay well shown in Figure 5. The data is taken for an inverter in $65nm$ technology by varying the supply voltage V_{DD} from $2 \times V_{T0}$ to $6 \times V_{T0}$ and fixing the other circuit parameters.

The data obtained from other gates across various technologies and circuit parameters such V_{DD} and V_T have similar results to Figure 5. There are two things to note in this figure:

1) The *correlation* measures the relative error. Intuitively, the relative error gives an estimate of how close the shape of the predicted delay curve is with the actual delay obtained from HSPICE simulations.
2) The *estimation error* gives the absolute difference between the predicted delay and the actual delay obtained from HSPICE simulations.

To visualize the performance of delay metrics with respect to the above two characteristics we use the scatter plot. The scatter plot of different delay metrics versus the actual delay values for INV in $65nm$ technology is shown in Figure 6.

The data points are obtained by varying different circuit parameters. We fitted a line through the data points to find out the constant of proportionality in the delay metrics. Then we find the estimation error between the fitted line and the HSPICE delay values. The correlation is shown as `corrcoef` and the estimation error is shown as 'Average error' in the scatter plot. From the scatter plot it is clear that the CPM delay metric has the highest correlation and the lowest estimation error among all the delay metrics.

Table I summarizes the *correlation* coefficient of different delay metrics for various gates across the technologies. The correlation was taken between the actual HSPICE delays and the delay metric. From the table, we observe that the correlation coefficient of the CPM metric is consistently greater than 0.98, which is not exhibited by the other delay metrics. The estimation errors are tabulated in Table II. The values listed in the table are the *average* of the estimation errors.

VI. Conclusion

In this paper, we proposed a new closed form delay metric based on the modified centroid of power dissipated. This new metric is inspired by our key observation that the SN delay can be viewed as the centroid of current. We also provide a theoretic proof that the SN delay is the Elmore delay of a CMOS gate when a gate is modeled as an RC circuit. The delay due to finite rise time can be incorporated using techniques such as PERI [14].

Our proposed metric has a very high correlation coefficient (≥ 0.98) when correlated with the actual delays got from the HSPICE simulations. Such high correlation is consistent across all major process technologies. The new metric is both simple and inexpensive to use as compared to the other metrics proposed in the literature. We anticipate its use in low voltage circuits and in the inner optimization of physical design tools where it is necessary to obtain quick and relatively accurate delay estimates.

Acknowledgment

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References

[1] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE Journal of Solid State Circuits*, vol. 25, no. 2, pp. 584–594, April 1990.

[2] C. J. Alpert, A. Devgan, and C. V. Kashyap, "RC delay metrics for performance optimization," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 20, no. 5, pp. 571–582, May 2001.

[3] J. Rubinstein, P. Penfield, and M. A. Horowitz, "Signal delay in RC tree networks," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 2, no. 3, pp. 202–211, July 1983.

[4] L. T. Pillage and R. A. Rohrer, "Asymptotic waveform evaluation for timing analysis," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 9, no. 4, pp. 352–366, April 1990.

[5] B. Tutuianu, F. Dartu, and L. Pileggi, "An explicit RC-circuit delay approximation based on the first three moments of the impulse response," in *Proc. of Design Automation Conf.*, 1996, pp. 611–616.

[6] A. B. Kahng and S. Muddu, "An analytical delay model for RLC interconnects," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 16, no. 12, pp. 1507–1514, December 1997.

[7] R. Kay and L. Pileggi, "PRIMO: Probability interpretation of moments for delay calculation," in *Proc. of Design Automation Conf.*, 1998, pp. 463–468.

[8] T. Lin, E. Acar, and L. Pileggi, "h-gamma: an RC delay metric based on a gamma distribution approximation of the homogeneous response," in *Proc. of the International Conf. on Computer-Aided Design*, 1998, pp. 19–25.

[9] F. Liu, C. Kashyap, and C. J. Alpert, "A delay metric for RC circuits based on the weibull distribution," in *Proc. of the International Conf. on Computer-Aided Design*, 2002, pp. 620–624.

[10] C. J. Alpert, F. Liu, C. Kashyap, and A. Devgan, "Delay and slew metrics using the lognormal distribution," in *Proc. of Design Automation Conf.*, 2003, pp. 382–385.

[11] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge University Press, 1998.

[12] W. Shockley, "A unipolar 'field-effect' transistor," in *Proc. of Institute of Radio Engineers*, 1952, pp. 1365–1376.

[13] T. Sakurai and A. R. Newton, "A simple MOSFET model for circuit analysis," *IEEE Trans. on Electron Devices*, vol. 38, no. 4, pp. 887–894, April 1991.

[14] C. V. Kashyap, C. J. Alpert, F. Y. Liu, and A. Devgan, "Closed-form expressions for extending step delay and slew metrics to ramp inputs for RC trees," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 23, no. 4, pp. 509–516, April 2004.

[15] D. Hodges, H. Jackson, and R. Saleh, *Analysis and Design of Digital Integrated Circuits: In Deep Submicron Technology*. McGraw-Hill, 2003.

[16] R. Gupta, B. Tutuianu, and L. Pileggi, "The elmore delay as a bound for RC trees with generalized input signals," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 16, no. 1, pp. 95–104, January 1997.

[17] W. Elmore, "The transient response of damped linear networks with particular regard to wideband amplifiers," *Journal of Applied Physics*, vol. 19, no. 1, pp. 55–63, January 1948.

[18] A. V. Oppenheim, A. S. Willsky, and S. H. Nawab, *Signals and Systems*. Prentice Hall, 1996.

[19] Y. Cao, T. Sato, M. Orshansky, D. Sylvester, and C. Hu, "New paradigm of predictive MOSFET and interconnect modeling for early circuit simulation," in *Proc. of Custom Integrated Circuits Conf.*, 2000, pp. 201–204.