Improved Weight Assignment for Logic Switching Activity During At-Speed Test Pattern Generation

M.-F. Wu, H.-C. Pan, T.-H. Wang, and J.-L. Huang
Graduate Institute of Electronics Engineering
Dept. of Electrical Engineering
National Taiwan University, Taipei 106, Taiwan

Kun-Han Tsai and Wu-Tung Cheng
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070, USA

ABSTRACT

For two-pattern at-speed scan testing, the excessive power supply noise at the launch cycle may cause the circuit under test to malfunction, leading to yield loss. This paper proposes a new weight assignment scheme for logic switching activity; it enhances the IR-drop assessment capability of the existing weighted switching activity (WSA) model. By including the power grid network structure information, the proposed weight assignment better reflects the regional IR-drop impact of each switching event. For ATPG, such comprehensive information is crucial in determining whether a switching event burdens the IR-drop effect. Simulation results show that, compared with previous weight assignment schemes, the estimated regional IR-drop profiles better correlate with those generated by commercial tools.

1. INTRODUCTION

It is known that the signal switching activity (SA) could be doubled or even more in the test mode than in the functional mode [21]. During manufacturing testing, this causes both thermal management and signal integrity (SI) problems. First, excessive SA leads to abnormal heat dissipation. If not properly transferred to the heat sink or the surroundings, the heat will accumulate and eventually cause permanent damage to the circuit under test (CUT) [6]. Secondly, high SA causes excessive power network IR-drop because more current is drawn from the power supply. The excessive IR-drop incurs extra gate delays, which may cause a good CUT to fail at-speed testing and result in test yield loss [15, 11]. This paper concerns the SI problem during manufacturing testing.

The IR-drop induced test yield loss in at-speed testing gets even worse for moderns ICs, which is due to the trend of decreasing power supply voltage (i.e., less immunity to IR-drop), growing chip complexity (i.e., more SA), and elevating clock rate (i.e., less timing margin). Thus, generating IR-drop-aware at-speed patterns has been an important ongoing topic.

A quick yet powerful IR-drop analyzer is indispensable to establish a robust test pattern generation flow, whether it guides ATPG to generate IR-drop-safe patterns or it helps screen out IR-drop violating test patterns. While commercial tools are available for accurate dynamic IR-drop evaluation, they are unsuitable for ATPG applications due to the time complixity.

1.1 At-Speed Scan Testing

At-speed scan testing has become mandatory in recent years [9]. Among various approaches to at-speed testing, the launch-on-capture (LOC) and launch-on-shift (LOS) schemes

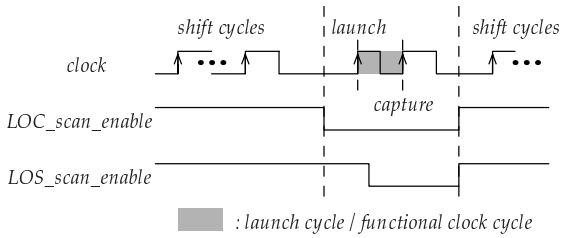

Figure 1: The LOC and LOS timing diagram.

are the most popular because they use the existing scan-design hardware. Figure 1 illustrates the timing diagram of these two schemes. In LOC, the activation pattern is launched by capture; in LOS, the activation pattern is launched by last shift. Once the activation pattern is launched, the test response is captured after the *functional* clock period to see whether the transitions reach the primary output and flip-flops in time. This functional cycle is called launch cycle in the following discussion.

Since at-speed scan testing is being challenged by the yield loss problem [15, 11], many techniques have been proposed to reduce the launch cycle SA by, for example, power-aware ATPG [12, 1, 2, 5], X-filling [17, 13, 3, 19], or design-for-test (DfT) [14, 16]. Weighted switching activity (WSA), the summation of the switching cells' weights, e.g., fanout count plus one [8], is commonly used to assess the SA-induced IR-drop severity in ATPG for its efficiency.

In the basic WSA model, timing and spatial information of the switching cells is not considered. It comes at no surprise that our experimental results show the correlation coefficient between launch cycle WSA and peak IR-drop is in general less than 0.5. Besides, it cannot reveal the regional IR-drop information.

To improve the correlation and capability, recent works start taking timing and layout information into account.

1.2 Power Supply Noise/IR-Drop Estimation

There have been several power supply noise/IR-drop evaluation methods to guide the ATPG process or to quantify the generated test patterns. These methods are explicitly or implicitly WSA-based; they differ in the weight assignment scheme, the timing model, and how they assess the regional IR-drop.

1.2.1 Weight Assignment

In all WSA-based approaches, the weight assigned to a standar cell is intended to reflect the actual load associated with that cell. A popular scheme is to use the fanout count plus one [8] as the standard cell's weight. Unit weight assignment [4], i.e., the toggle count, and load capacitance [2]

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are also often employed. To speed up computation, some approaches assign zero weight to all but the flip-flop. Our experiemental results show that these weight assignment schemes make little difference in IR-drop estimation accuracy and capability.

1.2.2 Temporal Distribution

The impact of SA's temporal distribution on peak IR-drop is apparent. For example, with the same SA count, the case where all SA occurs at a very narrow time window will almost always lead to more severe IR-drop than the case where all SA is evenly spread in a clock cycle.

The techniques in [1, 2] incorporate the longest delay information. First, the authors defined the switching time window (STW) of a test vector v as the time frame during which the transitions caused by v occur. $STW\,(v)$ is a function of the maximum path delay of v and the clock-to-register delay. Using $STW\,(v)$ (instead of the clock period), one obtains more accurate *average power* estimation. However, the improvement diminishes as the maximum delay approaches the clock period.

The techniques in [18, 4] utilize timed logic simulation to obtain the temporal distribution of switching events. A launch cycle is divided into several equal-length time slices; then, the instantaneous WSA of each time slice is computed. The maximum instantaneous WSA among all time slices is used to assess the peak IR-drop in this launch cycle. Our experimental results show that this time-slice-division technique substantially improves the peak IR-drop estimation quality. WSA-based model that utilizes this time-slice-division technique is denoted by WSA^{T+} in the rest of the paper.

1.2.3 Regional IR-Drop Assessment

Recently, the impact of regional IR-drop has drawn growing attention. In the basic WSA and WSA^{T+}, the global switching activity as a whole is concerned, which is problematic. For example, the same WSA (or WSA^{T+}) can cause yield loss or be harmless depending on how it affects the critical path delay. The regional IR-drop information thus helps devise a thorough IR-drop constraint plan.

Techniques in [18, 5, 7] proposed to divide cells in a chip into groups according to the layout. Then, the regional WSA in each group, i.e., WSA (or WSA^{T+}) of switching cells in the group, represents regional IR-drop severity in the corresponding area.

The advantage of using this group-based technique for regional IR-drop assessment is that it is very simple. It can be easily integrated into basic WSA or WSA^{T+} without additional computation overhead. However, quality of the regional IR-drop information obtained this way is in doubt. First, it ignores the fact that a switching cell causes IR-drop not only in the region it belongs but also other regions through which it draws current from the power supply pad. Furthermore, determining the group size and the partitioning scheme is either non-trivial or the chosen partitioning may not provide adequate spatial resolution to reveal the real regional IR-drop problem.

This work addresses the above concerns; its goal is to improve the weight assignment scheme to provide high-quality regional IR-drop information, i.e., whole-chip IR-drop profile, without incurring too much computation overhead.

1.3 Contributions

This paper proposes an improved weight assignment scheme for logic switching events. The goal is to facilitate IR-drop aware at-speed test pattern generation (but not to replace the accurate IR-drop estimation tools); thus, we are more concerned about its time complexity and its capability in pinpointing the problematic patterns rather than the actual IR-drop values.

First, a new weight assignment scheme is proposed. For each cell, its weight is a vector that stores its IR-drop impact on selected power grid nodes. The cell weights are characterized in the pre-process phase. In the rest of the paper, we use WSA^{W+} to denote the weighted switching activity obtained using the proposed weight assignment. Second, the power-grid network is reduced to lower the computation efforts in both pre-processing and regional IR-drop estimation. Finally, superposition is applied to obtain the whole-chip IR-drop profile with respect to a given set of switching cells.

We further combine WSA^{W+} with WSA^{T+} to obtain WSA^{WT+} which takes both switching cell's timing information and impact on whole chip into accout. This produces whole-chip IR-drop profiles for all time slices.

The contributions of the proposed WSA^{WT+} are summarized as follows:

1. Compared with previous approaches, each cell's weight now considers more realistic power grid structure than just physical location; this better reflects the actual regional IR-drop mechanism.

2. A two-phase approach is developed to speed up IR-drop calculation. The time-consuming matrix inversion operations are only needed in the characterization phase and once for each circuit. In the IR-drop profiling phase, the computation overhead is very small.

3. The quality of group-based WSA^{T+} and WSA^{WT+} techniques are evaluated via commercial post-layout IR-drop simulation tools. The results show that, for global peak IR-drop analysis in launch cycle, WSA^{T+} and WSA^{WT+} perform well with sufficient timing resolution. However, only WSA^{WT+} can provide high-quality whole-chip IR-drop profiles and truely reveal regional IR-drop.

1.4 Paper Organization

The paper organization is as follows. Section 2 describes the proposed quick whole-chip IR-drop estimation method. Then, Section 3 shows the launch cycle IR-drop analysis flow. Simulation results are given in Section 4. Finally, Section 5 concludes this work.

2. THE QUICK WHOLE-CHIP IR-DROP ESTIMATION TECHNIQUE

The idea of the proposed technique is to trade off between the accuracy of circuit simulation and the efficiency of WSA.

This section describes, given the power grid information and the set of switching cells, how the proposed technique computes the weight of each cell and how it enhances the WSA model to assess the resulting IR-drop profile over the whole die area.

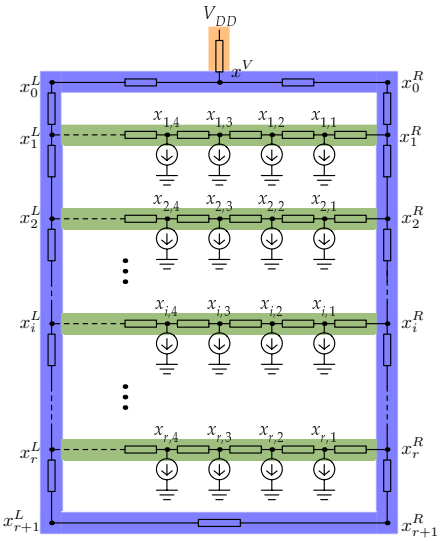


Figure 2: The power grid model.

2.1 The Power Grid Model

Figure 2 depicts a common circuit model of the power grid and the cells in standard cell designs. To speed up the IR-drop estimation process, we choose to model only the power grid resistance and ignore the capacitance; this tends to overestimate the IR-drop. The power grid structure and resistance values are extracted from the post-layout file.

Each cell is simplified as a current source; it draws a specified amount of current during the time slice it switches. The time it switches can be extracted from the value changed dump (VCD) file after timed logic simulation. Its location in the power grid network is also extracted from the layout information.

2.2 MNA-Based IR-Drop Computation

Given the power grid model in Figure 2 and a set of switching cells, the problem now is to compute a resistance-only circuit's node voltages.

One intuitive approach is to use modified nodal analysis (MNA). Assume that the power grid has n nodes. The linear system to calculate IR-drop is

$$A \cdot x = y \tag{1}$$

where A is an n-by-n matrix that describes the power grid structure, x is the vector of the n nodal voltages, and y is the vector that describes the independent sources.

However, solving (1) is still time consuming. The complexity is $O\left(n^3\right)$ if Gaussian elimination is used. (Faster algorithms exist, but not better than $O\left(n^2\right)$.) The incurred computation time is certainly unacceptable for ATPG purpose, not to mention that this has to be repeated for every test pattern and every time slice.

2.3 Proposed IR-Drop Estimation Flow

Figure 3 depicts the proposed flow. In the "Pre-Process" phase, the cell weight vectors are computed. In our technique, the weight vector associated with a cell $c_{i,j}$ relates to the IR-drop it induces on the *power branch points* (PBP's) assuming that it draws unit current during switching. Power

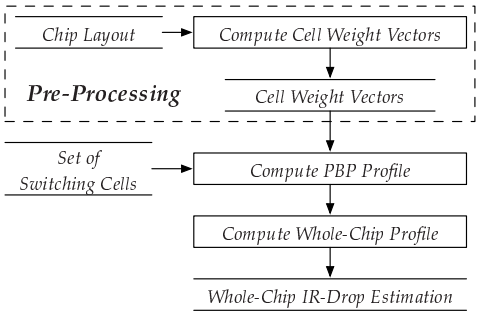


Figure 3: The IR-drop computation flow.

branch points are the nodes left in the power grid after we (1) remove all the current sources, and (2) merge serially connected resistors. For example, in Figure 2, x_1^L, $\cdots$, x_r^l, x_1^R, $\cdots$, x_r^R, and x^V are PBP's. Note that (1) the weight vector plays the same role as the weight in previous weight assignment schemes, and (2) the weight vector only concerns PBP's.

Because the power grid network considered here is a linear circuit of resistors, we can compute the aggregate effect of the switching cells on the power grid by superposition, i.e., the weighted sum of their weight vectors.

Once the estimated IR-drop profile on the PBP's is available, the IR-drop at the remaining V_{DD} terminals of standard cells can be computed. The result is the estimated power grid IR-drop profile of the whole chip. Note again that the computed IR-drop values are not real numerical values but relative ones because the current is normalized and the capacitance is ignored.

In the following, details of each step will be given.

2.4 Weight Vector Computation

For each cell $c_{i,j}$, the associated weight vector $\mathcal{M}_{i,j}$ records the estimated IR-drop on the PBP's assuming that $I_{i,j} = 1$; this saves both computation time and memory storage.

Because only the PBP's are concerned at this stage, the proposed technique simplifies the power grid network by merging serially connected resistors. The simplified network of Figure 2 is shown in Figure 4 assuming that $c_{i,j}$ is the characterized cell. After simplification, except for the one that contains $x_{i,j}$, any path that connects exactly two PBP's contains one resistor.

MNA is then performed on the simplified network; now the complexity of solving the linear system of MNA is reduced from $O(n^3)$ to $O((m+1)^3)$, where m is the number of PBP nodes in the simplified network. After solving the linear system, the estimated IR-drop at every PBP is known. For the example in Figure 4, $\mathcal{M}_{i,j}$ is shown in (2), where $v_i^L(v_i^R)$ corresponds to the incurred IR-drop on node $x_i^L(x_i^R)$.

$$\mathcal{M}_{i,j} = \left[v_1^L \ \cdots \ v_r^L \ , v_1^R \ \cdots \ v_r^R \ , v^V\right] \tag{2}$$

2.5 Compute PBP IR-Drop Profile

Let $I_{i,j}$ be the actual current drawn by $c_{i,j}$ when it switches and $t_{i,j}$ equal 1 if $c_{i,j}$ switches and 0 otherwise. The PBP IR-drop profile is obtained via superposition.

$$\mathcal{M} = \sum_i \sum_j t_{i,j} \cdot I_{i,j} \cdot \mathcal{M}_{i,j} \tag{3}$$

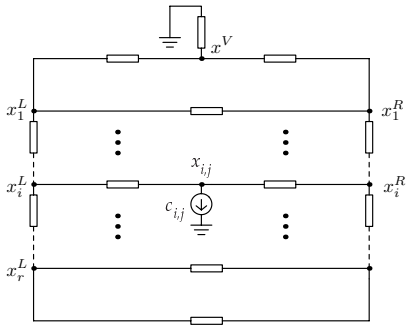


Figure 4: The simplified power grid for IR-drop weight vector computation.

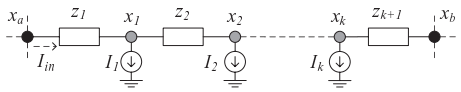


Figure 5: Computing node voltage between two PBP's.

In current implementation, we use $I_{i,j} = 1$ for all cells; thus, the proposed technique does not return the actual IR-drop voltages but the relative severity estimation.

2.6 Compute Whole-Chip IR-Drop Profile

Once the PBP IR-drop profile is available, the whole-chip profile can be compuated. Figure 5 illustrates how to compute the node voltage between any two PBP's. First, the flow-in currents, I_{in}, are computed.

$$I_{in} = (v_a - v_b + \sum_{q=1}^{k} \left(z_{q+1} \sum_{p=1}^{q} I_p \right)) / \sum_{p=1}^{k} z_p \qquad (4)$$

Then, the voltage of node x_i (denoted by v_i) is as follows.

$$v_i = v_a - I_{in} \sum_{p=1}^{i} z_i + \sum_{p=1}^{i-1} \left(I_p \sum_{q=p+1}^{i} z_q \right) \qquad (5)$$

2.7 Discussions

2.7.1 Applicability to Complex Power Network

In reality, the design may utilize more complicated power grid configuration to enhance the power grid robustness, for example, by adding more vertical, more horizonal stripes, and more V_{DD} pads as in Figure 6. The idea of PBP is still feasible and the same superposition and voltage computation techniques can be applied. For designs with million PBP's, faster solver [10, 20] can replace MNA to speed up the pre-process time for the weight vectors.

Although we only describe IR-drop estimation on power network, the same method can be utilized for ground network.

2.7.2 Performance Analysis

For designs with n cells and m PBP, the speedup factor compared to the intuitive MNA-based approach for computing the IR-drop profiles of p time slices can be roughly

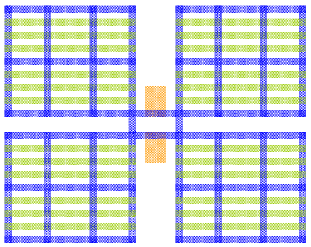


Figure 6: Another power grid configuration.

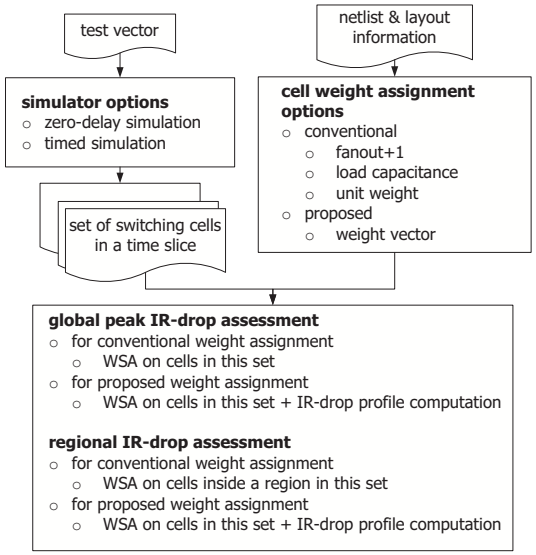


Figure 7: The launch cycle IR-drop estimation flow.

estimated by

$$\frac{\alpha \cdot p \cdot n^3}{\beta \cdot n \cdot (m+1)^3 + \gamma \cdot p \cdot n \cdot m} \qquad (6)$$

where α, β, and γ are constants; the first and second terms of the denominator correspond to the efforts of weight vector and IR-drop profile computation, respectively.

Take s38584 for example. It has $n \approx 20,000$, $m \approx 180$, and $p \approx 500 \times 20 = 10,000$ (500 patterns each of which has 20 time slices); the resulting speedup factor is about 10^5 assuming $\alpha = \beta = \gamma = 1$.

Compared to WSA^{T+}, the computation overhead of WSA^{WT+} includes (1) the weight vector computation, and (2) for each time slice, superposition and whole-chip profile computation.

3. LAUNCH CYCLE IR-DROP ESTIMATION FLOW

Figure 7 depicts the launch cycle global and regional IR-drop estimation flow. For a test vector, logic simulation is performed to obtain the switching events in the launch cycle. If timed logic simulator is used, each switching event further stores when it occurs. Then, according to user specified time slice size, the set of switching cells in each time slice is identified. When the time slice size equals the launch cycle period, only one set is produced. Netlist and layout information, on the other hand, are utilized to assign weight to each standard cell according to the selected option.

Table 1: WSA vs. Global Peak IR-Drop Correlation

	1	2	3	4	5
	basic	WSA^{T+}			WSA^{WT+}
W	fanout+1		load	unit	weight vector
T	20 ns	0.5 ns			
s5378	0.550	0.845	0.661	0.845	0.845
s13207	0.299	0.869	0.854	0.869	0.881
s15850	0.277	0.895	0.713	0.914	0.929
s35932	0.746	0.850	0.824	0.867	0.889
s38417	0.364	0.866	0.823	0.873	0.918
s38584	0.978	0.947	0.911	0.892	0.914
average	0.536	0.879	0.798	0.876	0.896

For each set of switching cells in a time slice, global peak IR-drop and regional IR-drop are measured; the estimation mechanism depends on which weight assignment option is used.

If ther are more than one time slice, the maximum global peak IR-drop estimation value among all time slices represents the launch cycle global peak IR-drop severity for this test vector.

4. SIMULATION RESULTS

For the purpose of validating our technique, a commercial post-layout IR-drop analysis tool is used to generate the reference IR-drop profiles. It uses the same VCD file in the IR-drop estimation flow; standard cell library and all required technology files are further included. When users input a specific time period, the commercial tool can report whole chip peak IR-drop result during that specific time period.

The experimental setup is as follows.

- The used power grid structure is similar to Figure 2.
  - Row-based standard cell design.
  - Single V_{DD}/V_{SS} pad is used.
  - No additional power stripes.
  - Each standard cell is fed by a single power rail.
- TSMC .13 μm cell library.
- V_{DD} = 1.08 V.
- At-speed fault model; launch cycle = 20 ns.

4.1 Global Peak IR-Drop Evaluation

A series of experiments are conducted to evaluate various IR-drop evaluation methods, including the proposed one.

The first experiment compares five different WSA-based approaches. Their setup on the weight assignment schemes (W) and time slice size (T) are listed in the 3rd row and the 4th row in Table 1. The 1st approach is basic WSA. The 2nd, 3rd and 4th approaches are WSA^{T+} with different conventional weight assignment schemes. The 5th approach is WSA^{WT+}. The correlation coefficients between the estimated global peak IR-drop and the referenced global peak IR-drop for at-speed test patterns for benchmark circuits are shown.

After incorporating the timing information, all correlate much better with the peak IR-drop than the basic WSA approach. The proposed method performs the best in average although the difference is not significant.

4.2 Regional IR-Drop Evaluation

Table 2: Chip Partitioning Information

circuit	rail	std. cell	group/rail	cell/group
s5378	23	3316	6	24
s13207	41	9863	11	22
s15850	44	9522	11	20
s35932	67	21247	15	21
s38417	57	27087	23	21
s38584	89	19770	12	19

However, the main strength of the proposed technique is the capability of generating high quality whole-chip IR-drop profile; this is validated in the following experiments.

For WSA^{T+} approaches (the 2nd, 3rd, and 4th ones), to compute regional IR-drop, regional WSA is computed. According to layout, we divide each power rail into equal length groups (regions). Columns 2 to 4 in Table 2 show the numbers of rails, standard cells, and groups per rail. The last column lists the average number of cells per group. The partitioning criterion is to keep the number of cells per group to be about 20 as in [5].

Figure 8(a) shows the whole-chip IR-drop snapshot obtained by the commercial tool. The chosen time slice is the one that exhibits the largest IR-drop during the 20 ns capture cycle of s38534's first test pattern. This snapshot is the bird's eye view of the chip. The only V_{DD} pad is located on the middle of the bottom boundary of the snapshot. The brighter the color, the more the IR-drop

Figure 8(b) shows the profile reported by the fanout+1 WSA^{T+} approach; it can be seen that the result is a low resolution profile and cannot reflect a good regional IR-drop result. The main reason is, although it shows more switching events are at left and the right bottom of the snapshot, it lacks the information of how far a switching event to the V_{DD} source is and the realistic power grid structure. (Because the results of the 2nd to 4th approach are very similar, we just take the 2nd approach as representative for WSA^{T+} with group-based technique.)

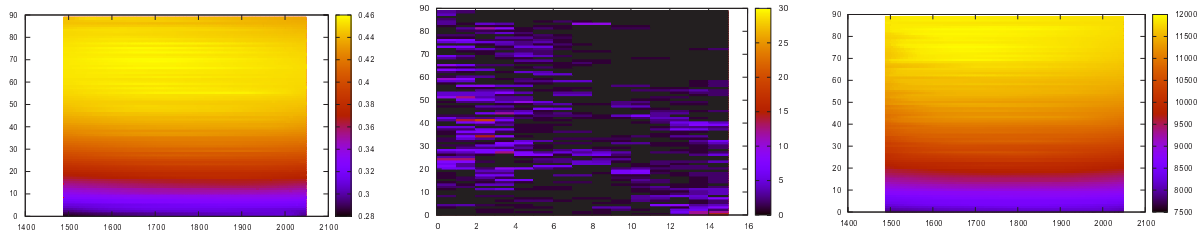
Figure 8(c) shows the profile reported by the proposed WSA^{WT+} approach. The results show that WSA^{WT+} captures the IR-drop profile much better than group-based WSA^{T+} techniques. The reason is that the weight of each cell considers all PBP's in the realistic power network. In this way, the impacts of the switching cells is on the whole chip rather than limited in a pre-defined area.

Note that WSA^{WT+} does not return the actual IR-drop voltage, either.

4.3 Snapshots Correlation Summary

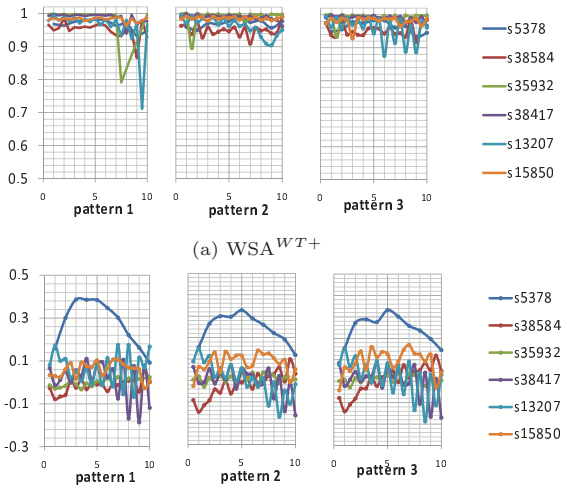
Figure 9(a) summarizes the correlation between the snapshots obtained by the commercial tool and by the proposed WSA^{WT+} technique. The correlation considers every power grid node that connects to the standard cell VDD terminal. For each circuit, results for the first three test patterns are shown. Each plot in Figure 9(a) corresponds to one pattern. The x-axis represents the time (from 0 to 10 ns); the y-axis represents the correlation coefficients between the two snapshots. The plots show very high correlation from 0 to 6 ns. However, after that, the correlation becomes unstable for some patterns; the reason is the lower IR-drop values.

The results for using fanout plus one as weights are shown in Figure 9(b). The plots show that there is almost no correlation.



(a) s38584, commercial tool (b) s38584, WSA^{T+} (c) s38584, WSA^{WT+}

Figure 8: Instantaneous IR-drop profiles.



(a) WSA^{WT+}

(b) WSA^{T+}

Figure 9: Whole-chip IR-drop snapshot correlation results (vs. reference).

4.4 CPU Time

For the pre-process time, it takes 87.6 seconds for the longest one (s38417). Note that this is performed just once for each circuit and it is not needed during ATPG phase.

For the IR-drop profiling time druing ATPG phase, the proposed (5th) approach takes about 0.1 seconds for the longest one (s38584); the other WSA-based approaches, on the other hand, takes about 0.05 seconds in average. Commercial tools, which can compute actual IR-drop values, take about 1 minute from the start to the end.

5. CONCLUSION

A quick and high spatial resolution IR-drop analysis technique is presented. A new cell weight assignment scheme is proposed. The new scheme considers the actual power grid structure; thus, it is able to enhance the conventional WSA model's capability of producing high-quality whole-chip IR-drop profile. With the high quality IR-drop profile, ATPG can screen out test patterns that suffer high IR-drop with much more regional information and knows better whether a switching event really burdens the current IR-drop profile through its weight vector. In the future, we will seek to integrate it into ATPG process and perform experiments on realistic designs.

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