Parallel Statistical Capacitance Extraction of On-Chip Interconnects with an Improved Geometric Variation Model

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Abstract – In this paper, a new geometric variation model, referred to as the improved continuous surface variation (ICSV) model, is proposed to accurately imitate the random variation of on-chip interconnects. In addition, a new statistical capacitance solver is implemented to incorporate the ICSV model, the HPC [5] and weighted PFA [6] techniques. The solver also employs a parallel computing technique to greatly improve its efficiency. Experiments show that on a typical 65nm-technology structure, ICSV model has significant advantage over other existing models, and the new solver is at least 10X faster than the MC simulation with 10000 samples. The parallel solver achieves 7X further speedup on an 8-core machine. We conclude this paper with several criteria to discuss the trade-off between different geometric models and statistical methods for different scenarios.

I. Introduction

As technology scales down to the nanometer era, interconnect parasitic extraction is now facing the new challenges of process variations. For capacitance extraction, the geometric variation of interconnect structure is of main concern, because it affects the shape and dimensions of interconnects, and thus the capacitance results. Due to different inherent mechanisms, the geometric variations can be classified into systematic variation and random variation [1], which are modeled with different methods respectively. For the random variation and complicated systematic variation, the stochastic modeling methodology is needed to generate the statistical distribution of capacitance, which can then be employed by the statistical circuit analysis. Therefore, the statistical capacitance extraction considering random variations has become important.

A large number of numerical methods have been proposed to derive the statistical behavior of the capacitance, for which the mean value and standard deviation (Std) are the two main metrics. Of all these methods, the most straight-forward approach is the Monte Carlo (MC) method, which generates thousands of stochastic sample structures. Each sample structure can be solved with deterministic capacitance extraction algorithms. The MC method has the drawback of huge computational cost, but produces the golden value for comparison of other methods. Several fast non-MC methods have been proposed to generate the variational capacitance model for on-chip interconnects. Based on a 3-D boundary element method (BEM) capacitance solver, a conversion method was proposed in [2] to generate a quadratic model for the capacitance variation. Since this method is based on the Taylor's expansion, it is only suitable for variation with small magnitude. An efficient method, called spectral stochastic collocation method (SSCM), was proposed in [3] with the same on-chip interconnect variation model. In [4], a spectral stochastic method using the Hermite polynomial chaos was proposed to generate the quadratic capacitance model. A method based on Hermite polynomial collocation (HPC) technique that considers the window-based chip-level capacitance extraction was proposed in [5]. The method efficiently calculates statistical full-path capacitance by fast computation of the capacitance covariances between windows. In [6], the method in [5] was extended to consider a continuous-surface model, and a weighted principle factor analysis (wPFA) technique was proposed to further reduce the random variables.

However, it must be noted that before applying any numerical solver for statistical capacitance extraction, the geometric variation model should be firstly established, where some geometric parameters are set to be random variables following certain kind of spatially correlated distribution. The geometric variation model must be carefully constructed to reflect the actual variation of the interconnect structures; otherwise any solver will not generate a realistic solution. In [2-4], the geometric variation was modeled as the fluctuation of conductor surface panels. This model, referred to as the discontinuous surfaces variation (DSV) model, obviously deviates from the actual situation. Moreover, it is shown in [6] that this DSV model will cause prominent Std error of total capacitance. A variation model with continuous surface was proposed in [6] to substitute the DSV model. However, this continuous surface variation (CSV) model is still not practical for depicting interconnects with large variation of wire width or thickness. And, the experiment setting in [6] did not reflect the reality of the sub-65nm technology. As a result, the error of the DSV model shown in experiments was not larger than 7%, and the Std was as small as 1% of the capacitance mean value in [6]. Besides, another geometric model, where each nominal conductor surface is assumed to vary as a whole, was used in [7, 8] for calculation of sensitivity, or in [9] for 2-D structures. We refer to this model as variation as a whole (VAW) model in this paper.

In this paper, an improved continuous surface variation (ICSV) model is proposed to overcome the drawback of the model in [6] through the setting of random variables. Considering the 65nm technology and the major variation quantities affecting capacitance, a typical interconnect structure is employed to generate test cases with different wire spacing and surface roughness. Through the comparison experiments with other existing models, the advantages of ICSV model are demonstrated. Based it, an efficient parallel statistical capacitance solver is developed, employing the

This work is supported by NSFC under Grant 61076034, and in part by the TNList Cross-Discipline Foundation, and the Opening Foundation of Key Laboratory of Computer System and Architecture, Institute of Computing Technology, Chinese Academy of Sciences.

978-1-4244-7516-2/11/$26.00 ©2011 IEEE

techniques of HPC for statistical model construction and the wPFA for variable reduction. Numerical experiments on an 8-core machine show 7X speedup of parallelization, and that the HPC based method is at least 10X faster than the MC method. Besides, we have also drawn six criteria regarding the statistical capacitance extraction for different scenarios.

II. The Improved Continuous-Surface Variation Model

In this section, we firstly give an overview of the existing geometric variation models. Then, we discuss the drawback of model in [6] and propose the improved model.

A. Existing geometric variation models

Random variations are usually modeled with a set of random variables $\boldsymbol{\xi}$. The geometric variation behavior of on-chip interconnects is often assumed to follow the spatially correlated multivariate Gaussian distribution:

$$\rho(\xi_i) = \frac{1}{\sqrt{2\pi}\sigma} \exp(-\frac{\xi_i^2}{2\sigma^2}) \quad , \tag{1}$$

$$\mathrm{cov}(\xi_i, \xi_j) = \sigma^2 \exp(\frac{-|\vec{r}_i - \vec{r}_j|^2}{\eta^2}) \quad , \tag{2}$$

where $\rho(\xi_i)$ is the probability density function (PDF) of the i'th variable ξ_i, and σ is the standard derivation (Std). The spatial correlation between two variables are reflected by the correlation function in (2), where η is called correlation length. $\vec{r}_i$ and $\vec{r}_j$ are the spatial locations associated with ξ_i and ξ_j, respectively. There are other forms of correlation function, which may be extracted through sophisticated techniques using statistical data from actual chips [1]. The larger the correlation length, the stronger the correlation between variables spatially distributed.

For variation-aware capacitance extraction, an interconnect structure can be modeled with the following three geometric models.

- Discontinuous surface variation (DSV) model: It is assumed that each panel on nominal conductor surface fluctuates along the normal direction of surface, while keeping its shape unchanged (see Fig. 1). Thus, discontinuous surfaces are generated. The DSV model was employed for statistical capacitance extraction in [2-4].
- Continuous surface variation (CSV) model: This model characterizes the fluctuations of vertices of nominal surface panels. The variational vertices are then connected with triangular panels to form continuous surfaces. The CSV model was used for 2-D plane structure in [9, 12] and 3-D interconnects in [6]. In Fig. 2, we show the variational planes generated with the DSV and CSV models, for the purpose of comparison.

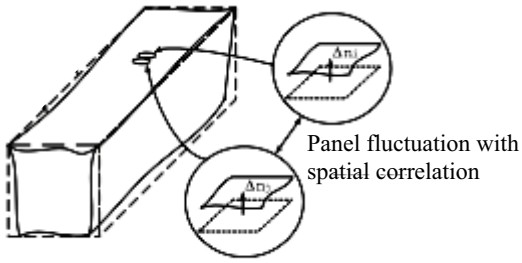
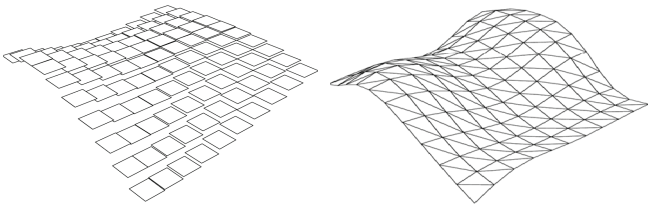


Fig. 1 The DSV model for statistical capacitance extraction [2].



(a) (b)

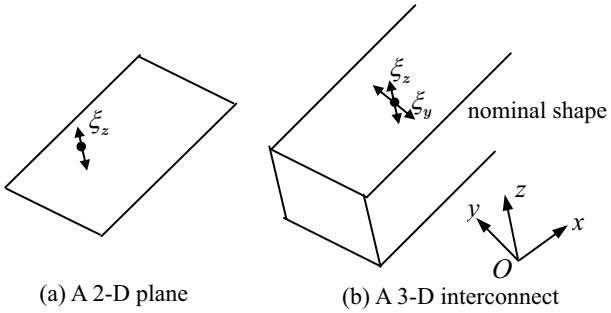
Fig. 2 A variational plane generated with: (a) the DSV model, and (b) the CSV model.

- Variation as a whole (VAW) model: It is assumed that the surface of nominal conductor fluctuates as a whole, such that the variational geometry keeps the same shape as the nominal geometry. The width and thickness of interconnect wire are often set to be random variables. This model was employed for sensitivity calculation [7, 8], and for statistical extraction of 2-D cross-section structure in [9].

Among the three models, the VAW model is the simplest one, which does not consider the detailed fluctuation of surface panels. The DSV model considers the detailed geometric variations, but generates an incomplete surface, that obviously deviates from the actual situation. For a 2-D plane, it is straightforward to improve it with a CSV model (see Fig. 2). However, for actual cases with two-direction variations of height and width, building the CSV model is not trivial. In [6], a CSV model was proposed, where two random variables are defined for each discretization vertex on nominal surface (as shown in Fig. 3). This model generates continuous surface while not increasing the number of variables. Experimental results in [6] reveal that the DSV model causes the underestimation of total capacitance variance. Therefore, it is necessary to adopt the CSV model for better accuracy.

To build the variation model for statistical capacitance extraction, we also need to divide the random variables into groups according to the assumption of variation source and their correlation. In each group, variables are correlated with the relationship defined by (2), while different variable groups are independent from each other. For the on-chip variation, the surfaces of interconnect wire are fabricated in different manufacture steps, that should be considered while setting the variable groups.

Besides, the width and thickness of interconnect wire, and the dielectric thickness are three major variable quantities [10-11]. In existing DSV and CSV models, the relationship between these quantities and surface random variables is not well taken care of. As we will show in the next subsection, the CSV model in [6] can cause very large surface fluctuation when describing a moderate width variation. Also, the variation of dielectric thickness is seldom considered in



(a) A 2-D plane (b) A 3-D interconnect

Fig. 3 The variable setting of the CSV model in [6].

existing works.

B. The drawback of the CSV model

The CSV model in [6] sets two random variables for each vertex. The variables along the tangential direction of surface include some redundant information. Moreover, to make natural transition of surfaces along an arris, the variables on the opposite surfaces of the same wire are set to correlated and have the same positive direction. This setting is illustrated by Fig. 4(a).

For illustration, we consider the distance between two surface vertices at the same horizontal level, i.e. points A and B in Fig. 4(a). Suppose the corresponding variables $\xi_{y,A}$ and $\xi_{y,B}$ follow the Gaussian distribution with Std of σ_y, and the correlation length for the y-direction variables is η_y. So, the wire width at this position is:

$$\xi_W = \xi_{y,B} + wid - \xi_{y,A} \quad , \tag{3}$$

where *wid* is the nominal wire width. Eq. (3) suggests that ξ_W also follows the Gaussian distribution, whose Std is:

$$\begin{aligned} \mathrm{std}(\xi_W) &= \sqrt{E(\xi_W^2) - E^2(\xi_W)} \\ &= \sqrt{E(\xi_{y,B}^2) + E(\xi_{y,A}^2) - 2\,\mathrm{cov}(\xi_{y,B}, \xi_{y,A})} \end{aligned} \quad . \tag{4}$$

With the property of Gaussian random variable and (2), we have

$$\mathrm{std}(\xi_W) = \sqrt{2\sigma_y^2 - 2\sigma_y^2 \exp(\frac{-wid^2}{\eta_y^2})} \approx \sigma_y \cdot \frac{\sqrt{2} \cdot wid}{\eta_y} \quad . \tag{5}$$

The last approximation is due to the fact that $wid^2 / \eta_y^2 << 1$ since the correlation length is usually much larger than wire width. Suppose η_y/wid=8, with (5) we can derive that $\sigma_y \approx 5.66 \cdot \mathrm{std}(\xi_W)$. This means, in order to make the Std of width being 10% of its nominal value, σ_y should be as large as 56.6% of the width. The large variance of surface fluctuation is obviously unrealistic. The analysis with this example shows that the model in [6] can hardly depict large variation of wire width or thickness.

C. The improved CSV model

To overcome the drawback of the existing CSV model, we firstly change the variation direction to the outer normal direction of nominal surface, as shown in Fig. 4(b). With this modification, the width of wire in the example becomes:

$$\xi_W = \xi_{y,B} + wid + \xi_{y,A} \quad , \tag{6}$$

whose Std is:

$$\mathrm{std}(\xi_W) = \sqrt{E(\xi_{y,B}^2) + E(\xi_{y,A}^2) + 2\,\mathrm{cov}(\xi_{y,B}, \xi_{y,A})} \quad . \tag{7}$$

Eq. (7) suggests that the Std of width approximates to 2X of σ_y. This is reasonable and enables generation of realistic interconnects with large width variance.

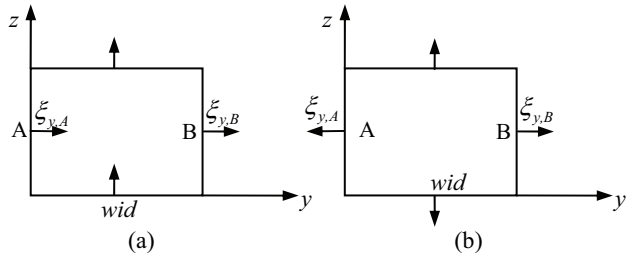


Fig. 4 The cross section of an interconnect wire, and the positive variation directions affecting the calculation of wire width and thickness. (a) the model in [6], (b) the proposed model.

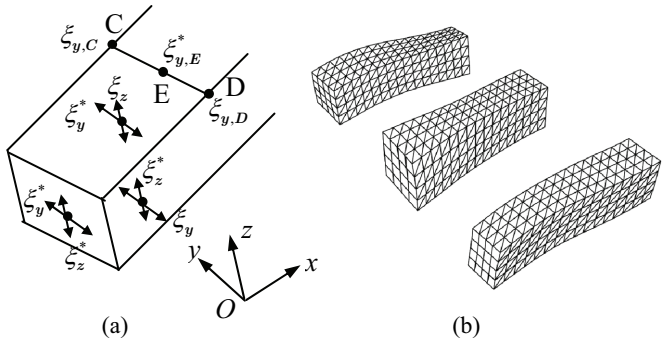


Fig. 5 The variable setting of the ICSV model (a), and the variational geometry of 3-D interconnects generated with it (b).

Under the assumption of variation directions, the two sides of top surface tend to move towards opposite directions. Therefore, how to make the natural surface transition at the arris becomes a problem. In this paper, we propose a new scheme for the variable setting, illustrated by Fig. 5(a). In this scheme, only one random variable is set for each vertex, representing the normal-direction variation. Then, to avoid the distortion and singularity of surface near the arris, a tangential displacement is generated for each nominal vertex, which is regarded as a derived variable (denoted by ξ^* in Fig. 5(a)). The value of derived variable is interpolated with two random variables. For example, at point E in Fig. 5(a),

$$\xi^*_{y,E} = \xi_{y,D} + (\xi_{y,C} - \xi_{y,D}) \frac{|\vec{r}_E - \vec{r}_D|}{|\vec{r}_C - \vec{r}_D|} \quad . \tag{8}$$

So, the value of derived variable reflects the propagation of the variations of points C and D. This scheme preserves the relative spatial relationship of two vertices after geometry variation, and thus generates a normal shape with continuous surfaces.

The variational surfaces of an interconnect wire can be classified as top, bottom, left-side, and right-side surfaces. So, we assume that the random variables form four groups, each of which obeys a Gaussian distribution with spatial correlation. With this assumption, (7) becomes:

$$\mathrm{std}(\xi_W) = \sqrt{2}\sigma_y \, . \tag{9}$$

Now, we can set a reasonable σ_y or σ_z to model the variations of wire width or thickness. Fig. 5(b) shows an example structure generated with the proposed model, which includes three parallel wires with surface variations. Besides, to consider the variation of dielectric thickness, we can simply include additional variables, one for an interlayer dielectric (ILD) thickness.

III. Experiments for Comparing the Three Geometric Variation Models

A. Experimental settings

Fig. 6 shows a typical on-chip interconnect structure for building the capacitance library. Investigating the statistical capacitance of this structure is very important for on-chip interconnect modeling. We consider the 65nm technology, and set the nominal values of the wire width (w), wire thickness (t) and dielectric thickness (h_1, h_2) for this structure: w=0.1μm, t=h_1=h_2=0.2μm. These values are obtained from [13], and are similar with those in International Roadmap for Semiconductors prediction [14]. We assume the length of the

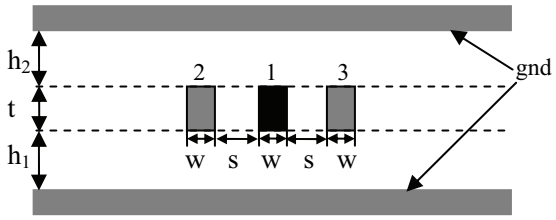


Fig. 6 The cross-section view of an interconnect structure with three parallel wires sandwiched by two ground planes

parallel wires to be L=1μm.

Because the top and bottom planes are the approximation of the densely-routed environment, and the coupling capacitance is becoming prominent, we ignore the variations on the surfaces of both planes, but set the dielectric thickness (h_1 and h_2) to be random variable. Both wire width and thickness variations are considered, with the same correlation length for simplicity. In this work, we only consider the random variation, and set the variation Std (σ) of width and thickness to be 10% of the nominal value (this makes the 3σ range to be 30% of the nominal dimension).

With different value of the correlation length (η), the test structure will exhibit different magnitude of surface roughness. In Fig. 7, we show the variational geometry of the test structure with different value of η. These pictures are generated with the ICSV model, and are selected from 10000 samples for MC simulation to obtain the maximum top surface fluctuation. The variations of their top-surface z-coordinates are 0.082μm, 0.065μm, and 0.035μm, respectively. In the following experiments, we assume the value of η varies from 0.5μm to 2μm, to reflect the actual surface roughness of interconnects at sub-65nm technology nodes. Changing the value of η also generates test cases with different ratios of structure dimension to correlation length (the L/η ratio). With them, we investigate the validity of the geometric models in this section, and compare the efficiency of different statistical extraction methods in Section IV. In experiments, the MC simulations with 10000 samples are performed. For each deterministic sample structure, the capacitance is extracted with FastCap 2.0 [15].

B. Experimental results

For the test cases, we use the VAW, DSV and ICSV models to describe the variational geometry, and then compare the MC simulation results of statistical capacitance. For the VAW model, there are only five random variables, while the Std of surface variables in DSV and ICSV is set to 7.07% to generate 10% Std of width and thickness (see (9)).

Firstly, we look at the case with η =1μm, which corresponds to the L/η ratio of 1. The simulation errors of the DSV and VAW are listed in Table I, where the results of ICSV are regarded as golden value. Then, other cases with different η and s (wire spacing) are simulated, and the errors of the two models are shown in Fig. 8.

TABLE I
The comparison of the three models (s=0.2μm, η =1μm)

	C_{11} / Error of C_{11}		C_{12} / Error of C_{12}		$C_{1,gnd}$ / Error of $C_{1,gnd}$	
	mean	Std	mean	Std	mean	Std
ICSV[+]	51.54	2.798	-11.19	1.184	-13.39	1.163
DSV	-0.1%	**-25.8%**	-0.1%	**-20.7%**	-0.0%	-0.1%
VAW	-0.6%	**9.0%**	-0.6%	**8.6%**	-0.5%	-1.6%

[+]: The capacitance values are listed, in unit of 10^{-18} F.

From Table I, we can see that the three models have little discrepancy in the mean value of extracted capacitances. However, the Std errors of total capacitance C_{11} and coupling capacitance C_{12} from the both models are prominent. The DSV largely underestimates the capacitance variation, with more than 20% error. The VAW overestimates the capacitance variation, since it is equivalent to an infinite correlation length. Fig. 8 shows the trends of error varying with the ratio of L/η. Experiments with different value of L (wire length) are also performed, which show similar trend as that in Fig. 8, and suggest the L/η ratio is a key factor. The results reveal that the error of VAW is nearly proportional to the value of L/η. If the ratio equals to 2, the error can be as large as 30%. If the ratio is less than 2/3, the error becomes less than 3%.

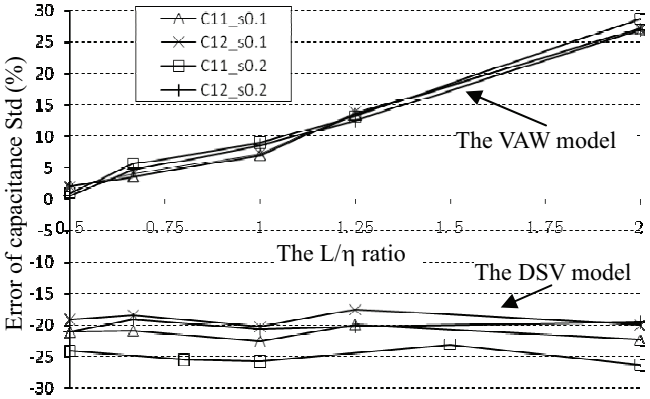
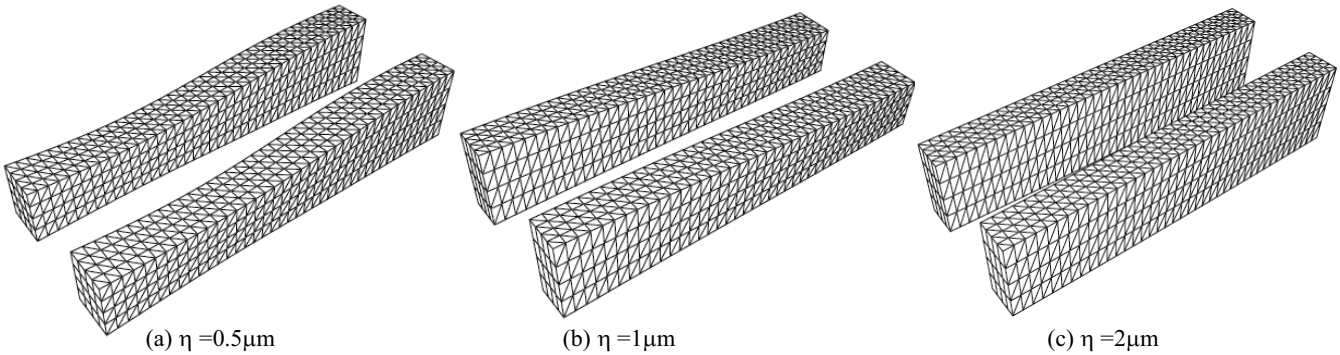


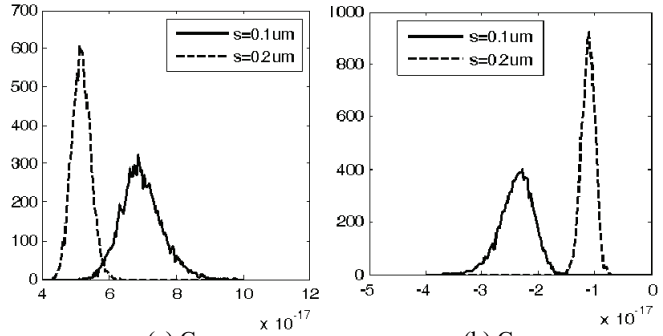
Fig. 8 The relative errors of the VAW model and DSV model in the capacitance Std.

The simulation results also show that the Std of capacitance is larger than 5% of the mean value for C_{11}, and larger than 10% for C_{12}. Fig. 9 gives the PDF of statistical capacitances for the case with η =1μm, which shows skewed probability distributions. It suggests that the quadratic model is need for



(a) η =0.5μm (b) η =1μm (c) η =2μm

Fig. 7 The variational geometry of 1μm-length wires with the maximum top surface fluctuation.



(a) C_{11} (b) C_{12}

Fig. 9 The PDF of statistical capacitances.

statistical capacitance, and the case with smaller wire spacing has more profound quadratic effect.

Based on the experimental results, we give the following criteria regarding statistical capacitance extraction.

CR1. The DSV model always underestimates the Std of both total and coupling capacitances, with at least 20% error.

CR2. The VAW model overestimates the Std of capacitances, with the error proportional to the L/η ratio of extracted structure. For small-size structures with L/η<2/3, the variational geometry can be simplified with VAW model.

CR3. If the Std of the geometric variation is 10% of nominal value, the variational capacitances have skewed distribution requiring quadratic stochastic modeling. But for structure with large wire spacing, the skewness will become minor and the linear model may be sufficient.

IV. Parallel Statistical Capacitance Extraction

We have implemented a new statistical capacitance solver based on the proposed IVCS variation model. The solver employs the techniques of HPC [5] with quadratic model as an efficient non-MC method, and wPFA [6] for variable reduction. For the both of this solver and the MC method, the parallel computing is used for acceleration. The programs are written in MATLAB, which generates the deterministic sample structures and calculates the statistical capacitances. Experiments are carried out to compare the accuracy and efficiency of MC and HPC-based methods with different test cases. All experiments are performed on a Linux server with 8 Xeon CPU cores with 2.13GHz.

A. Implementation details

Incorporating the ICSV model, the weighted PFA and HPC techniques, our solver follows the following algorithm.

Algorithm 1: *The HPC-based statistical capacitance solver*

1. Analyze the nominal geometry to generate covariance matrices of random variables;
2. Factorize the covariance matrices with the weighted PFA technique;
3. Generate the integral points $\{\boldsymbol{\zeta}^{(i)}\}$ of sparse-grid integration, and then covert it to random geometric variables $\{\boldsymbol{\xi}^{(i)}\}$ for the sample structures;
4. Generate the values of derived variables $\{\boldsymbol{\xi}^{*(i)}\}$, and write down the description files of sample structures;
5. For each sample structure, extract capacitances with deterministic 3-D capacitance solvers;
6. Process the results of the deterministic extractions, and calculate key metrics of statistical capacitance.

In Step 1 of the above algorithm, the nominal geometry of extracted structure is firstly discretized into panels. Then, the covariance matrices are generated according to the locations of the panel vertices. For each covariance matrix $\boldsymbol{\Delta n}$, the weighted PFA is employed to express the random variables with a small set of independent variables, with little loss of accuracy. The result of wPFA is an $n\times t$ matrix $\boldsymbol{U}$, where n and t are the numbers of random variables and independent variables, respectively.

In Step 3 of the algorithm, superscript (i) stands for the ith sample structure. The matrix $\boldsymbol{U}$ is used to obtain the value of random geometric variables through $\boldsymbol{\xi}^{(i)}=\boldsymbol{W}^{-1}\boldsymbol{U}\boldsymbol{\zeta}^{(i)}$, where $\boldsymbol{W}$ is a diagonal matrix of weights. We define the weight for variable ξ_i according to the charge around its position. With the capacitance extraction for the nominal structure performed in advance, the charges of panels are assigned to corresponding vertices. So, the diagonal entry of $\boldsymbol{W}$ is:

$$w_i = \sum_{\vec{r}_i \in panel_j} \frac{q_j}{3} \quad , \tag{10}$$

where q_j is the charge of panel j, and $\vec{r}_i$ stands for the vertex corresponding to variable ξ_i. Note the formula of weight (10) is different from that in [6].

In the ICSV model, the whole geometry cannot be constructed with only the sample of random variables. So, in Step 4, the values of derived variables are calculated with interpolation as that in (8). In Step 6, the statistical expression of capacitance is firstly calculated [6], and then the values of mean and Std, or the PDF can be obtained.

It should be pointed out that the main flow in Algorithm 1 is also suitable for the statistical extraction using the MC method. In that scenario, the standard Cholesky factorization, i.e. $\boldsymbol{\Delta n}=\boldsymbol{L}\boldsymbol{L}^T$, is employed in Step 2. Then, in Step 3, $\boldsymbol{\zeta}^{(i)}$ is the ith sample of random variables with $N(0,1)$ distribution, and $\boldsymbol{\xi}^{(i)}=\boldsymbol{L}\boldsymbol{\zeta}^{(i)}$.

In Algorithm 1, the 5th step includes solving capacitances with 3-D field solver. And, the number of samples $N\approx 2d^2$ for a quadratic statistical model, where d is the number of independent variables [5, 6]. Therefore, Step 5 consumes most of the computing time of the statistical capacitance extraction. Because the sample structures are independent from each other, the work can be distributed to multiple processors easily. In this work, we parallelize the Step 4 and 5 in Algorithm 1, with the help of the Parallel Computing Toolbox of MATLAB.

B. Experimental results

According to the **CR2** and **CR3** in last section, we consider the test cases with correlation length η=0.5μm, 0.8μm, 1μm, 1.5μm, and fix the wire spacing s=0.1μm. For the wPFA or the normal PFA, the criterion for truncation error of eigenvalues is set to 0.05.

Table II shows the capacitance errors of the HPC-based method with the wPFA technique, to the results of MC simulation. It validates the good accuracy of wPFA.

TABLE II
The errors of the "HPC+wPFA" method for the four test cases

η (μm)		0.5	0.8	1	1.5
Error for C_{11}	mean	0.2%	0.3%	0.0%	0.2%
	Std	-0.6%	1.1%	-0.9%	0.4%
Error for C_{12}	mean	0.1%	0.4%	0.0%	0.4%
	Std	-1.6%	0.5%	-1.6%	0.0%

In Table III, the number of variables after reduction by the wPFA and normal PFA are compared. The numbers of sample structures they correspond to are also listed, which is the times of invoking the deterministic capacitance solver. This table shows that wPFA can reduce the computing time for 22% or more for the first three cases. For the last case, wPFA cannot make further reduction, since there are only 10 variables.

TABLE III
The computational results of "HPC+wPFA" and MC simulation

η (μm)		0.5	0.8	1	1.5
The L/η ratio		2	1.25	1	0.67
PFA	#variable	26	16	14	10
	#sample	1431	561	435	231
wPFA	#variable	22	14	10	10
	#sample	1036	436	232	232
Reduction by wPFA		**28%**	**22%**	**47%**	**0%**
Time of MC simulation (s)	serial	14501	14500	14477	14518
	parallel	1966	1966	1958	1962
Time of HPC+wPFA(s)	serial	1473.7	610.9	333.2	331
	parallel	200.4	88.4	47.6	46.8
Sp. of "HPC+wPFA" to MC		**9.8**	**22**	**41**	**42**

In Table III, the serial and parallel computational times of the both methods are also listed. From it we can see that both methods achieve about 7X speedup with the parallelization on an 8-core machine. And, the speedup of non-MC method to MC simulation decreases with the increase of the L/η ratio. If L/η=2, the non-MC method is 9.8 times faster than MC method, while the speedup ratio is 42 for the case with L/η=0.67.

We conclude with the following criteria.

CR4. The weighted PFA for statistical capacitance extraction can achieve up to 47% efficiency improvement over the normal PFA, without loss of accuracy.

CR5. The HPC-based method can be easily parallelized, and achieves 7X speedup on an 8-core machine.

CR6. The HPC-based method is tens of times faster than the MC method for the test structures. For larger structures whose dimension is larger than 2X of correlation length η, its speedup to MC method will be lost, and the MC method or other better method (such as [9]) may be the best choice.

V. Conclusions

In this work, an improved continuous surface variation (ICSV) model is proposed to accurately imitate the random geometric variation of on-chip interconnects. Based on the ICSV model, the weighted PFA [6] and HPC [5] techniques, an efficient parallel statistical capacitance solver is then presented. Numerical results validate the advantages of proposed techniques. And with a series of experiments on a typical 65nm-technology structure, six criteria are drawn regarding the statistical capacitance extraction for different scenarios. In the future work, we will further improve the solver using the technique of incremental extraction for the deterministic samples, and combine the proposed model and the efficient technique in [16] to handle the problem of variation-aware resistance extraction.

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