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Stable Backward Reachability Correction for PLL Verification with Consideration of Environmental Noise Induced Jitter

Yang Song, Haipeng Fu, Hao Yu

School of Electrical and Electronic Engineering
Nanyang Technological University
Singapore 639798, Singapore
e-mail: {songyang,hpfu,haoyu}@ntu.edu.sg

Guoyong Shi

School of Microelectronics
Shanghai Jiao Tong University
Shanghai 200240, China
e-mail: shiguoyong@ic.sjtu.edu.cn

Abstract — It is unknown to perform efficient PLL system-level verification with consideration of jitter induced by substrate or power-supply noise. With the consideration of nonlinear phase noise macromodel, this paper introduces a forward reachability analysis with stable backward correction for PLL system-level verification with jitter. By refining initial state of PLL through backward correction, one can perform an efficient PLL verification to automatically adjust the locking range with consideration of environmental noise induced jitter. Moreover, to overcome the unstable nature during backward correction, a stability calibration is introduced in this paper to limit error. To validate our method, the proposed approach is applied to verify a number of PLL designs including single-LC or coupled-LC oscillators described by system-level behavioral model with jitter. Experimental results show that our forward reachability analysis with backward correction can succeed in reaching the adjusted locking range by correcting initial states in presence of environmental noise induced jitter.

I. INTRODUCTION

The design of RF-CMOS based integrated circuit has been in the scale of 40nm and 60GHz with primary applications in high-data-rate communication system [1, 2] such as wireless-HD and wiGiga specifications. At such an extreme scale, the verification of the RF-frontend has become particularly challenging due to heavy EM-coupling and low voltage-swing. For example, the noise injected through substrate or power-supply may significantly affect the sensitive analog/RF blocks such as phase-lock-loops (PLLs)[3] and analog-to-digital converters (ADCs).

As for the high-precision PLL design, random temporal variation of the phase, or called jitter, is one critical performance metric because large jitter can consume clock budget and hence introduce synchronization failure [4, 5, 6]. With careful design of PLL building blocks, the noise contribution of phase detector, the frequency divider, and the loop filter can be reduced to a tolerable level. The dominant noise is thus the phase noise of the VCO. There are possible substrate noise and power-supply noise coupled into the VCO signal path, which can modulate the oscillator signal both in frequency and amplitude [7, 8]. These modulation effects cause sideband spurs around the local oscillator and its harmonics with deviated phase from targeted locking range. The efficient verification of PLL jitter under certain design specification is thereby always one challenge for circuit designers.

In addition to the transistor-level verification of PLL, the system-level verification of PLL has become more and more important for early design stage exploration. Reachability analysis [9, 10, 11] is usually deployed for the PLL safety verification at system level. In a PLL circuit, thousands of switchings are necessary before reached in steady state, which introduces difficulty for the reachability analy-

sis because computation complexity due to switchings can be tremendous. In [11], reachability analysis is deployed to verify locking range of PLL over a set of initial states of charge-pump. The complexity from switchings is overcome by a method named *continuization*. However, it is unknown to consider the environmental noise induced jitter during the PLL verification, which is actually the primary need for most PLL circuit designers. A verification method that can verify PLL with jitter and further present correction is thereby required.

In this paper, a forward reachability analysis with stable backward correction is developed to verify PLL within valid locking range in presence of the environmental noise induced jitter. Firstly, a nonlinear phase noise macromodel is introduced to model substrate and power-supply noise induced jitter for PLL system-level model. Next, the PLL without consideration of jitter can be first verified by the forward zonotope-based [12] reachability analysis. At the same time, the according jitter can be calculated to adjust the PLL locking range. Consequently, an additional backward correction is applied to refine the initial state of PLL based on the adjusted locking range of PLL. Note that the backward reachability analysis was explored in [10] for VCO. However, this method is unstable as system poles are shifted to the right-half plane during the backward trajectory construction. Therefore, error may grow exponentially during the backward correction.

To overcome the stability problem, a calibration method is introduced in this paper by calculating the intersection between the forward and backward trajectories to limit the error growth. As a result, the obtained backward trajectory from the proposed approach will not deviate from the forward trajectory in presence of environmental noise induced jitter. The proposed approach is applied to verify a number of PLL designs including single-LC or coupled-LC oscillators with jitter. Experimental results show that the backward correction can successfully remove the environmental noise induced jitter during the PLL verification. Moreover, the stability calibration can effectively limit the error during the backward correction.

The rest of this paper is organized as follows. Section II discusses the system-level PLL model with addition of the nonlinear phase noise macromodel for jitter. Section III describes the forward reachability analysis with stable backward correction for PLL verification in presence of jitter. The proposed verification methodology is validated in Section IV for a number of single-LC and coupled-LC VCO based PLLs. Conclusions are finally drawn in Section V.

II. PLL SYSTEM MODEL WITH JITTER

A. Nonlinear Phase Noise Model for Jitter

In order to analyze the phase deviation or jitter caused by environmental noise from substrate and power-supply, we introduce a phase-domain macromodel by nonlinear perturbation analysis [6, 8, 13, 14].

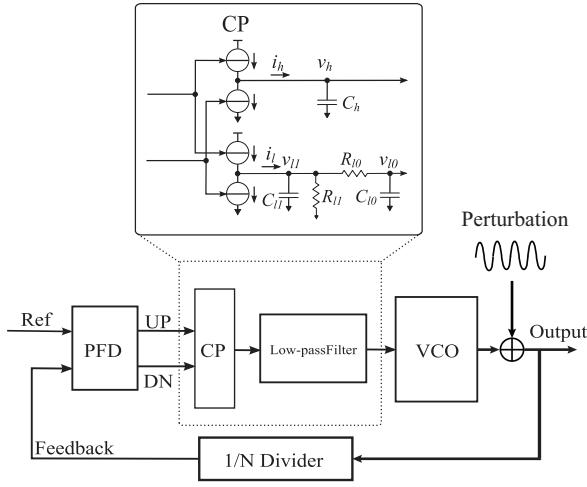


Fig. 1. PLL behavioral model.

An unperturbed oscillator can be expressed as a system of differential equation by

$$\dot{x} = f(x) \quad (1)$$

where $x(t)$ is a vector of state variables and $f(x)$ describes the behavior of the oscillator. The solution of (1) is denoted by $x_{pss}(t)$ which is the unperturbed periodic steady-state (PSS) solution of the oscillator.

A general oscillator under injected perturbation such as environmental noise can be expressed by

$$\dot{x} = f(x) + b(t) \quad (2)$$

where $b(t)$ is the additive perturbation coupled to oscillator. With the presence of small nonzero perturbation $b(t)$, solution of (2) can be approximated by

$$x(t) = x_{pss}(t + \alpha(t)) \quad (3)$$

where $\alpha(t) \in \mathbf{R}$ is the phase deviation caused by perturbation $b(t)$. $\alpha(t)$ can be obtained from nonlinear differential equation

$$\dot{\alpha}(t) = v(t)^T (t + \alpha(t)) \cdot b(t) \quad (4)$$

As such, jitter can be obtained by multiplying $\alpha(t)$ by free running oscillation frequency ω_0 .

Note that $v(t) \in \mathbf{R}^n$ is called perturbation projection vector (PPV). The PPV is a special projection vector of the perturbations and is calculated according to Floquet theory. It is a periodic function having the same period as the oscillator and can be computed directly from PSS solution. PPV can be computed by effective numerical methods [6]. Moreover, when the jitter is calculated from the nonlinear phase noise macromodel, one can superpose it into the system behavioral model of PLL. In each cycle of PLL, phase of oscillator deviates from unperturbed periodic steady-state. Phase deviation should be considered when computing locking range of oscillator.

B. PLL Behavioral Model with Jitter

As shown in Fig.1, a typical charge-pump PLL circuit is often composed of four main components, which are phase frequency detector (PFD), charge-pump (CP), voltage-controlled oscillator (VCO), and a feedback frequency divider. The behavioral model of the PLL [11] (Fig.1) can be described by

- the state vector $x = [v_h \ v_{l1} \ v_{l0} \ \Phi_v \ \Phi_{ref}]$;
- the input vector $u = [i_h \ i_l \ f_0 \ f_{ref}]$;

- $\Phi_v, \Phi_{ref}, f_0, f_{ref}$ for the reference signal phase, feedback signal phase, VCO central frequency and reference signal frequency, respectively.

Then, the unperturbed state space equation is expressed by (5)

$$\dot{x} = f(x) = Ax + Bu \quad (5)$$

where A is system matrix and B contains connection information of input vector.

$$A = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_{11}} \left(\frac{1}{R_{11}} + \frac{1}{R_{10}} \right) & \frac{1}{C_{11}R_{10}} & 0 & 0 \\ 0 & \frac{1}{C_{10}R_{10}} & -\frac{1}{C_{10}R_{10}} & 0 & 0 \\ \frac{K_h}{N} & 0 & \frac{K_l}{N} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad (6)$$

$$B = \begin{bmatrix} \frac{1}{C_h} & 0 & 0 & 0 \\ 0 & \frac{1}{C_{11}} & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{2\pi}{N} & 0 \\ 0 & 0 & 0 & 2\pi \end{bmatrix}. \quad (7)$$

Note that u is determined by the PFD output, which is actually related to the state vectors Φ_v and Φ_{ref} . One can describe this nonlinear behavior using the following behavior statements: if $\Phi_v > \Phi_{ref}$ then $i_h = I_h$ ($I_h > 0$), $i_l = I_l$ ($I_l > 0$); otherwise $i_h = -I_h$, $i_l = -I_l$.

Based on the system equation (5), the unperturbed feed-back signal phase satisfies (8)

$$\dot{\Phi}_v^{pss} = \frac{1}{N} (K_h v_h + K_l v_{l0} + 2\pi f_0). \quad (8)$$

By solving (8) the unperturbed feed-back phase $\Phi_v^{pss}(t)$ is obtained.

In the noisy PLL model, jitters are supposed to superpose the unperturbed phase by

$$\Phi_v = \frac{1}{N} \int_0^t (K_h v_h + K_l v_{l0} + 2\pi f_0) d\tau + 2\pi f_0 \alpha(t). \quad (9)$$

As such, leveraging the nonlinear phase noise model (4) discussed above, the perturbed phase or jitter is expressed in an integral form (9).

III. PLL REACHABILITY ANALYSIS WITH CORRECTION

The system level PLL verification is mainly based on the so-called reachability analysis [9, 11]. A reachable set is the collection of all trajectories that a system may visit within a given range of time. By exploring all potential trajectories of the system, one can check if the system will end up in unsafe states. Applications of reachability analysis include formal verification of continuous, hybrid or discrete system. In PLL circuits, phase difference between reference signal and oscillator should be locked within a certain range after the PLL system settles down in steady state. As such, the reachability analysis is performed to make sure that the final state of PLL settles within the locking range.

In this section, the basic concepts of reachability analysis by zonotope is presented, followed by forward reachability analysis and stable backward correction for PLL circuits with jitters.

A. Zonotope and Over-approximation

By introducing hypercube for representation of approximation around nominal trajectories, one can obtain a convex hull to enclose

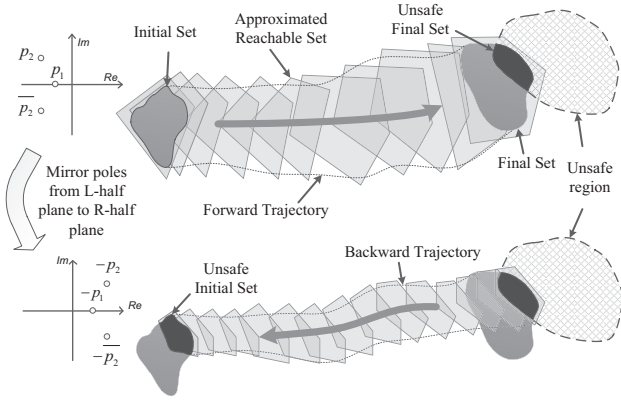


Fig. 2. Forward and backward trajectories with pole mirroring.

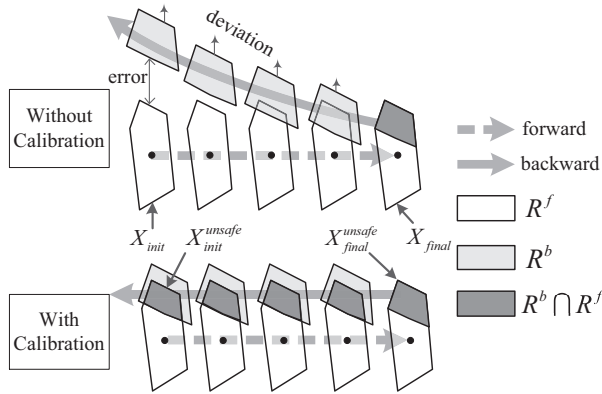


Fig. 3. Backward trajectories with and without stability calibration.

more-likely trajectories. One simple and symmetrical type of hypercube, *zonotope* [12] is defined as:

$$Z = \{x \in \mathbf{R}^n : x = c + \sum_{i=1}^q [-1, 1]g^{(i)}\} \quad (10)$$

where c is the center and $g^{(i)}$ are called *zonotope generators*. The generator representation of a zonotope is called a G-representation [9]. It can be efficiently deployed during the reachability analysis.

However, note that it is difficult to use G-representation to compute intersection of two sets, which is important during the stable backward correction to be discussed later. The other important representation of zonotope is V-representation, which can represent a zonotope with a set of vertices. V-representation of zonotope is thereby useful when detecting and computing the intersection of two sets for the stable backward correction.

As a result, the conversion from V-representation to G-representation is necessary when projecting intersected area of polytopes to a common reachable set. Firstly, a paralleloptope enclosure of polytope is calculated as below

$$Z = \Lambda \cdot \text{box}(\Lambda^{-1}P) \quad (11)$$

where Λ is a full-ranked matrix whose column vectors are base vectors of paralleloptope, and P is a set of vertices. In addition, $\text{box}()$

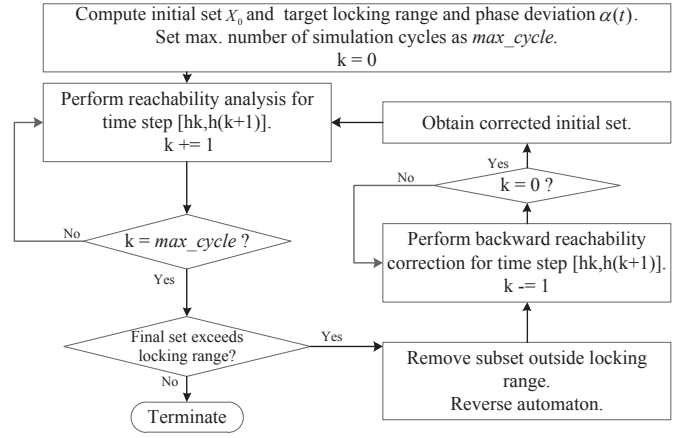


Fig. 4. Flow chart of PLL reachability analysis with backward correction.

operation returns an enclosing axis-aligned box of a set. As a result, a G-representation of order 1 can be constructed easily based on a given paralleloptope. But over-approximation is inevitably introduced when a polytope is reduced to a paralleloptope of lower order. The detailed illustration of zonotope conversion can be found in [9].

B. Forward Reachability Analysis

To verify a perturbed PLL locking, the forward reachability analysis starts with a linear continuous system expressed by (12) below

$$\dot{x} = Ax + Bu + b(t). \quad (12)$$

It allows to separate the unperturbed solution into two parts: the homogeneous solution with respect to the initial state when there is no input; and the inhomogeneous solution accounting for the system input when the initial state is the origin. As a result, given an initial set for one time step, two sets of solutions are computed and added together by a so-called Minkowski sum. Note that the entire algorithm of reachable is shown in Algorithm 1, where \oplus denotes Minkowski sum and $R([0, t_f])$ is the reachable set for $t \in [0, t_f]$.

Algorithm 1: Reachability Analysis

Input: Initial set X_0 , system matrix A , input vector Bu , simulation interval r , time horizon t_f .

Output: $R([0, t_f])$

Initial state solution for $t \in [0, r]$:

$$H_0 = \text{convex_hull}(X_0, e^{Ar}X_0)$$

Input solution for $t \in [0, r]$: $V_0 = F(Bu, r, A)$

Reachable set for $t \in [0, r]$: $R_0 = H_0 \oplus V_0$

for ($k = 1; k < t_f/r; k++$) **do**

$$H_k = e^{Ar}H_{k-1}$$

$$V_k = e^{Ar}V_{k-1}$$

$$R_k = H_k \oplus V_k$$

end for

$$R([0, t_f]) = \bigcup_{k=1}^{t_f/r} R_{k-1}.$$

As for PLL circuit, reachability analysis may have complexity challenge as thousands of switchings of charge-pumps are necessary for the convergence of system state. In [11], a *continuization* method is introduced, in which each simulation time-step has a fixed span with respect to the reference signal. For one step, reachability analysis is

performed to consider the possible behavior of a charge-pump PLL circuit

$$X_{k+1} \in e^{At_{cycle}} X_k \oplus X_{const} \oplus X_{up} \oplus X_{both} \oplus X_{down} \quad (13)$$

where reachable set X_{k+1} contains different components including: initial state solution ($e^{At_{cycle}} X_k$), and input solutions when charge-pump is being charged (X_{up}), discharged (X_{down}) or when both current drives are active (X_{both}).

More importantly, to consider the environmental induced perturbation, phase deviation of oscillator is introduced to *continuization* in this paper by considering jitter when approximating active time of charge-pump (14):

$$\begin{aligned} t_{active} &\in [\bar{t}_{active}, \bar{t}_{active}] \\ &= \{(\Phi_v + 2\pi f_0 \Delta\alpha(t)) / \dot{\Phi}_v \\ &\quad | \Phi_v \in [\underline{u}, \bar{u}], \dot{\Phi}_v \in [\underline{v}, \bar{v}]\} \end{aligned} \quad (14)$$

where $\Delta\alpha(t)$ is increment of phase deviation in current cycle.

If the final set X_{final} intersects the unsafe region (Fig.2), it is simply a geometric matter to find out unsafe subset X_{final}^{unsafe} . However, the forward reachability analysis can only verify whether a design is safe or not but it cannot perform automatic correction. The issue of correction is addressed in the following part.

C. Backward Reachability Correction

Backward reachability correction can further calibrate the unsafe initial sets by computing backward trajectory and its intersection with X_{init} . After getting rid of the unsafe subset of X_{init} , initial states are adjusted to ensure a corrected PLL design, for example, under the noise induced jitter. As for PLL circuit, phase difference between oscillator and reference signal in time domain as jitter can be limited within certain locking range such as $[-0.1, 0.1] \cdot 2\pi$. Therefore, one can first apply the forward reachability analysis to detect the phase difference violation due to jitter at the steady state [11]; and then correct the phase difference violation by performing a correction based on the backward reachability analysis.

Similar to the backward reachability analysis in [10], the automaton needs to be reversed when backward correction is performed. For example, the reverse automaton is obtained by reversing the transition relations, by reversing the sign of the derivatives in (15), and then by swapping initial and final states as well. As such, one can obtain a reverse linear differential equation below

$$-\dot{x} = Ax + Bu + b(t), x(0) \in X_{final}. \quad (15)$$

Note that after reversing the sign of the derivatives, system poles are all mirrored from the left-half plane to the right-half plane (Fig.2), which turns a stable system into unstable. Therefore, the integration error can grow exponentially in an unstable system and interrupt the signal eventually. In the PLL system-level verification, the integration error is inevitably generated due to the conversion between analog and digital/logical signal. Moreover, the over-approximation can introduce extra error as well (11). Therefore, the backward trajectory based on [10] can deviate from the forward trajectory within only a few steps and hence can ruin the backward correction easily. As a result, calibration must be performed to ensure the stability during the backward reachability analysis.

As shown in Algorithm 2, we propose a method to calibrate the backward trajectory R^b with the reference to the stored forward trajectory R^f . Specifically, as shown in Fig.3, polytope intersection $R^b \cap R^f$ between the forward trajectory and backward trajectory is

calculated at the beginning of each time step and projected to a reachable set (11), which is used as the initial set for current step (16).

$$\begin{aligned} R_k^b &= R^b([kh, (k+1)h]) \\ R_{k-1}^b &= f_{step}^b(R_k^b \cap R^f([0, t_f])) \end{aligned} \quad (16)$$

Therefore, one can make sure that the integration error during the backward correction does not grow unboundedly. The flowchart of the complete forward reachability analysis with backward correction flow is summarized in Fig.4.

Algorithm 2: Backward Reachability Correction

Input: Final set $X_{t_f/r}$, forward trajectory $R^f([0, t_f])$, system matrix A , input vector Bu , simulation interval r , time horizon t_f .

Output: Backward reachable sets $R^b([0, t_f])$.

Backward initial state solution for $t \in [t_f - r, t_f]$:

$$H_{t_f/r-1}^b = \text{convex_hull}(X_{t_f/r}, e^{-Ar} X_{t_f/r})$$

Backward input solution for $t \in [t_f - r, t_f]$:

$$V_{t_f/r-1}^b = F(-Bu, r, -A)$$

Backward reachable set for $t \in [t_f - r, t_f]$:

$$R_{t_f/r-1}^b = H_{t_f/r-1}^b \oplus V_{t_f/r-1}^b$$

for ($k = t_f/r - 1; k > 0; k--$) **do**

$$H_{k-1}^b = e^{-Ar}(R_k^b \cap R^f([0, t_f]))$$

$$V_{k-1}^b = e^{-Ar} V_k^b$$

$$R_{k-1}^b = H_{k-1}^b \oplus V_{k-1}^b$$

end for

$$R^b([0, t_f]) = \bigcup_{k=1}^{t_f/r} R_{k-1}^b$$

IV. EXPERIMENTAL RESULTS

The proposed forward reachability analysis with backward correction is implemented to verify PLL circuits. Parameter list of the PLL is similar to [11]. The VCO circuits are shown in Fig. 5 for both single-LC and coupled-LC oscillators, which make the primary phase noise or jitter contribution. The behavioral model of PLL with jitter is built in MATLAB with implementation of nonlinear phase-noise macromodel. Manipulation of polytopes used in reachability analysis is performed by Multi-Parametric Toolbox (MPT) [15] integrated in MATLAB. All the experiment results are collected on an Intel Core i5 server with 3.2GHz processor and 8GB memory.

Firstly, a comparison between the PLL models with and without jitters is made in Fig. 6. In this case, the initial node voltage of v_h of PLL in Fig.1 is set as [3.965V, 4.035V]. Node voltages v_{l0} and v_{l1} of PLL in Fig.1 are both set to 0.5V. As such, the normalized PLL locking range $(\Phi_v - \Phi_{ref})/2\pi$ becomes $[-0.1, 0.1]$. Moreover, the number of simulation cycles is 2000. The environmental noise induced phase deviation is assumed as $0.01rad$, which is introduced by a perturbation to each simulation cycle. Unperturbed and perturbed PLL trajectories are shown in Fig.6. One can observe that the environmental noise induced jitter can cause the final set of states to deviate from the initially assumed locking range. Therefore, the verification of PLL with consideration of jitter is quite a need when performing the reachability analysis.

Then, the validation of the proposed backward correction is inspected. We first consider case A, a PLL design with one single-LC oscillator (Fig.5). This oscillator is governed by the differential equation (17),

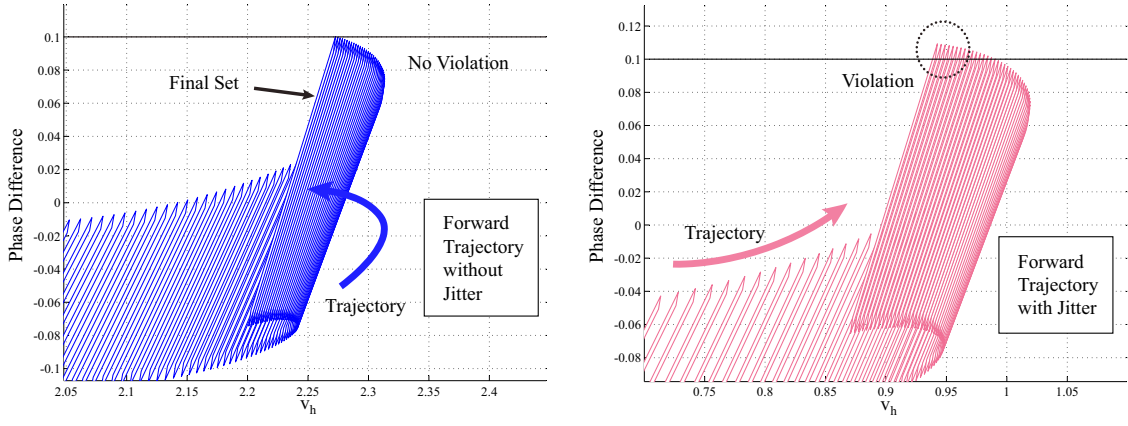


Fig. 6. Unperturbed and perturbed PLL trajectories with and without jitter.

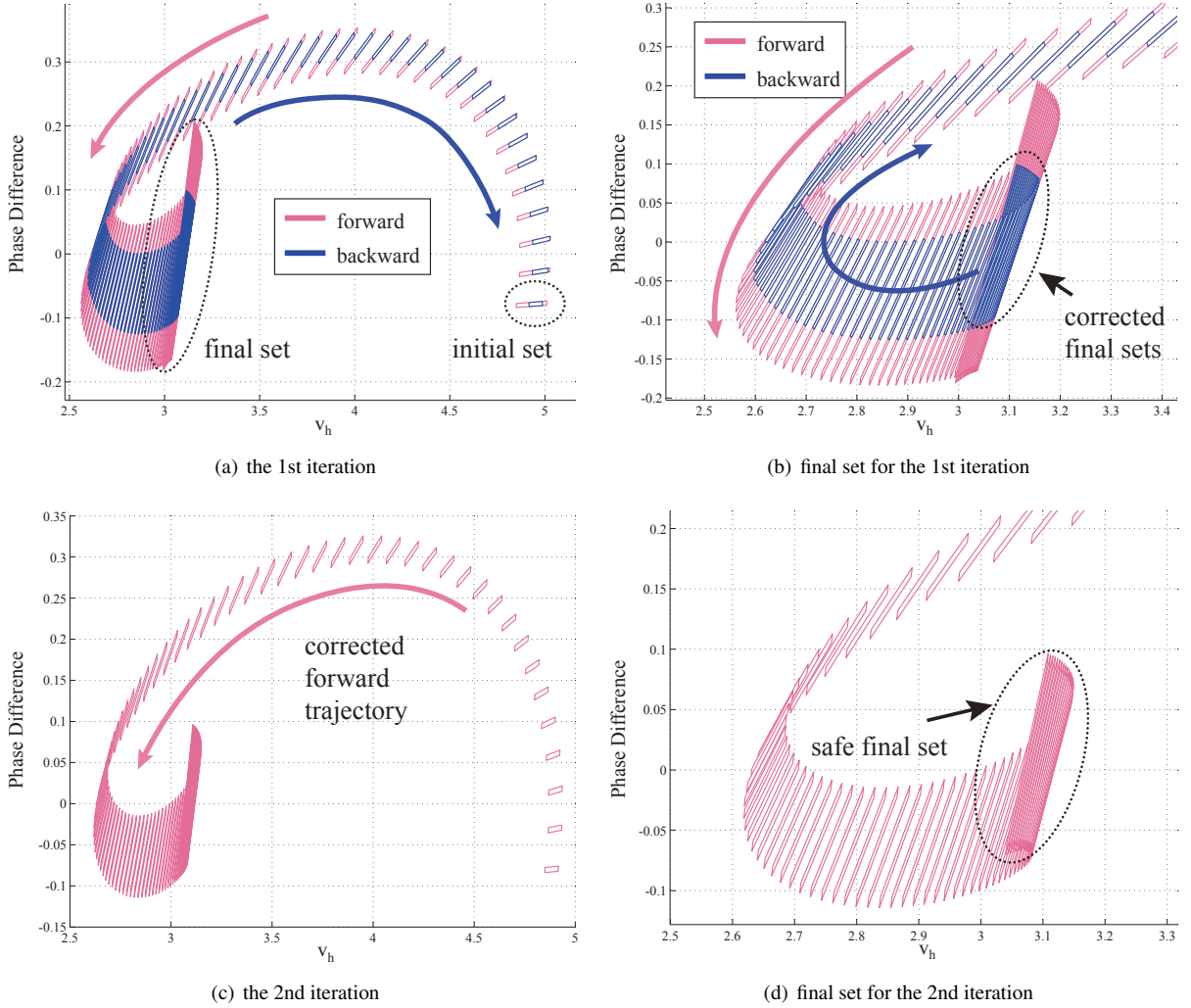


Fig. 7. PLL verification under jitter by forward reachability analysis with backward correction.

$$\begin{aligned}
 C \frac{dv(t)}{dt} + \frac{v(t)}{R} + i(t) + S \cdot \tanh\left(\frac{G_n}{S} v(t)\right) &= b(t) \\
 L \frac{di(t)}{dt} - v(t) &= 0
 \end{aligned} \quad (17)$$

in which $L = 640pH$, $C = 192fF$, $R = 0.0005\Omega$ and $G_n = 7.5mS$. With these parameters, one can find that the inductor current in the single-LC oscillator has an amplitude $A_0 = 2.2mA$. We assume that the environmental noise induced perturbation current

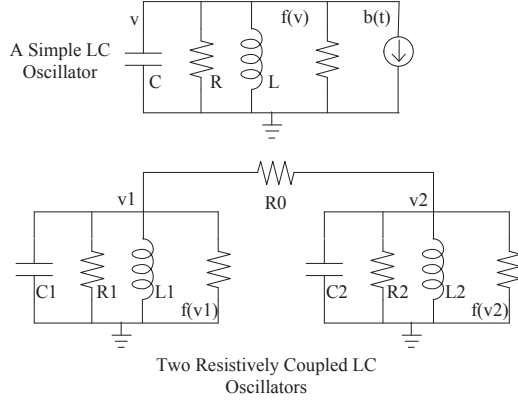


Fig. 5. VCO by single and coupled LC oscillators.

t is $0.001A_0\sin(0.999999\omega_0t)$. Based on the nonlinear phase noise simulation by PPV, the perturbation caused phase deviation is found -0.0062rad per cycle. Moreover, the initial range of node voltage v_h is $[4.9V, 5.1V]$. Other node voltages are set as $v_{l1} = v_{l0} = 0.5V$. The maximum number of simulation cycles is 2000.

TABLE I
PERFORMANCE OF REACHABILITY ANALYSIS FOR PLL WITH LC
OSCILLATORS

Oscillator	Iter.	Time(s)	Init. State (v_h)	Final State ($(\Phi_v - \Phi_{ref})/2\pi$)
case A	1	202.99	[4.82, 4.98]	[-0.18, 0.21]
	2	69.98	[4.82, 4.89]	[-0.07, 0.10]
case B	1	187.95	[2.90, 3.10]	[-0.22, 0.26]
	2	74.68	[2.90, 2.96]	[-0.06, 0.09]

As a result, the forward and backward trajectories of case A derived from reachability analysis are shown in Fig.7, in which the forward trajectory is painted in light purple and the backward trajectory is in dark blue. In the first iteration, the final set $[-0.18, 0.21]$ overflows the allowed phase locking range $[-0.1, 0.1]$ (Fig.7(a)) due to jitter. By performing the backward correction, we trace back to the initial set and obtain the adjusted initial set $[4.82, 4.89]$ (Fig.7(b)). In the second iteration, we start from the corrected initial set obtained from the last step and perform the forward reachability analysis again (Fig.7(d)). As shown in Fig.7(d), the final set ends up in the desired locking range $[-0.1, 0.1]$. As such, the whole correction procedure completes within two iterations in minutes, which is much less than the time needed for trial-and-error simulation. The initial set and final set for each iteration are summarized in Table I.

Next, as for case B, we use resistively coupled-LC oscillator (Fig.5). Circuit parameters of coupled-LC oscillator are the same with case A but with $R_0 = 10k\Omega$. The environmental noise induced perturbation current is assumed as $0.01A_0\sin(1.000002\omega_0t)$. After P-PV based nonlinear phase noise simulation, the phase deviation of the coupled-LC oscillator is found as 0.012rad per cycle. Moreover, the initial range of v_h is set as $[2.90, 3.10]$. The other simulation setup is the same as case A. After the first iteration, the initial state is adjusted down to $[2.90, 2.96]$. The second iteration proves that the new initial state $[2.90, 2.96]$ can result in a safe final state. The initial set and final set for each iteration are summarized in Table I.

V. CONCLUSIONS

In this paper, a system behavioral model of PLL circuits with jitter from environmental noise has been introduced. A forward reachabil-

ity analysis with stable backward correction is proposed and applied to verification of PLL phase locking under jitter. The challenge of backward correction stems from instability of system equation when tracing back in time. A method for calibration is presented to overcome instability of backward trajectory. Experimental results were collected from two test cases with different oscillators and initial states. It has been shown that by adjusting initial sets, backward correction helps PLL converge to desired locking range quickly. Future work of our research will focus on backward correction with multiple state variables for system uncertainties from not only noise but also from mismatch.

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