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A 31-μW, 148-fs Step, 9-bit Capacitor-DAC-Based Constant-Slope Digital-to-Time Converter in 28-nm CMOS

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***Abstract*— This article proposes a power-efficient highly linear capacitor-array-based digital-to-time converter (DTC) using a charge redistribution constant-slope approach. A fringe-capacitor-based digital-to-analog converter (C-DAC) array is used to regulate the starting supply voltage of the constant discharging slope fed to a fixed-threshold comparator. The DTC operation mechanism is analyzed and design tradeoffs are investigated. The proposed DTC consumes merely 31 μW from a 1-V supply when clocked at 40 MHz, while achieving a fine resolution of 148 fs over a 9-bit range. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are 0.96/1.07 LSB.**

***Index Terms*— Capacitor-based digital-to-analog converter (C-DAC), constant slope, digital-to-time converter (DTC), femtosecond resolution, integral nonlinearity (INL), phase-locked loop (PLL), power-efficient, ultra-low power (ULP).**

I. Introduction

AS AN important building block in time-domain signal processing [1], a digital-to-time converter (DTC) delays the transition edges of its input signal (e.g., clock) by an amount dynamically controlled by a digital code. It is increasingly utilized in various applications that exploit fast and precise edge manipulations in scaled low-voltage CMOS technology, e.g., polar transmitters [2], phase-locked loops (PLLs) [3]–[5], [7], [8], [10], [12], [13], direct-digital frequency synthesis (DDFS) [14], sampling oscilloscopes [15], and successive approximation time-to-digital converters (SAR-TDCs) [16].

Traditionally, to achieve low in-band phase noise in an all-digital PLL (ADPLL), a fine-resolution TDC with a dynamic range of at least one oscillator period is required [1]. Such a wide range makes it one of the most power-hungry blocks in the ADPLL [after the digitally controlled oscillator (DCO)]. Moreover, high linearity is essential in avoiding significant in-band fractional spurious tones.

In recent years, the DTCs have aroused significant interest in the design of PLLs [4], [5], [11], [13], [27], [28]. A DTC can reduce the TDC detection range in a fractional-N ADPLL via a reference clock edge prediction and realignment. With the assistance of the DTC, one can greatly reduce power consumption of the phase detection circuitry, which can now employ a TDC with a much narrower range. This is instrumental in pushing the ADPLL's power consumption to below 1 mW for Bluetooth low-energy (BLE) applications [4], [5]. However, [4] suffers from large fractional spurs due to the DTC's nonlinearity. A phase-dithering technique was adopted in the later version [5]. The literature also reports a DTC used to dither the reference clock over an ADPLL to suppress its spurs at near integer-N channels [17], as well as ADPLLs achieving fractional-N operation based on a conventional integer-N PLL architecture [7], [10]. The dynamic range of the DTC can be relaxed by using multi-phase outputs from a DCO divider or a coarse–fine DTC architecture [6], [12]. It can further be reduced with an assistance of a phase interpolator (PI) in the feedback path [7]. A DTC with a fine resolution can reduce its quantization noise contribution in the PLL.

A generic DTC topology would consist of input and output buffers in addition to a variable delay-generation part. One popular DTC propagates the signal through a digitally controlled delay chain comprised of inverters/buffers [4]. This approach suffers from limited resolution and high power consumption due to a large number of delay cells. For high-resolution DTCs, special attention is paid to the input–output buffers to isolate the delay-generation part from the outside interference. For example, in [10], the DTC delay unit is built as a cascade of two inverters, each loaded with tunable MOS capacitors, and extra buffers are added to isolate each delay unit. By controlling the MOS capacitance, the loading of each of the two inverters has two states, generating two different delays. That architecture suffers from a MOS capacitance mismatch among different units. Thus, the DTC resolution and nonlinearity are limited by the manufacturing variations.

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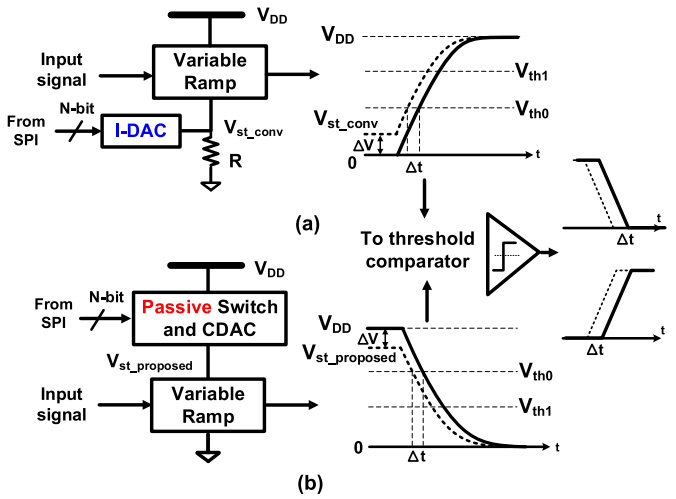

Fig. 1. Conceptual diagram of the delay-generation circuit in (a) conventional constant-slope DTC using I-DAC [19] and (b) proposed constant-slope DTC using passive C-DAC.

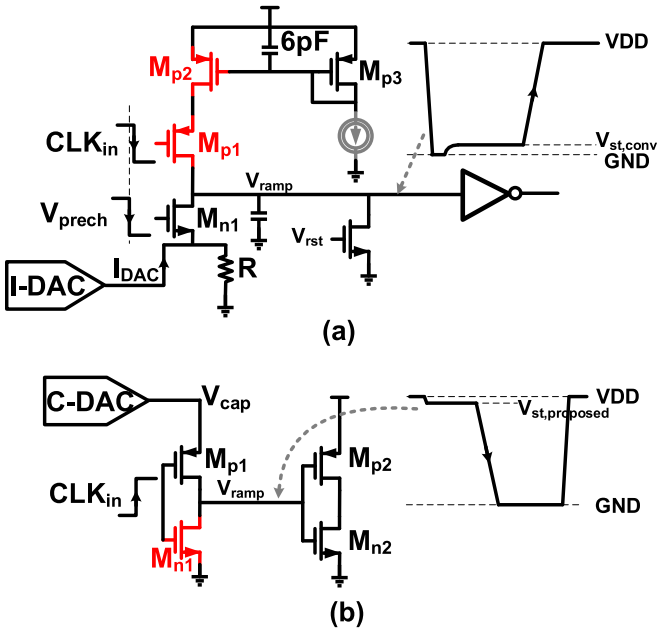

Fig. 2. Detailed comparison of (a) conventional constant-slope charging DTCs adopting I-DAC [19] and (b) proposed constant-slope-discharging DTC adopting C-DAC.

Another popular method in [18] regulates a variable voltage ramp driving a threshold comparator. The variable ramp generator can be simply modeled as a first-order *RC* circuit. The slope of the voltage ramp is controlled through tunable capacitances. Even though the DTC can achieve fine resolution <500 fs [12], [18], it suffers from poor linearity due to a nonlinear relationship between the propagation delay and the input ramp time. This problem can be alleviated by exploiting a constant-slope method [3], [19], which generates voltage ramps with different starting voltages. As shown in Fig. 1(a), the slope is maintained and it ideally produces a linear relationship if the following threshold comparator has a constant sampling aperture. Despite the significant improvements in resolution and linearity, the main power contributor in [19] is the current digital-to-analog converter (I-DAC), which consumes 1 mW. To reduce the power consumption of I-DAC, an isolation technique of ramp signal, and offset generations was proposed in [3] in which the DAC has to only charge a 10× smaller capacitor. However, since the architecture still needs an independent DAC and a cascoded current mirror, the power consumption is 98 μW at 26 MHz.

In this article, we propose a new architecture of the constant-slope DTC that achieves much lower power consumption while maintaining high resolution and linearity. By exploiting a passive capacitor-based DAC (C-DAC) as part of the ramp generator, the power consumption is significantly reduced through charge redistribution. The capacitive DAC regulates the supply of the ramp generator, creating a linearly stepped starting voltage for the constant discharging slope. The high linearity of the DTC is ensured by the constant-slope method and excellent matching of C-DAC's metal–oxide–metal (MOM) capacitors as well as a built-in predistortion. The C-DAC design follows the principles and derives benefits from a successive approximation register analog-to-digital converter (SAR-ADC) architecture [21], [22]. The C-DAC output supplies the threshold comparator such that different supply voltages generate proportional delays with extremely fine resolution through the constant-slope discharging process, as shown in Fig. 1(b).

In the rest of this article, Section II explains the proposed concept of constant-slope discharging using the programmable passive C-DAC. Design details of the proposed DTC architecture are described in Section III. The experimental results are shown in Section IV. At last, the conclusions are given in Section V.

II. Charge-Redistribution Constant Slope

A. Constant-Slope Discharging

Comparison between the DTC variable-slope and constant-slope methods can be found in [19]. Briefly, the delay is controlled in the former by varying the signal's voltage transition slope at its rising (i.e., significant) edges. However, this suffers from a systematic nonlinearity (see [19, Fig. 7]) due to the rise time versus delay dependence in practical comparators. In contrast, the constant-slope method maintains the same slope at every ramp. The conventional constant-slope DTCs employ an I-DAC, as shown in Fig. 1(a). A variable start voltage ($V_{\text{st\_conv}}$) is used to linearly program the variable delay. All ramps above a certain $V_{\text{st\_conv,max}}$ have the same shape, thus exerting the same influence on the following comparator. Considering a more practical model of the comparator, the output voltage transition mainly responds to a "soft" range of input voltages [V_{th0}, V_{th1}]. As long as $V_{\text{st\_conv,max}} < V_{\text{th0}}$, it is reasonable to assume the comparator does not add extra nonlinearity, irrespective of the comparator's bandwidth.

The proposed C-DAC-based constant-slope DTC shown in Fig. 1(b) inherits the benefits of the conventional I-DAC structure but with additional advantages derived from the constant-slope discharging, rather than the constant-slope charging as in [19]. As a result, the start voltage here ranges from $V_{\text{st,min}}$ to V_{DD}, in contrast with the ground-to-$V_{\text{st,max}}$ range in the I-DAC-based DTC. The differences are shown in Fig. 2. For both the DTCs, the difference in the voltage ramp

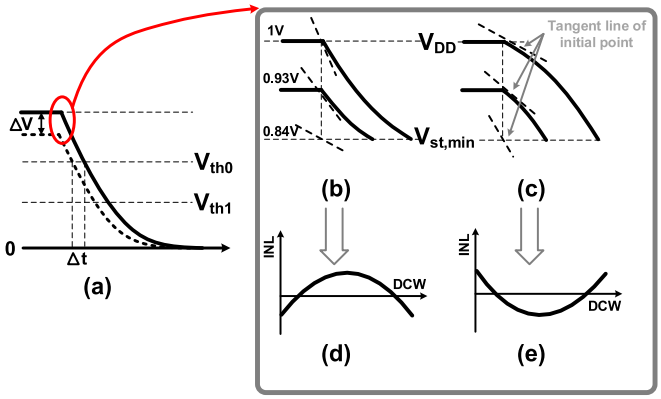

Fig. 3. Built-in predistortion decomposition. (a) Discharging slope influenced by (b) channel-length modulation and (c) variable loading capacitance. Induced INL from (d) channel-length modulation and (e) from variable loading capacitance.

is within the start voltage ranges. Note that the output delay can be expressed as $\Delta t = \Delta V/(I/C)$, where I/C is the ramp slope. We will discuss I and C in the following regarding their influences on Δt, which contains DTC nonlinearity effects.

Due to the channel-length modulation, the current is not constant, since the drain voltage changes in the saturation mode. The drain current is given by [20]

$$I = \frac{1}{2}\mu_n C_{\text{ox}} \frac{W}{L}(V_{\text{GS}} - V_{\text{th}})^2(1 + \lambda_I V_{\text{DS}}). \tag{1}$$

To partially alleviate this issue in the prior-art circuits, a 6-pF capacitor is connected to the gate of M_{P2} to stabilize its V_{GS} voltage, as shown in Fig. 2(a). The cascode transistor M_{P1} helps to stabilize the drain voltage of M_{P2}. The charging *current* is thus less sensitive to the variable starting voltage V_{st}. At the same time, to achieve a *fixed* capacitance of the V_{ramp} node, a big capacitor is attached to that node. Its value should be large enough so that it suppresses the MOS parasitics, thus dominating the V_{ramp} node's capacitance. Similar issues could also affect the proposed DTC architecture. During the discharging process, various DTC control codes produce varying V_{st}, which is the V_{DS} of the discharging NMOS. Without the isolating cascode current mirror, the channel-length modulation effect would be more severe. However, it is interesting to point out that V_{ramp} node's capacitance also increases with the voltage. In other words, the V_{ramp} node manifests a varactor property, which compensates the nonlinearity induced by the channel-length modulation when properly sized, as shown in Fig. 3.

With only the channel-length modulation effect, the discharging current would reduce as V_{ramp} drops, making the discharging curve convex. On the other hand, when only the variable loading capacitance effect exists, the slope increases as V_{ramp} drops, forcing the discharging curve to be concave. The dashed lines in Fig. 3(b) and (c) are slopes at the points of interest. Fig. 3(d) corresponds to the case when the channel length modulation effects dominate the nonlinearity contribution. The integral nonlinearity (INL) in Fig. 3(e) indicates that the variable loading capacitance exerts more influence than the channel length modulation. Those two opposing effects

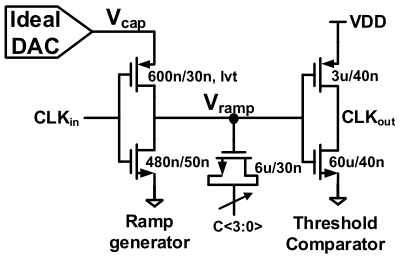

Fig. 4. Schematic of the DTC core with ideal DAC feeding V_{cap}.

can roughly compensate, with the latter acting as a built-in predistortion for the former across a certain voltage range.

B. PVT Sensitivity

To verify the effectiveness of the proposed technique, Fig. 4 schematic is now simulated under different process, voltage, temperature (PVT) variations. The circuit comprises the DTC core $M_{\text{P1,N1,P2,N2}}$ with an ideal DAC to generate V_{cap} ranging from 0.8 to 1 V while the incoming clock runs at 40 MHz. The control code C⟨3:0⟩ is set to "1100" in the PVT sensitivity analysis. Post-layout simulations indicate the typical range of ∼80 ps. Fig. 5(a) shows the post-layout simulation results over five process corners. The worst case INL is maintained within 2 LSBs over the 9-bit range. To check for the temperature and voltage variations, the INL is simulated at 0.9- and 1.1-V supply voltages at room temperature, as well as at −50°C and 120°C at 1-V supply, respectively, as shown in Fig. 5(b). Its worst case INL is slightly larger than 1 LSB over the 9-bit design. Specifically, at the lower supply of 0.9 V, due to the slope of the ramp node capacitance against the ramp voltage being steeper, the varactor effect dominates. As a result, the INL curve tends to be convex, which is aligned with the analysis in Fig. 3(e). As compared with [19, Fig. 13], the proposed architecture features comparable linearity but at a much lower complexity and power consumption.

C. Trial Calibration

In order to allow for a possible calibration of the nonlinearity, four identical MOS capacitors were added in this article (missing in our earlier version in [9]) between the ramp node and the ground, as shown in Fig. 4. When we enable (EN) all the MOS capacitors with the calibration control code "0000," the varactor effect dominates when compared with the light-loading case of "1111," which shows a desired S-shape. Code "0000" thus causes the INL curve to become convex. The conclusion is verified by the post-layout simulations in Fig. 5(c).

III. Proposed Digital-to-Time Converter

This design is based on our charge-sharing constant-slope DTC topology originally proposed in [9]. In this article, four identical MOS capacitors are added at the V_{ramp} node for fine-tuning the INL. Furthermore, the original 5-bit topology was extended to 9 bits, while the layout and the MOS transistor sizes were additionally optimized.

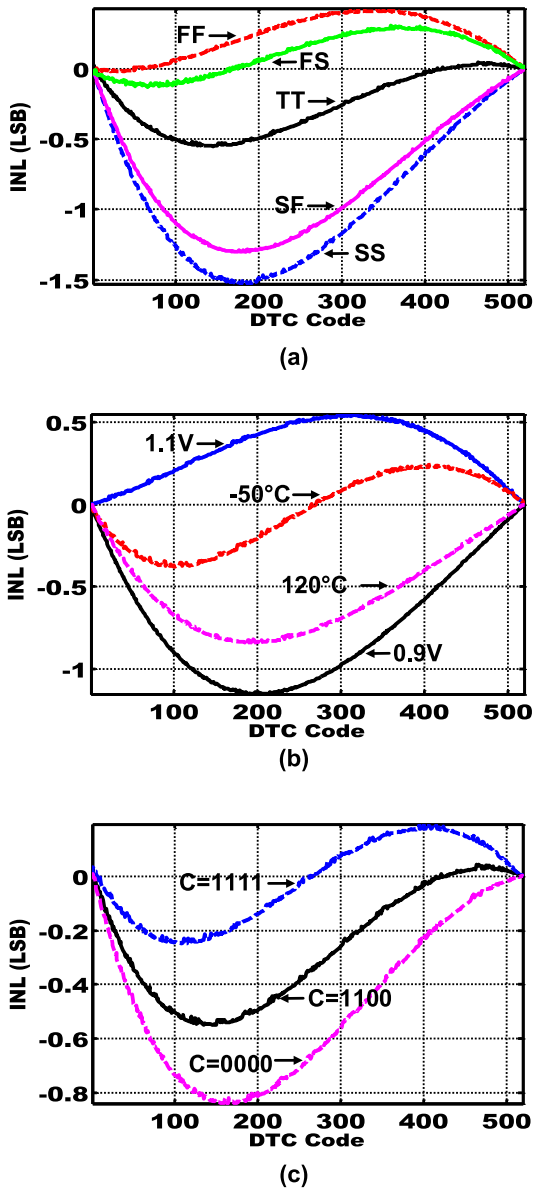

Fig. 5. Simulated INL characteristics of the DTC core including parasitic capacitances with an ideal DAC at (a) different corners, (b) temperature and supply variations, and (c) different calibration codes.

A. Proposed DTC Architecture

The schematic of the proposed constant-slope discharging DTC is shown in Fig. 6. It consists of the input and output buffers, a ramp generator, and a threshold comparator. The transmission gate, fixed capacitor C_0, and controllable capacitor array C_a are used to regulate the supply voltage of the ramp generator. The output of the ramp generator drives the threshold comparator to generate the time delay Δt_d proportional to the initial voltage drop $\Delta V_{\rm DD}$. Four identical loading MOS capacitors are added at the ramp node controlled by $C\langle 3:0\rangle$ to explore the calibration possibility.

The supply regulation of the ramp generator is carried out in two phases: pre-charging φ_1 and discharging φ_2, as shown in Fig. 7. During φ_1, the transmission gate is transparent and the shaded part of the C_a capacitor array (corresponding to C_2 in Fig. 9) is disabled by keeping the zero voltage across

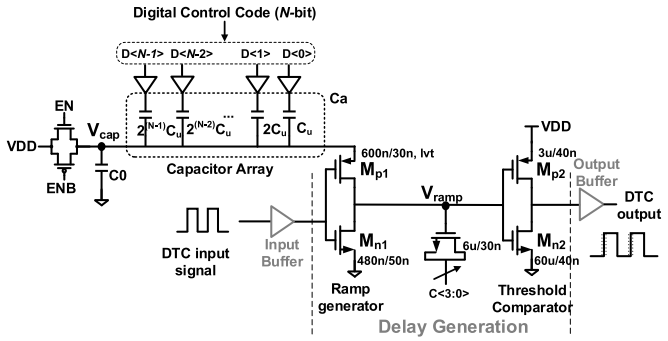

Fig. 6. Schematic of the proposed constant-slope discharging DTC.

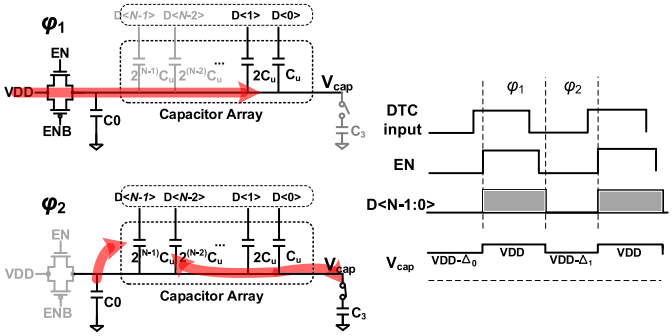

Fig. 7. Illustration of charging and discharging processes of the programmable C-DAC.

the constituting capacitors, as shown in Fig. 9. The fixed capacitor C_0 and the remaining (un-shaded) capacitor array (corresponding to C_1 in Fig. 9) are precharged to $V_{\rm DD}$. During the φ_2 discharge phase, the transmission gate is opaque and all the capacitor arrays gets engaged together with the $V_{\rm ramp}$ node capacitance C_3. The charge is thus shared with the newly engaged capacitors. This produces a regulated voltage drop on $V_{\rm cap}$. Referring to Figs. 6 and 9, $V_{\rm cap}$ is expressed as

$$V_{\rm cap} = \frac{C_1}{C_1 + C_2 + C_3} V_{\rm DD} \tag{2}$$

where $C_1 = C_0 + \sum_{i=0}^{N-1} D\langle i\rangle 2^i C_u$ and $C_2 = \sum_{i=0}^{N-1} (1 - D\langle i\rangle) 2^i C_u$. The total capacitance $C_1 + C_2 + C_3$ is kept constant. When C_1 is linearly increased with the digital control code, C_2 will be linearly decreased by the same amount. As an example, a 900-fF capacitance is first pre-charged to 1 V. Then, the charge is shared with the total 1000-fF capacitance, making $V_{\rm cap}$ settled at 0.9 V. The supply voltage for the ramp generator discharging becomes $V_{\rm DD} - \Delta_k$, which is the start voltage ($V_{\rm st\_proposed}$) in Fig. 1(b).

B. Timing Strategy

A detailed timing diagram is shown in Fig. 8. The DTC input rising (i.e., significant) edge is the critical edge to be precisely delayed. Compared with the conventional DTCs [4], [5], there is one extra control signal here whose timing should be taken care of, i.e., the control signal EN for the transmission gate. Since it affects the next cycle operation, together with the DTC delay control word, $D\langle N-1:0\rangle$, the rising edge of the EN should come safely *after* the rising edge

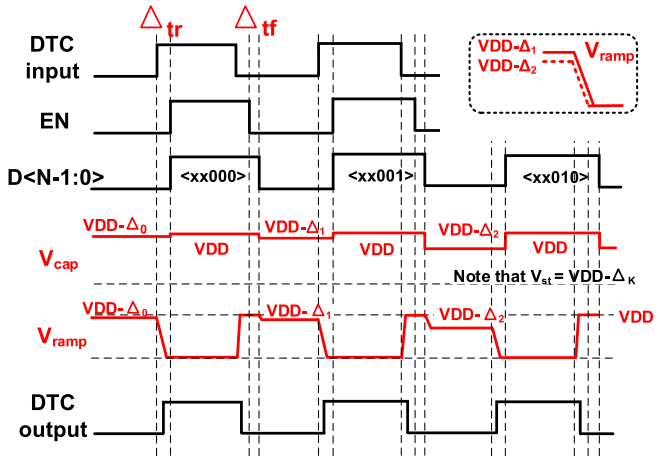

Fig. 8. Timing diagram of the proposed constant-slope DTC using charge redistribution.

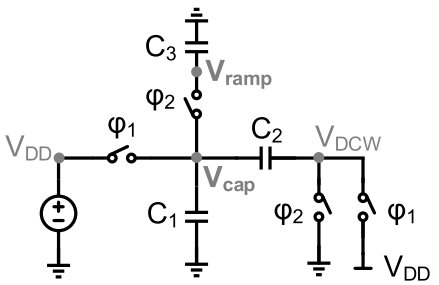

Fig. 9. Abstract diagram of charge redistribution mechanism.

of the DTC input. $\Delta_{\rm tr}$ is the time to allow the ramp inverter output ($V_{\rm ramp}$) to discharge to ground and well settle there. This way, EN and $D\langle N-1{:}0\rangle$ will not affect the previous DTC input rising edge propagation. After the transmission gate is enabled, DTC enters into φ_1. $V_{\rm cap}$ is preset to $V_{\rm DD}$ in preparation for φ_2. $\Delta_{\rm tf}$ represents the time difference between the nearby falling edge of EN and $D\langle N-1{:}0\rangle$. This ensures that the transmission gate will be turned off completely. The charge stored on the capacitor array is still $(C_0+kC_u)V_{\rm DD}$, where C_0 is a fixed capacitance, C_u is the unit capacitance of C-DAC, and k represents the number of chosen charging units in the capacitor array. After $D\langle N-1{:}0\rangle$ is reset to zero, the stored charge is shared over $C_1+C_2+C_3$, resulting in $V_{\rm cap}$ going to $V_{\rm DD}-\Delta_K$. When the next DTC input arrives, $V_{\rm ramp}$ discharges from $V_{\rm DD}-\Delta_K$ to ground. Thus, by different initial discharging ramp voltages, the DTC output rising edge is programmably delayed. More control bits selected result in less capacitors engaged in storing the charge. Consequently, a larger voltage drop $V_{\rm ramp}$ node will ensue, giving less discharging time. Finally, this causes the input signal to propagate faster to the output.

C. Power Advantages With Abstract Diagram

As shown in Fig. 2(a), I-DAC continues to charge the ramp node even after the voltage is settled, thus burning power on the resistor. In contrast, the proposed C-DAC stores the charge on the ramp node after the voltages settles to $V_{\rm st}$, with no more charge drawn from the supply. This is because M_{n1} is disabled before the arrival of the critical input rising edge, thus preventing the charge on $V_{\rm cap}$ to go to ground. This helps to improve the energy efficiency.

The proposed C-DAC does not inherently dissipate any charge, since $V_{\rm cap}$ achieves the desired voltage by charge sharing and there is no path to ground for the $V_{\rm cap}$ node. By taking advantage of the charge redistribution, the variable start voltage generation can be realized with much less power than that in the conventional I-DAC. Fig. 9 shows a simplified abstract model of the charge redistribution used in the proposed DTC. During φ_1, C_1 is charged to $V_{\rm DD}$, accumulating an overall charge of $C_1V_{\rm DD}$, while the charge on C_2 is zero due to its both nodes being at the same voltage potential. During φ_2, the right-hand side electrode of C_2, which is denoted as $V_{\rm DCW}$, gets grounded. The $V_{\rm ramp}$ node capacitance gets also shorted to $V_{\rm cap}$. The charge originally stored on C_1 is hence redistributed over $C_1+C_2+C_3$, reducing C_1's voltage from $V_{\rm DD}$ to $C_1\ V_{\rm DD}/(C_1+C_2+C_3)$. Even though the charge is conserved, the energy loss due to the charge redistribution during the φ_1 to φ_2 transition is $C_1(C_2+C_3)/(C_1+C_2+C_3)\cdot V_{\rm DD}^2$. Then, from φ_2 to the next cycle of φ_1, the power supply needs to fuel up that energy loss. Thus, the energy loss of the entire operation period is obtained as $C_1(C_2+C_3)/(C_1+C_2+C_3)\cdot V_{\rm DD}^2$. The energy loss can be small when C_1 is much larger than C_2 and C_3. Even though the voltage variation on C_2 and C_3 can be as large as $V_{\rm DD}$ or close to $V_{\rm DD}$, their capacitances are relatively small. C_1 is large, while its voltage variation is small. Hence, the power consumption caused by this passive network of three capacitors could be very low.

Referring back to Fig. 4, the $V_{\rm cap}$ node features a slow discharging slope, forcing the threshold comparator to stay in the feedthrough status for a long time. Thus, longer channel length can be selected for it to bring the power consumption down.

As a last remark, there is no need for extra-large buffers to drive the DTC input signal, as compared with the conventional ramp generator [19]. Consequently, the power consumption can be further reduced.

D. C-DAC-Based Ramp Generator

The size of the transmission gate should be carefully chosen to minimize its on-resistance and to reduce the $V_{\rm cap}$ settling time so that it does not limit the operating speed of the DTC. The capacitor array implementation should take into account its power efficiency, matching accuracy, and noise suppression. The digital control word drivers should be strong enough to keep the settling time within half clock period, satisfying the timing conditions in Fig. 8. In this article, a custom-designed MOM capacitor [21] is used, as shown in Fig. 10. The unit capacitance is laid out using metal-2 (M2) to M7 with 0.05-μm width and 1.4-μm length. The layout extraction estimates a unit capacitance of 0.84 fF. It is chosen to guarantee that the quantization noise is buried under the thermal noise level. Only M5 is used to connect the capacitor and the control bits. The distance from the control bits to the custom-designed capacitor fingers is enlarged to reduce the unwanted parasitics.

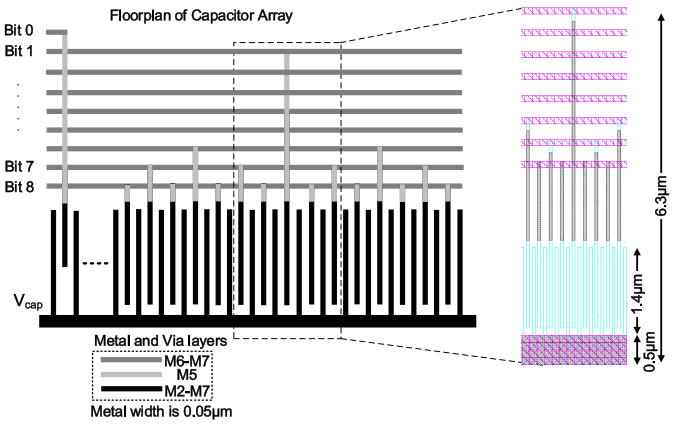

Fig. 10. Layout fragment of the capacitor array.

The LSB is implemented with half of the length of one unit finger to reduce the area. The fixed capacitor (C_0) is built as an MOM capacitor from the PDK and has a value of 2.26 pF. The capacitors occupy the majority of core area. The voltage variation range for V_{cap} is from the minimum initial voltage ($V_{\text{st,min}}$) to V_{DD}, where $V_{\text{st,min}}$ can be determined as

$$V_{\text{st,min}} = \frac{C_0 V_{\text{DD}}}{C_a + C_0 + C_3}. \tag{3}$$

With the implemented capacitor array, $V_{\text{st,min}}$ is 820 mV. In the layout, M1 and M2 are not used in C_0 in order to reduce the substrate interference. The ramp inverter size should not be overly large in order to prevent its self-parasitic capacitance from being too large. The avoidance of the cascode structure in the ramp inverter, as previously done in Fig. 2, is instrumental in substantially lowering the supply voltage in the proposed DTC. In addition, a guard ring is used for noise isolation.

E. Threshold Comparator

The threshold comparator serves two roles: providing the loading capacitance as well as the predistortion for the channel-length modulation. As mentioned in Section II-A, the discharging slope is I/C. After the node V_{ramp} discharges below $V_{\text{st,min}}$, the discharging curves under different DTC control codes are the same, therefore experiencing the same effects. Thus, when deciding on I/C, only the part above $V_{\text{st,min}}$ needs to be considered. In order to ensure that the initial ramp voltage stays sufficiently away from the comparator's threshold voltage, its NMOS transistor is sized larger than the PMOS. This resulted in substantial lowering of the comparator's threshold. When the drain voltage of M_{n1} in the ramp generator drops from V_{DD} to $V_{\text{st,min}}$, it still operates in the saturation region. Then, the discharged current linearly increases with the drain voltage scaled by the factor of λ_I following the conventional I–V formula in (1). As a result, to keep the slope I/C constant, the loading capacitance must decrease as V_{ramp} decreases from V_{DD} to $V_{\text{st,min}}$.

The size of the comparator is large and is optimized to slow down the input ramp and to cover the desired dynamic range. Thus, the node capacitance of V_{ramp} is mainly determined by the gate capacitance of the comparator rather than the drain capacitance of ramp generator, even though the latter can still contribute a small amount of nonlinearities. Considering that the gate voltage of the comparator (inverter) is still high even when it drops to $V_{\text{st,min}}$, then M_{p2} is OFF and M_{n2} is ON. Hence, the comparator output node voltage stays low. Under these conditions, sweeping the gate from $V_{\text{st,min}}$ to V_{DD} causes the NMOS gate capacitance to increase much faster than that of the PMOS. By properly sizing the PMOS versus NMOS, the slope due to capacitance variation can approach the slope due to channel-length modulation. Fig. 11 shows the circuit simulation results of capacitance at the V_{ramp} node against its voltage. Even though this C–V curve is not very linear, this nonlinearity has a weak effect on the DTC delay nonlinearity, as explained in the following. After the V_{ramp}-node capacitance manages to track the channel-length modulation effect, the ramp capacitance can be written as

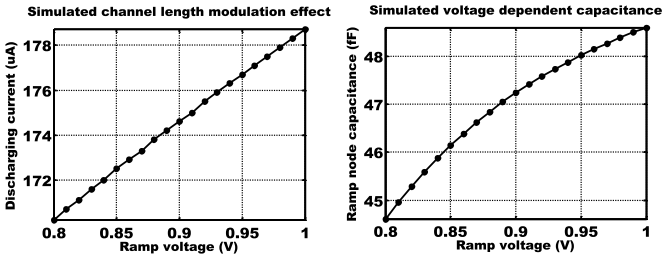

Fig. 11. Schematic simulation results of channel-length modulation effect and voltage-dependent capacitance of V_{ramp} node.

$$C = C_0(1 + \lambda_C V) + f_n(V) \tag{4}$$

where $f_n(V)$ models the nonlinearity of the V_{ramp}-node C–V relationship

$$\begin{aligned} \Delta t &= \Delta V/(I/C) \\ &= \frac{\Delta V}{I_0(1+\lambda_I V)/(C_0(1+\lambda_C V) + f_n(V))} \\ &= \frac{\Delta V}{I_0/C_0}\left(1 + \frac{f_n(V)}{C_0(1+\lambda_C V)}\right). \end{aligned} \tag{5}$$

It can be observed that $f_n(V)$ needs to be scaled by C_0 before affecting the delay nonlinearity. The large size of the comparator not only makes the ratio more robust but also provides strong driving ability to the following output buffer. It can be roughly calculated that λ for the current and capacitance is $\lambda_I = 0.25\ \text{V}^{-1}$ [see (1)] and $\lambda_C = 0.45\ \text{V}^{-1}$ [see (4)], respectively. However, considering that fixed parasitics will be added to the capacitance at post-layout simulations, the latter λ approaches to the former until they are first-order-compensated properly.

IV. Experimental Results

To demonstrate the effectiveness of the proposed techniques, a brand new constant-slope DTC is implemented in a 28-nm low power (LP) CMOS. Fig. 12 shows the chip micrograph. The effective DTC area is 0.0019 mm^2. When operating at a 1-V supply, it consumes only 31 μW while clocking at 40 MHz.

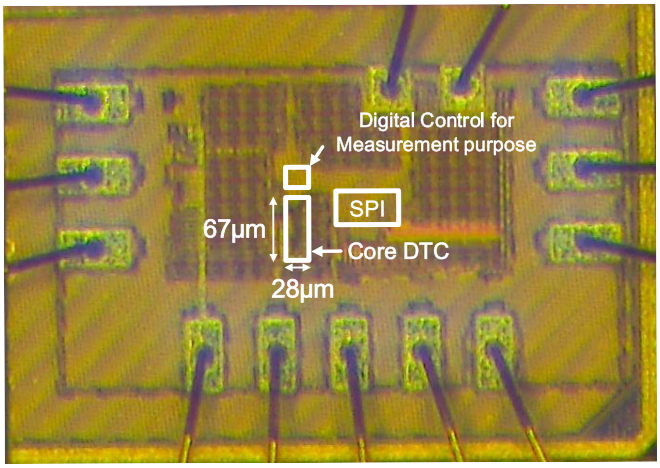

Fig. 12. Die photograph of the proposed DTC.

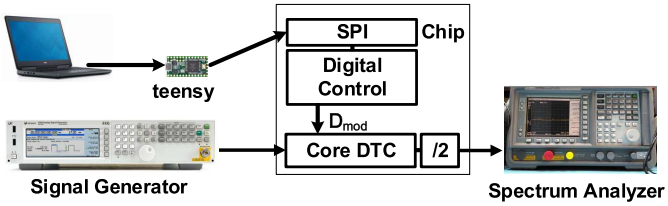

Fig. 13. Measurement setup.

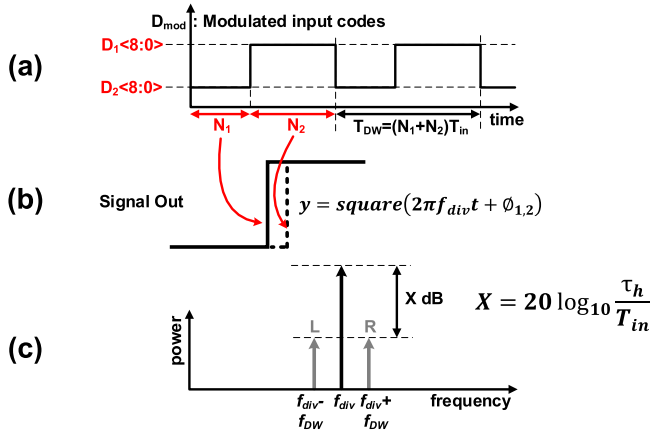

Fig. 14. DTC delay measurement via phase modulation method. (a) Input modulating codes, $D1$ and $D2$. (b) Corresponding modulated output delays in time domain. (c) Spectrum of modulated delays.

The measurement setup is shown in Fig. 13. To measure the DTC nonlinearity,[1] a sensitive frequency-domain method is adopted from [25], as shown in Fig. 14(c). A digital control block is embedded to generate alternating codes $D1$ and $D2$ to periodically modulate the DTC delay. Φ_1 and Φ_2 are the corresponding DTC output phases. The spurious tone level then corresponds to the delay difference between the two corresponding control codes. Similar to the method in [25], the DTC output is divided by 2, yielding a 20-MHz square wave as the output. The spectrum is measured using Agilent E4405B ESA-E. The relation between the spur

[1]In this context, DNL/INL are defined as DNL $= |A_{i+1} - A_i|/A_{\mathrm{LSB}} - 1$, INL $= (A_{i,\mathrm{real}} - A_{i,\mathrm{ideal}})/A_{\mathrm{LSB}}$, where A_{LSB} is a positive LSB.

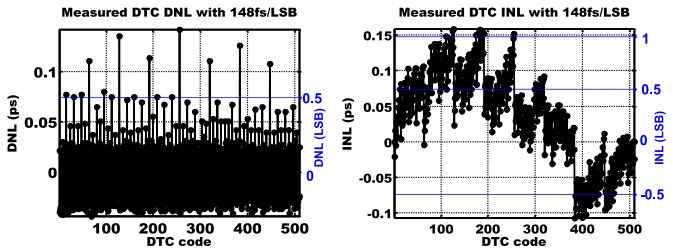

Fig. 15. Measurement results of DNL/INL.

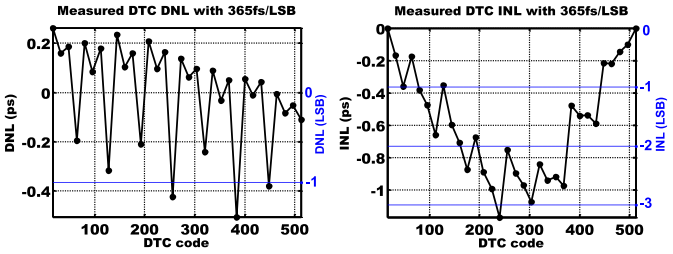

Fig. 16. Nonlinearity under 0.75-V supply voltage.

level and the relative time step can be expressed as

$$\mathrm{spur_h}(f_{\mathrm{div}} \pm f_{\mathrm{DW}}) = 20\log_{10}\left(\frac{|\tau_h|}{T_{in}}\right)[\mathrm{dBc}] \tag{6}$$

where τ_h is the delay difference between the two corresponding control codes $D1\langle 8{:}0\rangle$ and $D2\langle 8{:}0\rangle$; T_{in} is the period of the DTC input clock; f_{div} is the fundamental frequency of the divided DTC output; and f_{DW} is the frequency of the code waveform. The code waveform is set as eight periods of the input clock. Referring to the fundamental frequency at 20 MHz, the relative spur level at 5-MHz offset is, for example, -105 dBc when the DTC control codes are modulated with a single-LSB step difference, which corresponds to a 141-fs delay step. The measured differential nonlinearity (DNL) and INL are, respectively, 0.96 and 1.07 LSB of the 148-fs step size, as shown in Fig. 15. The DNL is mainly contributed by the MSB switching, originating from the systematic layout parasitics. Moreover, due to the LSB being implemented as half of the unit length as other bits, there is an odd–even pattern in the DNL originating from the process mismatch and parasitics. By avoiding the usage of the cascoding topology, the proposed DTC can operate at a low supply voltage. This was verified at as low as 0.75 V with 16-LSB steps per measurement. These results are shown in Fig. 16. The INL is 3.2 LSB with a full range of 187 ps. Its INL degrades due to voltage-dependent ramp node capacitance dominating the nonlinearity. Since the sizes are optimized with 1-V supply, the degraded INL is within the expectations. Current consumption of the DTC core (all the blocks in Fig. 6) is measured under 1 and 0.75 V. The results are shown in Fig. 17, indicating that the consumed power increases with DCW. The average currents are 22.7 and 16.2 μA, respectively. To help generating Δ_{tf} and Δ_{tf} in Fig. 8, extra buffers are needed. These assistant 3-ns delay buffers for the timing control consume 8.5 and 6.1 μA (post-layout simulations), respectively, running at 40 MHz, which can be further reduced, since their jitter has

TABLE I
PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART DTCS

	ISSCC18 [3] Liu	ISSCC11 [12] Pavlovic	ESSCIRC14 [18] Markulic	JSSC15 [19] Ru	JSSC16 [26] Sievert	VLSI06 [15] Inagaki	ISSCC14 [4] Chillara	**This work**	
Method	Constant slope	Variable slope	Variable slope	Constant slope (I-DAC)	Interpolation	Variable threshold	Buffer-based	Constant slope (C-DAC)	
Technology (nm)	65	65	28	65	28	90	40	28	
Supply (V)	1	1.2	0.9	1.2	1.1	1.0	1.0	1.0	**0.75**
Resolution (fs)	580	241-330	550	189	244	1000	21500	**148**	**365**
Number of bits	10	10	10	10	11	6	6	9	
INL[1] (fs)	870*+ (0.15%)	3000 (1%)	990+ (0.18%)	328+ (0.17%)	1200+ (0.24%)	3200 (5%)	67600* (4.9%)	**159+ (0.21%)**	1170+ (0.63%)
Range (ps)	593	247-338	563	189	500	64	1376	76	187
Power (mW)	0.14@ 52MHz	2.2@ 40MHz	0.5@ 40MHz	0.8+1.0@ 55MHz	19.8@ 2GHz	N/A	0.0137@ 32MHz	**0.031@ 40MHz**	**0.017@ 40MHz**

[1] *End-point, +Best fit straight line.

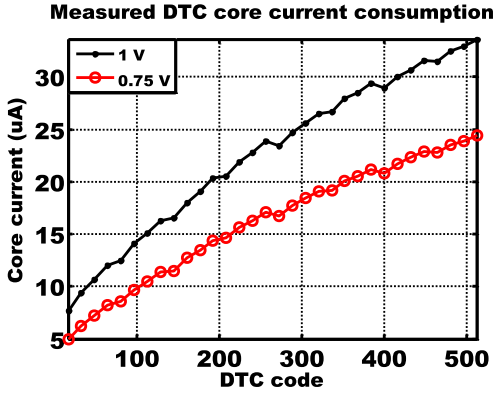

Fig. 17. Current consumption versus DTC control codes with two different voltages.

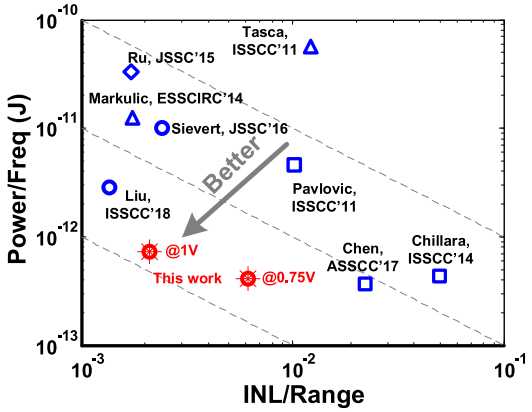

Fig. 18. Performance landscape of the state-of-the-art DTCs.

only a slight influence compared with the 3 ns delay. Thus, the total power consumption of the DTC is 31 μW with the 1-V supply, and 17 μW with 0.75 V.

The measured phase noise of the whole DTC, including the test circuitry, with a 100-MHz sinusoidal input and a 50-MHz square-wave output is −151 dBc/Hz at 100 kHz and −154 dBc/Hz at above 1-MHz offset frequencies. The integrated jitter from 10 kHz to 10 MHz is 267 fs. By incorporating this DTC into an ADPLL, the DTC might contribute some limited amount into the ADPLL's in-band phase noise. Doubling the dissipated power could roughly reduce the jitter power by half. The power consumption of the self-biased buffer is not included in the total power calculation, unlike in [19], which embeds the input driving buffer for testing purpose into the core DTC design. In addition, the input of the proposed compact DTC core is a square wave rather than a sine wave, which is favored by the digital design approach.

The key performance metrics of the proposed DTC are compared in Table I with the state-of-the-art DTCs. It is noted that the constant-slope DTCs can achieve fine resolution and excellent linearity. In this article, the proposed DTC maintains such performance, while consuming significantly less power. Moreover, we should acknowledge that different definitions of INL are chosen in various publications. The endpoint usually gives worse numbers than the best fit straight line method, even though the best fit straight line method is preferred in the ADPLL application, since the DTC offset is normally compensated by the loop.

The DTC performance comparison landscape considering the four key parameters (consumed power, clock frequency, INL, and range) is shown in Fig. 18. The highly accurate matching property of the MOM capacitors in the C-DAC and the constant-slope operation result in a competitive INL/range performance along the horizontal axis. For the vertical axis, which shows the power consumption over clock frequency, this article achieves top performance thanks to the excellent power efficiency of the passive C-DAC, simple ramp generator, and threshold comparator. No additional biasing circuits and current mirror are needed.

The above measurements were done with board #3 and control codes for the loading MOS capacitors C⟨3:0⟩=1100. To check the influence from process and supply variations, and how much influence the trial calibration (four identical MOS varactors controlled by C⟨3:0⟩) can impose, three boards were measured under different control codes of C⟨3:0⟩ and supply voltages. To simplify the DNL/INL measurements, readings were taken every 16 LSBs. The results can be slightly different from the ones taken by 1-LSB step due to the measurement error. The measured resolution and DNL/INL are shown in Figs. 19–21 and summarized in Table II. It can

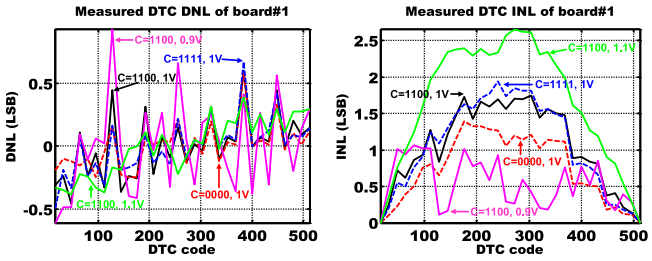

Fig. 19. Measured DNL/INL of board #1.

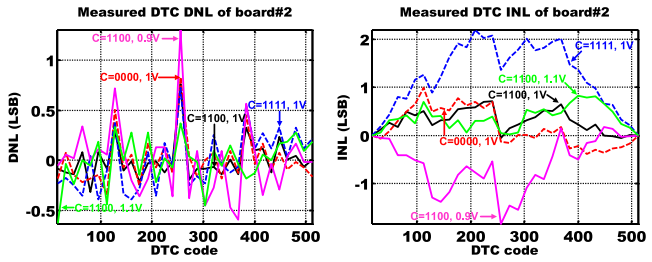

Fig. 20. Measured DNL/INL of board #2.

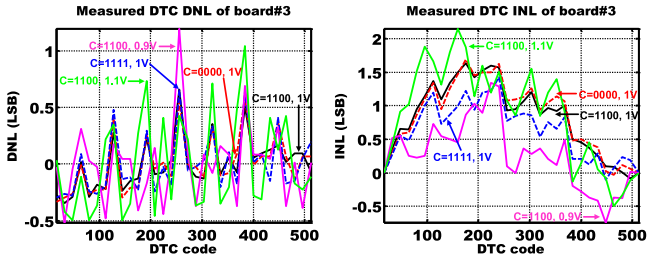

Fig. 21. Measured DNL/INL board #3.

TABLE II
PERFORMANCE SUMMARY OF THREE BOARDS

	'1100' @1 V	'0000' @1 V	'1111' @1 V	'1100' @0.9 V	'1100' @1.1 V
Board#1					
Resolution (fs)	163	170	156	204	140
DNL (LSB)	0.60	0.59	0.67	0.93	0.39
INL (LSB)	1.75	1.39	1.94	1.06	2.66
Board#2					
Resolution (fs)	167	159	177	209	138
DNL (LSB)	0.76	0.73	0.83	1.31	0.54
INL (LSB)	0.71	2.20	0.99	1.84	1.89
Board#3					
Resolution (fs)	153	160	145	189	127
DNL (LSB)	0.66	0.59	0.65	1.20	1.04
INL (LSB)	1.64	1.69	1.42	1.34	2.15

be observed that the voltage variation has a larger influence on INL than the control-code tuning of the MOS capacitors. Comparing between the control codes "1111" and "0000," the significant influence by the tunable MOS capacitance is verified in boards #1 and #2. The INL difference is relatively small in board #3. Comparing the supply voltages between 0.9 and 1.1 V, its influence is verified by all three boards. The INL is more convex at 0.9 V than at 1.1 V. As a conclusion, the calibration can be done either by tuning the supply voltage or by tuning the loading MOS capacitances at the ramp node.

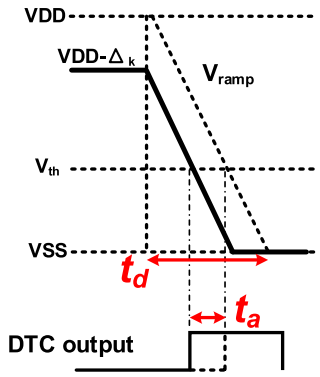

Fig. 22. Linear model of constant-slope discharging voltage ramp.

V. CONCLUSION

In this article, we have proposed a high-resolution, ultra-low-power (ULP) DTC. When operating at 1 V, it achieves 9-bit range with 148-fs step size at 31-μW drained power. Benefiting from the constant-slope operation, the proposed DTC achieves 159-fs INL. It makes use of a simple inverter structure with a built-in predistortion and a passive capacitor array as a DAC generating the initial ramp voltage. The DTC can offer high resolution with good linearity while consuming extremely LP, thus making it suitable for the Internet-of-Things (IoT) applications.

APPENDIX

A. Nonlinearity Versus Range

A larger ratio of the tuning range over the total delay will worsen the nonlinearity, since V_{ramp} node experiences more non-linear distortions. As shown in Fig. 22, for a given slope and total delay t_d, the range t_a can only be increased with a larger voltage drop Δ_k, which obviously worsens the linearity. Under the 1-V supply, a drop to 0.7 V brings much worse linearity than a drop to 0.8 V.

B. Phase-Modulation Measurement Method

As commented in [25], a subset of INL points could also describe the DTC linearity if the INL behavior is fairly smooth. It means that measuring the DNL with 1-LSB steps should result in the same INL as with 16-LSB steps, provided noise is disregarded. However, making the measurements with the finest 1-LSB steps over the 9-bit range will accumulate the measurement error 511 times, adding more uncertainty to the results than with the coarse steps. This is even despite the fact that the spur sensitivity is better with finer steps. The noise can make the spur vary more at larger amplitudes. This requires longer time for averaging, resulting in significant increases in the measurement times.

One scenario that has not been covered in [25] is the case when the DTC transfer function is not monotonic. The DNL/INL calculation cannot directly follow the procedures described in the above publication. As shown in Fig. 23,

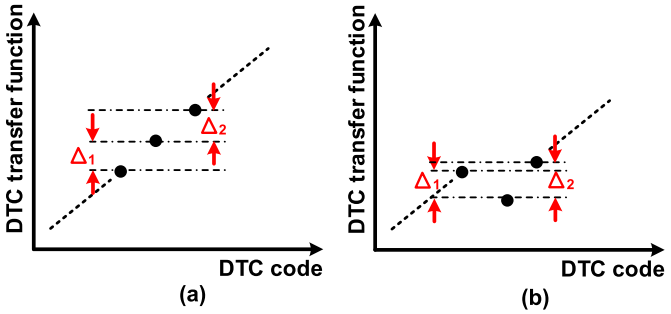

Fig. 23. DTC transfer function (a) with monotonicity, and (b) without monotonicity.

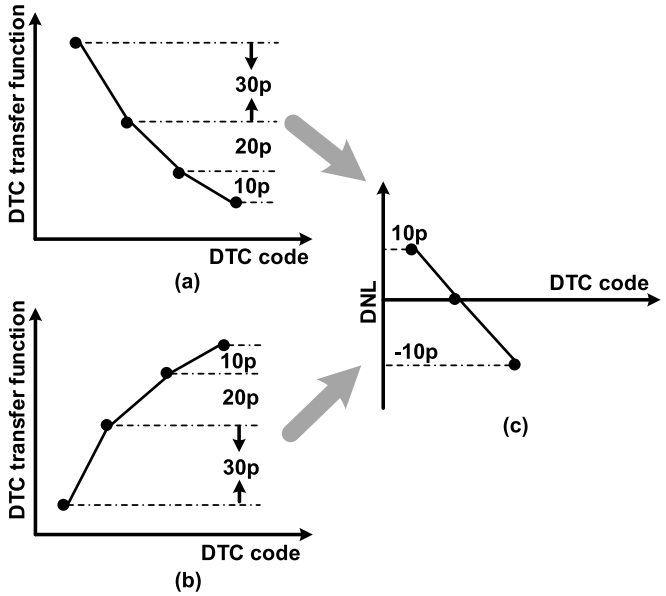

Fig. 24. Different DTC transfer functions can yield the same measured DNL. (a) Descending transfer function. (b) Ascending transfer function. (c) Resulting DNL.

similar results can be derived for two different DTC transfer functions. The DNL calculation should involve with the polarity information. To eliminate such a potential issue, not only 1-LSB steps should be measured across the whole range but also 2 LSB or even more spacing should be confirmed.

Another scenario that should be seriously considered is the INL polarity when transferring DNL into INL. The method described in [25] assumes that the DTC delay increases with the control codes. Fig. 24 shows that two different DTC transfer functions can result in the same measured DNL. When the delay decreases with the control codes, the INL calculated through the conventional way needs to be inverted.

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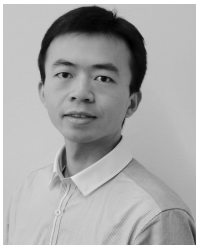

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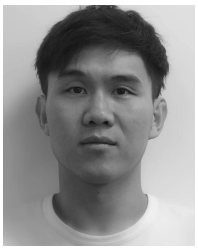

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