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***Abstract*—The Aggressive technology scaling makes modern advanced SRAMs more and more sensitive to soft errors that include single-node upsets (SNUs) and double-node upsets (DNUs). This paper presents a novel Sextuple Cross-Coupled SRAM cell, namely SCCS cell, which can tolerate both SNUs and DNUs. The cell mainly consists of six cross-coupled input-split inverters, constructing a large error-interceptive feedback loop to robustly retain stored values. Since the cell has many redundant storage nodes, the cell achieves the following robustness: (1) the cell can self-recover from all possible SNU; (2) the cell can self-recover from partial DNUs; (3) the cell can avoid the occurrence of other DNUs due to node-separation. Simulation results validate the excellent robustness of the proposed cell. Moreover, compared with the state-of-the-art typical existing hardened cells, the proposed cell achieves an approximate 61% read access time as well as 12% write access time reduction at the costs of 47% power dissipation as well as 44% silicon area on average.**

I. Introduction

It is reported by the *International Technology Roadmap for Semiconductors* (*ITRS*) that CMOS technologies will reach approximate 3nm by 2021 [1], significantly improving the integration and performance of circuits and systems. However, in the advanced nano-scale CMOS technologies, the amount of critical charge stored on a node in a circuit decreases due to the smaller and smaller supply voltages and node capacitances. As a result, the advanced CMOS circuits are becoming more and more susceptive to soft errors induced by the striking of particles, such as protons, neutrons, heavy ions, electrons, muons, and alpha particles [2]. Soft errors can cause potential data corruptions, execution errors, or even crashes to the advanced CMOS circuits. Therefore, it is crucial to work out novel circuit-design techniques to solve the problems on circuit-reliability issues with respect to soft errors.

When a particle strikes an OFF-state transistor in a combinational circuit, the collected charges may cause a transient pulse, i.e., *single event transient* (*SET*), which can be detected at the output of the affected logic gate. If the SET pulse propagates through the downstream combinational logic gates arriving at a storage element, the pulse may be captured causing an invalid value-retention in the storage element [3]. On the other hand, the particle may directly strike an OFF-state transistor in a storage element, causing a *single-node upset* (*SNU*). Moreover, with the aggressive CMOS technology scaling, circuit integration is becoming much higher and node spacing is becoming much smaller. As a result, one striking-particle may simultaneously affect two OFF-state transistors in a storage element due to multiple node charge collection mechanisms [4], causing a *double-node upset* (*DNU*). SNUs and DNUs can cause an invalid value-retention in a storage element which is an important part of the modern advanced circuits and systems. Consequently, to improve the robustness of circuits and systems that are protected against potential data corruptions, execution errors, or even crashes, both SNUs and DNUs are required to consider for reliability designs.

To mitigate SNUs or even DNUs, using *radiation hardening by design* (*RHBD*) techniques, many novel designs of latches [5-7] and flip-flops [8-10] are proposed, while the other designs mainly consider hardening for *static random access memory* (*SRAM*) cells [11-26]. This paper mainly considers hardening for SRAMs. The traditional SRAM memory cell is called 6T since it consists of 6 transistors that include 2 PMOS and 2 NMOS transistors for value-retention and 2 NMOS transistors for access operations. Since the 6T cell cannot tolerate SNUs, many hardened SRAM cells have been proposed for reliability improvement. Typical SNU hardened cells include Quatro [11], NS10T [12], PS10T [12], RHBD10T [15], NASA13T [17], RHD12T [18], We-Quaro [19], Zhang14T [20], QUCCE12T [21], and so on. Typical DNU hardened cells include RHD11 and RHD13 [16], and so on. However, these cells still suffer from some problems such as the following.

(1) To ensure complete SNU tolerance, they have to use extra techniques such as enlarging sizes of some transistors, increasing spacing between nodes, identifying sensitive and insensitive nodes, etc.

(2) They are not effectively DNU hardened. For example, neither RHD11 nor RHD13 can effectively tolerate DNUs, and they even cannot tolerate SNUs. This is because, they use a reliable component (i.e., C-element or Schmitt trigger) to retain values, but the output of the component is fed to its inputs.

(3) They suffer from large overhead especially in terms of read access time. Moreover, some of the cells still suffer from large write access time and power dissipation.

Based on the RHBD technique, this paper presents a novel highly reliable *Sextuple Cross-Coupled SRAM* (*SCCS*) cell with optimized read/write access operations. The storage module of the cell comprises 6 interlocked input-split inverters, and the

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transistors among these inverters are cross-coupled to ensure high reliability. Due to an elaborately constructed error-interceptive large feedback loop, the cell can self-recover from any possible SNU and partial DNU irrespective of the energy of striking-particles. To avoid the occurrence of other DNUs, related nodes are separated for the cell. Moreover, using 6 parallel access-transistors, the cell can achieve low overhead in terms of read/write access time at the costs of extra indispensable silicon area and power dissipation compared with the state-of-the-art SNU/DNU hardened SRAM cells. Simulation results demonstrate the reliability and optimized access operations for the proposed SRAM cell.

The rest of this paper is organized as follows. Section II describes the schematic and working principles of the proposed SRAM cell. Section III presents the comparison and evaluation results. Section IV concludes the paper.

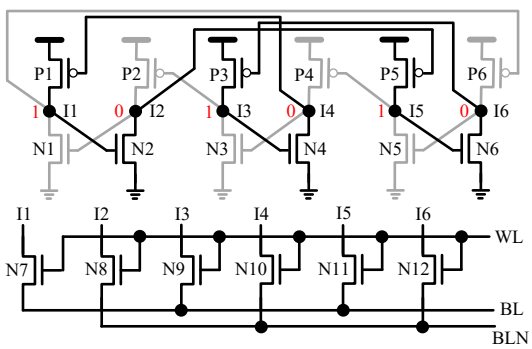

Fig. 1. Schematic of the proposed SCCS cell.

II. Proposed SRAM Cell

A. Schematic and Normal Operations

Fig. 1 shows the schematic of the proposed *Sextuple Cross-Coupled SRAM* (*SCCS*) cell. The SCCS cell comprises 18 transistors, including PMOS transistors P1 to P6 and NMOS transistors N1 to N12. Transistors P1 to P6 and N1 to N6 are used for value-retention. Transistors N7 to N12 are used for access operations and their gates are connected to word-line WL. BL and BLN are bit-lines. I1 to I6 are internal nodes. When WL = 1, the access transistors are ON, allowing write/read access operations to be executed. When WL = 0, the cell retains the stored value.

The normal operations of the proposed SCCS cell are described as follows. Fig. 1 shows the scenario when the cell stores 1, i.e., I1 = I3 = I5 = 1 and I2 = I4 = I6 = 0. First, we consider the case of writing 1. Before the write operation, BL = 1 and BLN = 0. When WL = 1, the operation of writing 1 to the cell is executed. At this time, transistors N1, N3, N5, P2, P4, and P6 are OFF and transistors P1, P3, P5, N2, N4, and N6 are ON. Thus, a large feedback loop (I1 → I2 → I5 → I6 → I3 → I4 → I1) is constructed in the cell. Clearly, the operation of writing 1 is completed and the cell retains the writing value through the feedback loop. Next, we consider the case of reading the stored 1. Before the read operation, the voltages of BL and BLN are raised to that of logic 1. When WL = 1, the operation of reading 1 from the cell is executed. At this time, the voltage of BL does not change. However, the voltage of BLN decreases because of its discharge operation through N8, N10, and N12. Once the differential sense amplifier detects that the voltage difference between BL and BLN is a specified constant value, the read operation is finished and the cell outputs the stored value. For writing/reading 0, the similar scenario can be observed.

Fig. 2 shows the simulation results for normal operations of the proposed SCCS cell. It can be seen from Fig. 2 that a series of write 0, read 0, write 1, and read 1 operations were correctly executed and these wrote values were correctly retained in the proposed cell.

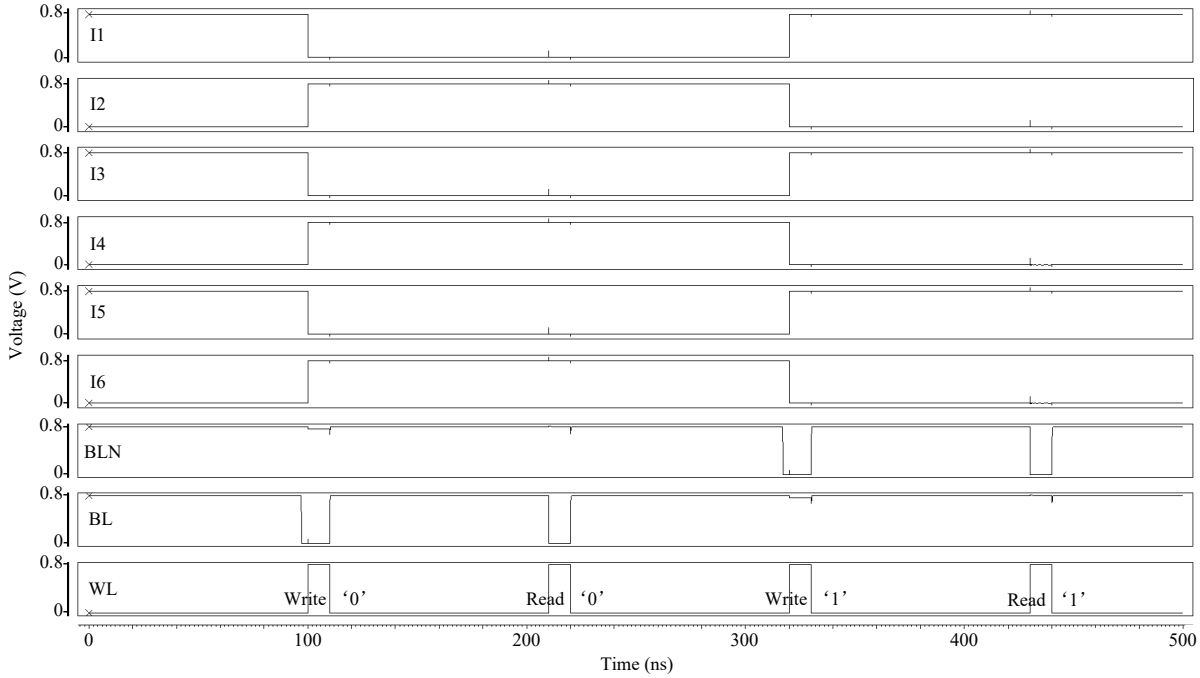

Fig. 2. Simulation results for normal operations of the proposed SCCS cell.

The fault-tolerance principles of the proposed SCCS cell are described as follows. Here, we use the case of 1 being stored (i.e., I1 = I3 = I5 = 1 and I2 = I4 = I6 = 0) for illustration. First, we discuss the SNU self-recovery principles and the key nodes are only I1 and I2 due to the symmetry of the proposed cell.

B. SNU Self-Recovery Principles

We first describe the case where I1 is affected by an SNU, i.e., I1 is temporarily changed to 0 from 1. Obviously, the SNU is intercepted by N2 since N2 becomes OFF. Thus, I2 is not affected (I2 = 0) and P5 is still ON. Since I5 is also not affected (I5 = 1), N6 is still ON and I6 outputs 0 (strong 0). Meanwhile, the fact that I1 temporarily changes to 0 from 1 can cause P6 to be ON temporarily and I6 outputs 1 (weak 1). However, the strong 0 of I6 can neutralize this weak 1, and hence I6 is still correct (I6 = 0). Thus, P3 is still ON (I3 = 1) and N4 is still ON (I4 = 0), allowing P1 to be still ON (I1 = 1). Clearly, I1 can self-recover from the SNU.

Next, we describe the case where I2 is affected by an SNU, i.e., I2 is temporarily changed to 1 from 0. Obviously, the SNU is intercepted by P5 since P5 becomes OFF. Thus, I5 is not affected (I5 = 1) and N6 is still ON (I6 = 0). Meanwhile, the fact that I2 temporarily changes to 1 from 0 can cause N1 to be ON temporarily and I1 outputs a temporary undetermined value especially when the striking-particle has a large energy since the not-affected I4 can allow P1 to be ON. However, at this time, since P6 cannot be ON, I6 still has its correct value (I6 = 0). Thus, P3 is still ON and I3 is also not affected (I3 = 1). Then, N4 is still ON and I4 is also not affected (I4 = 0). Thus, P1 is still ON and I1 outputs 1 (strong 1). However, the strong 1 of I1 can neutralize the temporary-ON-of-N1-induced weak 0 of I1. In other words, I1 can self-recover to its previous value (I1 = 1). Thus, N2 can be still ON, and clearly, I2 can self-recover from the SNU. As for any other single-node, the similar SNU self-recovery principles can be got. In summary, the proposed cell can self-recover from SNUs.

Fig. 3 shows the simulation results for SNU self-recovery on nodes I1 to I6 of the proposed SCCS cell. At 20 ns, 40 ns, and 60 ns, an SNU was respectively injected to nodes I1, I3, and I5. At 360 ns, 380 ns, and 400 ns, an SNU was respectively injected to nodes I2, I4, and I6. It can be seen from Fig. 3 that the proposed cell can self-recover from SNUs.

Next, the cases for DNUs are described. Due to the symmetry of the cell, the node-pairs in any following group are identical.

Group 1: {<I1, I2>, <I3, I4>, and <I5, I6>};
Group 2: {<I2, I3>, <I4, I5>, and <I6, I1>};
Group 3: {<I1, I3>, <I3, I5>, and <I5, I1>};
Group 4: {<I2, I4>, <I4, I6>, and <I6, I2>};
Group 5: {<I1, I4>, <I3, I6>, and <I5, I2>}. Obviously, this group is identical to group {<I2, I5>, <I4, I1>, and <I6, I3>}.

Note that, <I1, I5>, <I1, I6> and their identical node-pairs are also considered in the above pair groups. Thus, the key node-pairs are only <I1, I2 >, <I2, I3>, <I1, I3>, <I2, I4>, and <I1, I4>. The DNU tolerance principles of the proposed cell are described as follows.

C. DNU Tolerance Principles

***Case 1*:** <I1, I2> suffers from a DNU.

In this case, I1 is temporarily changed to 0 from 1 and I2 is temporarily changed to 1 from 0. Thus, P5 becomes temporarily OFF and P6 becomes temporarily ON. However, I5 is not directly affected (I5 = 1). Thus, I6 outputs 0. Meanwhile, the fact that I1 is temporarily changed to 0 can allow P6 to be temporarily ON and I6 outputs 1. As a result, I6 becomes temporarily undetermined and N5 cannot be ON. At this time, I5 = 1 cannot affect P4, I4 = 0 cannot affect N3, and I3 = 1 cannot affect P2. Meanwhile, I4 = 0 can allow P1 to be still ON and I1 outputs 1 (strong 1). As a result, the strong 1 of I1 can neutralize the DNU-induced weak 0 of I1. Thus, I1 is still correct (I1 = 1), P6 becomes OFF, and I6 self-recovers to 0. Meanwhile, N2 can be still ON to output 0 (strong 0). As a result, the strong 0 of I2 can neutralize the DNU-induced weak 1 of I2. Thus, I2 = 0, N1 becomes OFF, and P5 becomes ON. Finally, all nodes and transistors can self-recover to their original states. In other words, <I1, I2> of the proposed cell can self-recover from the DNU.

***Case 2*:** <I2, I3> suffers from a DNU.

In this case, I2 is temporarily changed to 1 from 0 and I3 is temporarily changed to 0 from 1. Thus, P2 becomes temporarily ON. Since I1 = 1 is not directly affected, N2 is still ON. As a result, I2 cannot be determined. However, I2 is temporarily changed to 1 due to the DNU. Thus, N1 becomes temporarily ON. Meanwhile, I4 is not directly affected (I4 = 1). Thus, P1 is still ON. As a result, I1 cannot be determined and P6 cannot be ON. At this time, I6 = 0 cannot affect N5, I5 = 1 cannot affect P4, and I4 = 0 cannot affect N3. However, I6 = 0 can allow P3 to be still ON and I3 outputs 1 (strong 1). As a result, the strong 1 of I3 can neutralize the DNU-induced weak 0 of I3. Thus, I3 is still correct (I3 = 1) and P2 becomes OFF. Meanwhile, I4 = 0 can allow P1 to be still ON, and I1 outputs 1 (strong 1). As a result, the strong 1 of I1 can neutralize the DNU-induced weak 0 of I1. Thus, I1 is still correct (I1 = 1) and N2 becomes still ON to output 0 (strong 0). As a result, the strong 0 of I2 can neutralize the DNU-induced weak 1 of I2. Thus, I2 = 0, N1 becomes OFF, and P5 becomes ON. Finally, all nodes and transistors can self-recover to their original states. In other words, <I2, I3> of the proposed cell can self-recover from the DNU.

***Case 3*:** <I1, I3> suffers from a DNU.

In this case, both I1 and I3 are temporarily changed to 0 from 1. Thus, P2 becomes temporarily ON and N2 becomes temporarily OFF. Then, I2 temporarily outputs 1 and N1 becomes temporarily ON. Since I4 = 0 is not directly affected, P1 is ON. As a result, I1 cannot be determined and P6 cannot be ON. At this time, I6 = 0 cannot affect N5, I5 = 1 cannot affect P4, and I4 = 0 cannot affect N3. However, I6 = 0 can allow P3 to be still ON and I3 outputs 1 (strong 1). As a result, the strong 1 of I3 can neutralize the DNU-induced weak 0 of I3. Thus, I3 is still correct (I3 = 1) and P2 becomes OFF. Meanwhile, I4 = 0 can allow P1 to be still ON and I1 outputs 1 (strong 1). As a result, the strong 1 of I1 can neutralize the DNU-induced weak 0 of I1. Thus, I1 is still correct (I1 = 1) and N2 becomes still ON to output 0 (I2 = 0). Finally, all nodes and transistors can self-recover to their original states. In other words, <I1, I3> of the proposed cell can self-recover from the DNU.

***Case 4*:** <I2, I4> suffers from a DNU.

In this case, both I2 and I4 are changed to 1 from 0. Thus, N1 and N3 become ON and P1 and P5 become OFF. Thus, I1 has to be an invalid value (I1 = 0) and P6 becomes ON. Since I5 = 1 is not directly affected, N6 is still ON. As a result, I6 cannot be determined, making both P3 and N5 become OFF. The fact that both P5 and N5 are OFF can lead to an undetermined value on I5 as time passes. Thus, N6 cannot be ON. Since P6 is ON as mentioned above, I6 has to be an invalid value (I6 = 1) and N5 becomes ON. Meanwhile, since P5 is OFF as mentioned above, I5 has to be an invalid value (I5 = 0). Since N3 is ON and P3 is OFF as mentioned above, I3 has to be an invalid value (I3 = 0). Finally, all nodes and transistors cannot self-recover to their original states. In other words, the proposed cell cannot tolerate the DNU on <I2, I4>. However, the nodes in the pair are not adjacent, and hence the proposed cell can avoid the occurrence of this DNU through the layout technique.

***Case 5*:** <I1, I4> suffers from a DNU.

This case is similar to Case 4, and finally, all nodes and transistors cannot self-recover to their original states. In other words, the proposed cell cannot tolerate the DNU on <I1, I4>. However, the nodes in the pair are not adjacent, and hence the proposed cell can avoid the occurrence of this DNU through the layout technique.

Fig. 4 shows the simulation results for DNUs of the proposed SCCS cell. At 20 ns, 40 ns, and 60 ns, a DNU was respectively injected to node-pairs <I1, I2>, <I2, I3>, and <I2, I4>. At 360 ns and 380 ns, a DNU was respectively injected to node-pairs <I1, I3> and <I1, I4>. It can be seen from Fig. 4 that node pairs <I1, I2>, <I2, I3>, and <I1, I3> of the proposed cell can self-recover from DNUs. Node pairs <I2, I4> and <I1, I4> of the proposed cell cannot self-recover from DNUs. However, the nodes in any of the DNU-not-self-recoverable pairs are not adjacent, and hence the proposed cell can avoid the occurrence of this kind of DNUs through the layout technique. In summary, the proposed cell can tolerate DNUs.

In the above-mentioned fault-injections, a popular and flexible double-exponential current-source model was used. The time constant of the rise and fall of the current pulse was set to be 0.1 and 3 ps, respectively. In all simulations, the Synopsys HSPICE tool was used with the 22nm CMOS library under the room temperature and the supply voltage VDD was set to 0.8V.

III. Comparison and Evaluation

To quantify various overhead of the proposed SCCS cell to make a fair comparison with the state-of-the-art typical SRAM cells described in Section I, the same simulation conditions described in the above section were used for all simulations. Table I shows the reliability and overhead comparison results among the unhardened/hardened SRAM cells in terms of SNU/DNU hardness, *write access time* (*WAT*), *read access time* (*RAT*), average power dissipation (dynamic and static), and silicon area measured with the method in [27].

The reliability comparison is described. It can be seen from Table I that the cells except the 6T are SNU hardened. However, only the proposed SCCS cell can provide a complete SNU self-recoverability from any possible SNU as validated in the above section. For DNUs, only the proposed SCCS cell is DNU hardened. As validated in the above section, the cell can self-recover from partial DNUs and can avoid the occurrence of other DNUs since the nodes in a pair are not adjacent to suffer from a DNU. In other words, the proposed SCCS cell is the most reliable.

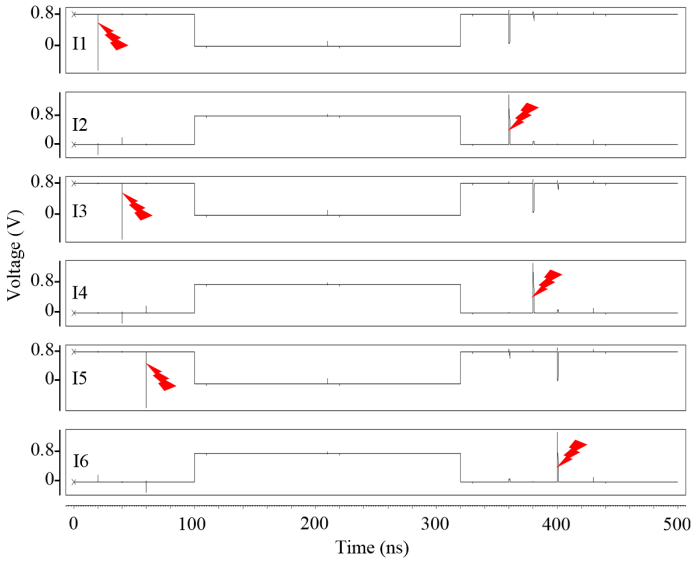

Fig. 3. Simulation results for SNU self-recovery of the proposed SCCS cell.

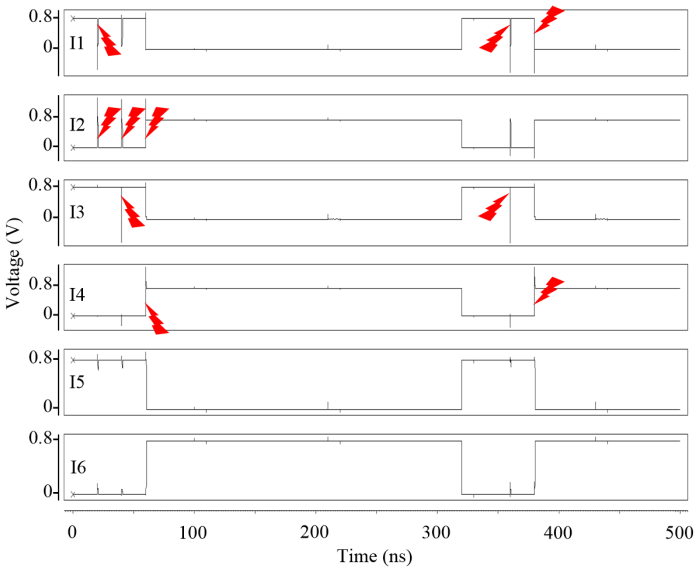

Fig. 4. Simulation results for DNUs of the proposed SCCS cell.

The qualitative overhead comparison is described. For WATs and RATs, it can be seen from Table I that the 6T cell has the smallest WAT. This is mainly because the cell has less current competition when writing a value. However, the NASA13T has the largest WAT due to more current competition when writing a value. It can be seen from Table I that the proposed SCCS cell has a comparable WAT compared with the other hardened cells. However, the proposed SCCS cell has the smallest RAT due to the use of 6 parallel access transistors for reading a value. The NASA13T has the largest RAT due to its special read operation (it has specified extra read transistors). The intrinsic charge/discharge of cell nodes through access transistors can affect WATs and RATs.

TABLE I
RELIABILITY AND OVERHEAD COMPARISON RESULTS AMONG THE UNHARDENED/HARDENED SRAM CELLS.

	6T	NASA13T	RHD12T	We-Quatro	Zhang14T	QUCCE12T	SCCS
Ref.	-	[17]	[18]	[19]	[20]	[21]	Proposed
SNU Hardness	×	√	√	√	√	√	√
DNU Hardness	×	×	×	×	×	×	√
WAT (ps)	3.65	16.39	5.06	4.38	3.80	4.31	4.50
RAT (ps)	25.88	128.67	25.72	12.99	50.66	13.02	8.75
Power (nW)	5.24	18.92	10.38	10.43	7.78	10.43	15.62
10^{-3}×Area (nm^2)	4.35	9.70	8.27	8.71	10.25	8.71	13.07

For power and area, it can be seen from Table I that the 6T cell has the smallest power and area due to the use of a total of only 6 transistors. Generally, a cell having fewer transistors has to use a smaller area and power dissipation; a cell having a larger area has to consume more power. It can be seen from Table I that the proposed SCCS cell has to use extra transistors/area to ensure the self-recoverability from any possible SNU and partial DNU as well as optimized access operations. Thus, the cell has larger power dissipation as well. However, the NASA13T consumes the largest power mainly due to the large current competition in its feedback loops and the use of extra read transistors. The RHD12T, We-Quatro, and QUCCE12T has similar area and power dissipation mainly due to their identical used amount of transistors and similar cell constructions. Therefore, the high reliability and optimized access operations of the proposed SCCS cell are mainly achieved at the costs of extra indispensable silicon area and power dissipation compared with the other hardened SRAM cells.

$$PRC_{WAT}=\frac{WAT_{\text{compared}}(i)-WAT_{\text{proposed}}}{WAT_{\text{compared}}(i)}\times 100\% \quad (1)$$

$$PRC_{WAT}^{\text{average}}=\frac{1}{n}\sum_{i=1}^{n}\frac{WAT_{\text{compared}}(i)-WAT_{\text{proposed}}}{WAT_{\text{compared}}(i)}\times 100\% \quad (2)$$

The quantitative overhead comparison is described. The *percentages of reduced costs* (*PRCs*) of the proposed SCCS cell compared with the other cells were calculated. The PRC of the WAT was calculated with Eq. (1). Similarly, the PRCs of the RAT, power dissipation, and silicon area can be calculated. The average PRCs were calculated with Eq. (2). However, for the brevity of the paper, only the average PRCs are discussed. Compared with the SNU/DNU hardened cells, the average PRCs of the WAT, RAT, power dissipation, and silicon area are 11.61%, 61.47%, -46.67%, and -44.08%, respectively. In other words, the proposed SCCS cell achieves an approximate 12% WAT as well as 61% RAT reduction at the costs of 47% power dissipation as well as 44% silicon area on average.

In summary, the excellent fault-tolerance of the proposed SCCS cell is achieved at the cost of approximate 47% power dissipation and 44% silicon area on average, compared with the existing hardened cells. However, due to the use of 6 parallel access transistors, the access operations of the proposed SCCS cell are optimized to reduce approximate 61% RAT and 12% WAT on average.

IV. CONCLUSION

The aggressive CMOS technology scaling increases the sensitivity of SRAMs to soft errors such as SNUs and DNUs. Based on RHBD, a novel highly reliable SCCS memory cell with optimized access operations at the cost of power dissipation and silicon area has been proposed in this paper. The cell can self-recover from any possible SNU and partial DNUs. For those node-pairs that cannot self-recover from a DNU, they can avoid the DNU sensitivity since the nodes in any of the pairs are not adjacent. The access operations of the proposed SCCS cell are optimized through the use of 6 parallel access transistors. The proposed SCCS cell can be effectively applied to fields, such as aerospace and safety-critical terrestrial applications, where higher reliability is indispensable.

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