A 24 GHz Sub-Harmonically Pumped Resistive Mixer in GaN HEMT Technology

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***Abstract*—This paper presents the design and the characterization of a 24 GHz sub-harmonically pumped resistive mixer (SHM) in an advanced gallium nitride (GaN) high electron mobility transistor (HEMT) technology. The mixer is desired for building up a high-performance phase-locked W-band signal source, and is designed in a single-balanced configuration, where the balanced LO input is generated by an on-chip first order lattice balun. In measurement, a conversion loss around 12 dB is achieved at the RF bandwidth of 22-28 GHz and the IF bandwidth of 3-6 GHz with a LO power of 10 dBm. The mixer exhibits an RF input P1dB of 13 dBm, and the measured LO to IF isolation achieves 40 dB at the desired LO of 10 GHz. To the best of the author's knowledge, this is the first sub-harmonically pumped mixer in GaN HEMT technology.**

Keywords—resistive mixer, GaN HEMT, conversion loss, isolation

I. Introduction

Gallium nitride (GaN) semiconductor technology is well known for its properties of wide bandgap, high heat capacity and good thermal conductivity. Hence, at microwave frequencies, GaN technology is especially attractive for power amplifier applications [1]. In recent years, GaN HEMT also drew increasing attention from low phase noise, in particular far carrier phase noise, oscillator designs, since the devices show a great power handling capability and particularly high break-down voltage [2]. Aiming for a high power and low phase noise signal source at W-band, a desired integration is shown in Fig. 1. The voltage-controlled oscillator (VCO) is designed at the frequency of around 24 GHz and followed by a ×4 frequency multiplier. In order to obtain low phase noise near carrier, the signal will be phase locked to an ultra-low phase noise reference, e.g. a crystal oscillator. Due to the limited choices of commercial phase/frequency detector at the frequency as high as 24 GHz, a SHM is introduced to convert the VCO signal down to 4 GHz, which facilitate the phase-locked loop (PLL) design with increased options of commercial phase/frequency detectors.

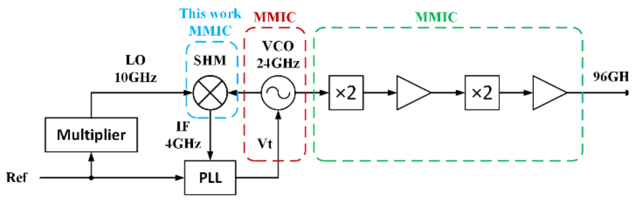

Fig. 1. Block diagram of the desired W-band signal source.

This paper presents the design and characterization of the sub-harmonically pumped resistive mixer part. The circuit was fabricated in OMMIC's advanced GaN HEMT technology (D01GH/D006GH). This process includes both 100 nm and 60 nm devices, which demonstrates cut-off frequencies f_t / f_{max} of 105/180 GHz and 190/250 GHz respectively.

II. Mixer Design

A resistive mixer utilizes the channel resistance, which can be effectively switched by the local oscillator (LO) signal, to achieve the function of mixing [3]. It is featured with good linearity and low DC power consumption at the expense of relatively high LO driving power.

In this work, a single-balanced SHM is chosen instead of a fundamentally pumped resistive mixer, so that the required LO input frequency is reduced to half. Hence, from the system point of view in Fig. 1, the size and DC power consumption of the multiplier at the LO input can be reduced to a large extend. Fig. 2 shows the topology of the designed SHM. T1 and T2 are two identical 100 nm transistors with gate width of 30 µm. The single-ended LO input was converted to the balanced signal and further feed into the gate of the transistor pair. Considering that only narrow band is needed in our application, a first-order lattice balun is designed with lumped elements [4]. Compared to a planar single-layer microwave balun, e.g. Marchand balun [5], the chosen one is more area efficient. According to [4], values of the inductors and capacitors in lattice balun can be calculated as:

$$L_1 = L_2 = \frac{\sqrt{R_S \times R_B}}{2\pi f} \tag{1}$$

$$C_1 = C_2 = \frac{1}{2\pi f \times \sqrt{R_S \times R_B}} \tag{2}$$

where:

- Rs is the unbalanced input resistor, which is usually 50 Ω.
- R_B is the balanced output impedance.

The transistors T1 and T2 are combined in phase at the drain, so that the differential LO leakage will be theoretically cancelled out. The RF input signal is applied to the combined drain node, where the IF output signal is also coupled from. To improve the isolation between the two ports, a third order high pass Chebyshev filter is added at the RF path, while a fifth order low pass Chebyshev filter is included at the IF path. Both filters are implemented with lumped components. As a resistive mixer, the gate of the transistors T_1 and T_2 are biased close to pinch-off for enhanced conversion loss, and the drains

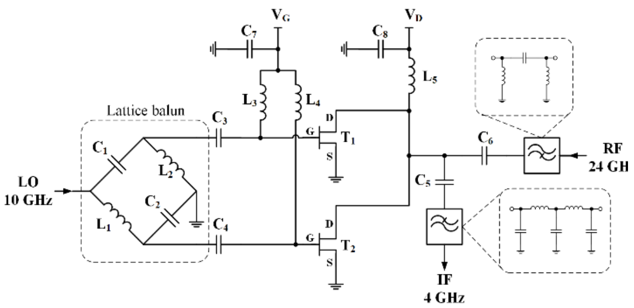

Fig. 2. Topology of the single-balanced SHM.

are biased close to zero. Both gate and drain biases are applied through a big inductor as the RF chock. The circuit is designed and optimized in Keysight's Advanced Design System (ADS) with dedicated design kit from OMMIC. Fig. 3 shows the photograph of the designed SHM, and it occupies an area of 1.7×1.4 μm^2.

III. Measurement

The circuit is measured on-wafer where all ports are connected through probes. The conversion loss of the designed SHM is measured by a 4-port VNA, which has mixer mode enabled. Fig. 4 shows the measurement setup. The LO signal is applied from the port 3 of VNA. The IF and RF ports are connected to port 1 and port 2 of the VNA respectively. Different from a standard S-parameter measurement, the input frequency of VNA is not equal to the output frequency under the mixer measurement mode. Therefore, instead of a direct on-wafer calibration, the setup is calibrated at the coaxial interface, where the SHM together with the IF probe and the

RF probe are treated as the device under test (DUT). Then the conversion loss of the SHM can be obtained from the measured SC12 by de-embedding the probe losses.

At the LO frequency of 10 GHz, the input RF signal is swept from 20 GHz up to 30 GHz, which corresponds to an IF frequency range of 0-10 GHz. The simulated and measured conversion loss is shown in Fig. 5. A typical conversion loss of around 12 dB was obtained at the IF bandwidth of 3-6 GHz. The performance at the lower end of IF frequencies is mainly limited by the on-chip DC blocking capacitor at the IF path, and it can be easily extended by increasing the capacitance or replacing it with an off-chip DC block. In measurement, both gate bias and the drain bias were tuned to obtain the best conversion loss, and the designed circuit shows stable performance with varied bias conditions. Fig. 6 shows the simulated and measured conversion loss as a function of the RF frequency at the IF frequency of 4 GHz and LO power of around 10 dBm. Similar bias conditions were also applied in this measurement. At the gate bias of -1.7V and the drain bias of 0.5 V, a typical conversion loss of 12 dB was obtained at the RF bandwidth of 22-28 GHz.

At the input LO frequency of 10 GHz and RF frequency of 24 GHz, the conversion loss is measured as a function of the LO driving power. As can be seen from Fig. 7, more than 8 dBm LO power is required to drive the designed SHM to work efficiently. Fig. 8 shows the simulated and measured IF output power versus the RF input power. In the measurement, no saturation was observed with an input RF power up to 11 dBm. The measured results agree well with the simulation, an

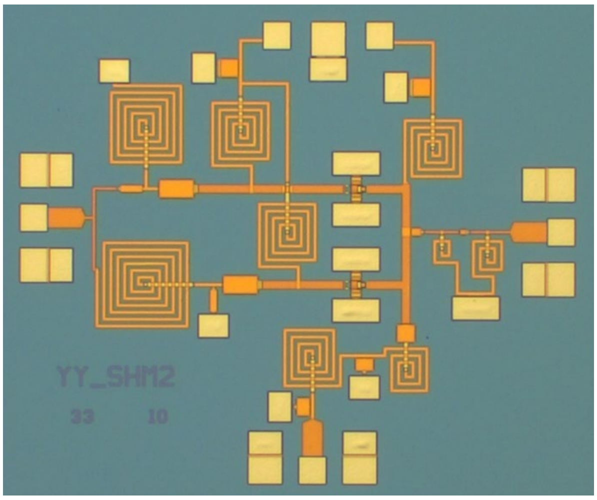

Fig. 3. Photo of the designed SHM:

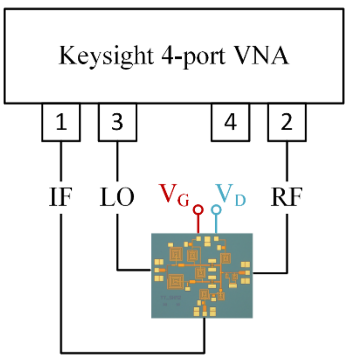

Fig. 4. Measurement setup.

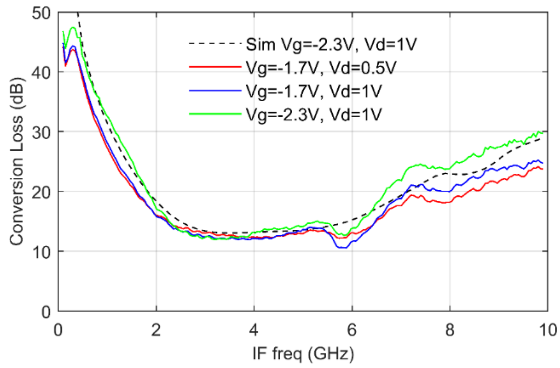

Fig. 5. Simulated and measured conversion loss vs. IF freqeucies as a function of the LO frequency of 10 GHz and LO power of around 10 dBm.

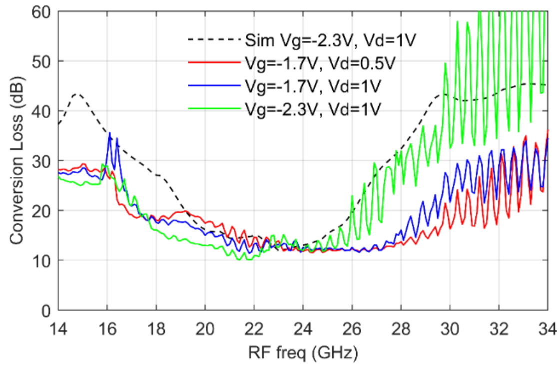

Fig. 6. Simulated and measured conversion loss vs. RF freqeucies at the IF frequency of 4 GHz and LO power of around 10 dBm.

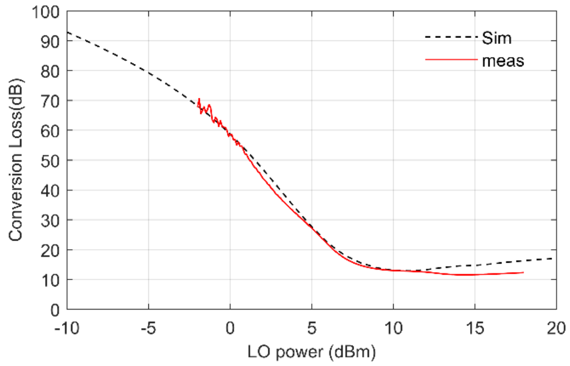

Fig. 7. Simulated and measured conversion loss vs. LO power at the RF freqeucy of 24 GHz and LO frequency of 10 GHz.

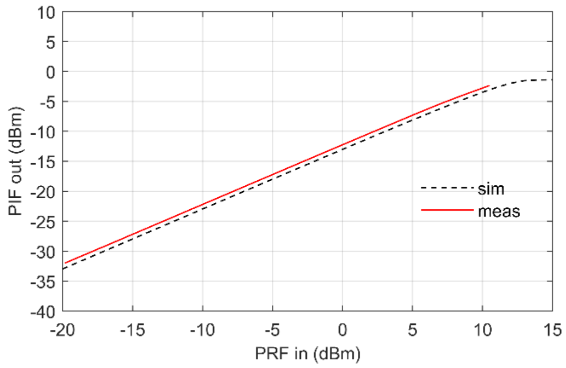

Fig. 8. Simulated and measured IF output power vs. RF input power at the RF frequency of 24 GHz and LO frequency of 10 GHz.

input P1dB of around 13 dBm can be predicted from simulation.

As a down-converter mixer, a strong LO-to-IF leakage may further saturate the IF amplifier in a system. The designed SHM was characterized in a standard 2-port S-parameter measurement, where the LO port was treated as the input and the IF port was considered as the output. The circuit is biased at the same condition as it is designed for SHM, so the isolation can be measured and derived from S21. Fig. 9 shows the measured LO-to-IF isolation, and around 40 dB isolation has been achieved at the desired LO frequency of 10 GHz.

IV. Conclution

Aiming for a further integrated high power and low phase noise phase locked W-band signal source, a 24 GHz sub-harmonically pumped resistive mixer is demonstrated in an advanced 100 nm GaN HEMT technology. The mixer is

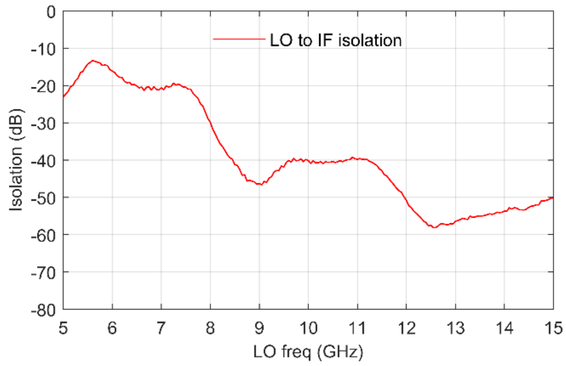

Fig. 9. Measured LO-to-IF isolation.

designed in a single-balanced configuration. A conversion loss on the order of 12 dB was obtained in the RF bandwidth of 22-28 GHz and IF bandwidth of 3-6 GHz. It exhibits good linearity, with an input P1dB of 13 dBm. The measured LO-to-IF isolation achieves 40 dB at the desired LO frequency of 10 GHz.

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