

# An auto-scaling wide dynamic range current to frequency converter for real-time monitoring of signals in neuromorphic systems

Ning Qiao and Giacomo Indiveri Institute of Neuroinformatics, University of Zurich and ETH Zurich  
Zurich, Switzerland  
Email: [qiaoning|giacomo]@ini.uzh.ch

**Abstract**—Neuromorphic systems typically employ current-mode circuits that model neural dynamics and produce output currents that range from few pico-Amperes to hundreds of micro-Amperes. On-line real-time monitoring of the signals produced by these circuits is crucial, for prototyping and debugging purposes, as well as for analyzing and understanding the network dynamics and computational properties. To this end, we propose a compact on-chip auto-scaling Current to Frequency Converter (CFC) for real-time monitoring of analog currents in mixed-signal/analog neuromorphic electronic systems. The proposed CFC is a self-timed asynchronous circuit that has a wide dynamic input range of up to 6 decades, ranging from pico-Amps to micro-Amps, with high current measurement sensitivity. To produce a linear output frequency response, while properly covering the wide dynamic input range, the circuit automatically detects the scale of the input current and adjusts the scale of its output firing rate accordingly. Here we describe the proposed circuit and present experimental results measured from multiple instances of the circuit, implemented using a standard 180 nm CMOS process, and interfaced to silicon neuron and synapse circuits for real-time current monitoring. We demonstrate how the circuit is suitable for measuring neural dynamics by showing the converted response properties of the chip silicon neurons and synapses as they are stimulated by input spikes.

## I. INTRODUCTION

Mixed-signal analog/digital neuromorphic Very Large Scale Integration (VLSI) systems often employ current-mode circuits to emulate the properties of biological neural systems, and to implement their computational principles [1]. By exploiting their transistor's subthreshold region of operation and by interfacing them to asynchronous Address-Event Representation (AER) digital communication modules [2], these analog circuits are suitable for implementing complex and large-scale spiking neural networks in very low-power and compact dedicated VLSI systems [3], [4]. During the system prototyping phases, basic research experiments, and neuromorphic system deployment in practical applications it is very useful and often necessary to perform on-line monitoring of the system's internal nodes and state variables at run-time. While this is something very costly in terms of memory and I/O bandwidth resources with digital neuromorphic systems, it is relatively simple to implement, in mixed signal analog/digital neuromorphic systems. However, this is true only for monitoring the *voltages* of internal nodes, and not currents. For monitoring analog voltage signals it is sufficient to use digital circuits to select the nodes that should be monitored and high precision voltage buffers for

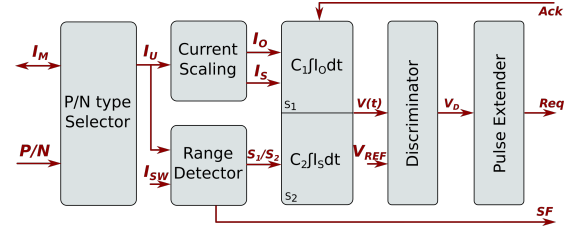


Fig. 1. Block diagram describing the architecture of proposed CFC. The monitored current passes first through a *P/N type Selector* block; its rectified version is then copied to a *Current Scaling* block, while in parallel its value is evaluated by a *Range Detector* block; the scaled current from *Current Scaling* block is then integrated using a capacitor that is selected by the *Range Detector* block output signal; the *Discriminator* and *Pulse Extender* blocks produce Pulse-Frequency-Modulated voltage pulses using the AER protocol, with a rate that is linearly proportional to the integrated current signal.

sending the signals to pads and off-chip. However log-domain current-mode circuits present additional challenges: while it is possible in principle to monitor voltages converted from current-mode circuits using the same buffers, in practice this is not desirable, because the conversion typically involves a compressing logarithmic non-linearity. For this reason it is preferable to monitor directly the currents of such circuits, especially if they represent dynamic variables that emulate biophysically realistic temporal properties of real neural circuits. Existing approaches for monitoring currents are mainly based on precise clocked techniques [5], [6] which are not suitable for continuous time log-domain circuits embedded in asynchronous event-driven systems. In this paper we propose a novel asynchronous auto-scaling Current to Frequency Converter (CFC), based on a low-power programmable current integrator design, that is optimally suited for current-mode neuromorphic circuits, and which linearly converts the monitored current to spike rates, via Pulse Frequency Modulation (PFM).

In the next Section, we describe the circuits that implement the proposed CFC. In Section III we present experimental results obtained from the measurements of test circuits fabricated using a standard 180 nm CMOS process, and in Section IV we present concluding remarks that outline the benefits and potential of the approach proposed.

## II. CURRENT TO FREQUENCY CONVERTER CIRCUIT

Neuromorphic systems that employ current-mode sub-threshold circuits to model neural dynamics usually produce

currents that range from few pico-Amperes to tens of micro-Amperes, with time constants that range from tens to hundreds of milliseconds. To accurately reproduce these signals, the CFC needs to have a wide enough input dynamic range, and a high enough time resolution. Indeed, the CFC circuit should produce spikes at rates that are high enough to allow an accurate reconstruction of the monitored transient current. To convert linearly currents that span six orders of magnitude e.g., ranging from 1 pA to 1  $\mu$ A, using for example output frequencies that range from 10Hz to 10MHz, it would be necessary to allocate a significant amount of resources, in terms of area and power consumption. For this reason, we propose a design that senses the scale of the input current and re-scales it, automatically adapting the output frequency and keeping it within a limited manageable dynamic range. The block diagram of the proposed CFC design is shown in Fig. 1. The circuit consists of a *P/N type Selector* block for rectifying the input current; a *Range Detector* and a *Current Scaling* block for sensing and scaling the rectified current; a *Current Integrator* block which chooses one of two options for integrating the scaled current; and a *Discriminator* block which determines when to trigger an output pulse, whose duration is controlled by the *Pulse Extender* block. The detailed circuit schematics of the CFC circuit are shown in Fig. 2.

The *P/N type selector* circuits rectifies the input current  $I_M$ , via the digitally controlled transistors  $M_3 - M_5$  to produce a current  $I_U$  which is copied by  $M_6-M_8$  to the  $I_O$  current and by  $M_6-M_{10}$  to the  $I_S$  current. Transistors  $M_8, M_{10}$  are sized such that  $I_S = \beta I_O$ , with  $\beta < 1$ . In parallel, the gate voltage of  $M_6$  is compared to a reference voltage  $V_{SW}$ , by the *Range Detector* block. Depending on the outcome of this comparison, two active-low digital signals  $S_1$  and  $S_2$  are generated, which encode either the condition  $I_M < I_{SW}$  or  $I_M > I_{SW}$ , respectively. A third digital output voltage  $SF$  is used to signal to the user the range that is currently being considered. Based on the output of this block, either the current  $I_O$  or  $I_S$  is copied, via  $M_7-M_{13}$  or  $M_9-M_{13}$ , into the *Current Integrator* block. The *Current Integrator* block comprises two integrating capacitors  $C_1$  and  $C_2$  with a ratio  $C_2/C_1 = \alpha$  and  $\alpha > 1$ . The same  $S_1$  and  $S_2$  signals generated by the *Range Detector* block determine which of the two capacitors to use, for the current integration, via the transistors  $M_{16}$  and  $M_{17}$ . Therefore, small currents get integrated with an integration factor of 1, while large currents get integrated with a much smaller integration factor of  $\beta/\alpha$ . To initialize the integrator block it is possible to use the global reset signal  $Rst$ . At the beginning, both plates of the capacitors will be reset to  $V_{refH}$  with  $V(t=0) = V_{refH}$  as initial condition. Once the  $Rst$  is de-asserted, the current through  $M_{13}$  gets integrated on the selected capacitor, and the circuit's output voltage  $V_t$  decreases accordingly. As soon as  $V_t$  reaches the reference voltage  $V_{refL}$ , the output of the *Discriminator* block  $V_D$  will go high, and trigger the  $Req$  to go high as well, for a duration that is set by  $V_{PWLK}$  in the *Pulse Extender* block. The  $Req$  signal is sent to AER interfacing circuits which, after encoding the CFC channel address, transmitting the Address-Event to the off-chip receiver, and receiving the handshaking  $Ack$  signal back, will reset the integrator. The *Pulse Extender* block has

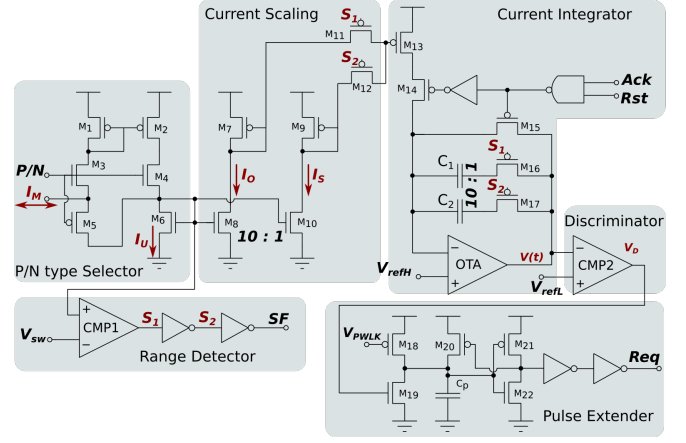


Fig. 2. Circuit schematic of the proposed CFC. The monitored current  $I_M$  is rectified as  $I_U$ , mirrored as  $I_O$ , and scaled down as  $I_S$ . In parallel, the *Range Detector* circuit evaluates  $I_M$  and produces the signals  $S_1$  and  $S_2$  for integrating either  $I_O$  on  $C_1$  or  $I_S$  on  $C_2$  by transistors  $M_{11,12,16,17}$ . The voltage  $V(t)$  gradually decreases during the integration phase, from its initial value  $V_{refH}$ ; once  $V(t)$  reaches  $V_{refL}$ , it triggers a  $Req$  pulse, of extended duration, regulated by the *Pulse Extender* block. The integrator is reset once it receives an acknowledge signal  $Ack$ , from an AER compatible receiver module.

been implemented to make sure that the reset pulse is long enough to fully reset the current integrator.

We can derive the inter-spike interval  $\delta T$  that the CFC circuit described above produces, in response to an input current  $I_{mon}$ :

$$\delta T = \frac{\beta C (V_{refH} - V_{refL})}{\alpha I_{mon}} \quad (1)$$

In our implementation we set the current mirror ratio  $\beta = M_{10}/M_9$  to 10, and the integration capacitor ratio  $\alpha = C_2/C_1$  to 10. So for currents larger than a user-programmable reference value, the total scaling factor is  $\beta/\alpha = 100$ . The reference voltages  $V_{refH}$  and  $V_{refL}$  are also programmable biases, which can be further tuned for selecting a desired output firing rate. For example, if we set  $V_{refH} - V_{refL} = 1V$ , consider capacitors  $C_1 = 100 fF$  and  $C_2 = 1 pF$ , and set the scaling reference threshold such that currents  $I_{mon} < 10 nA$  are not scaled, and  $I_{mon} > 10 nA$  are scaled, then input current ranges from 1 pA to 10 nA will produce output firing rates that range from 10Hz to 100kHz, and current ranges from 10 nA to 1  $\mu$ A will produce output rates from 1kHz to 100kHz. The response of the circuit is linear, provided that the duration of the reset pulse, extended by the *Pulse Extender* block, is negligible with respect to the minimum inter-spike interval produced by the CFC. For the capacitors sizes implemented in our test chip  $C_1 = 100 fF$  and  $C_2 = 1 pF$ , reset pulse lengths of  $T_{RST} = 0.1 \mu s$  are sufficiently smaller than the typical  $\delta T$ s produced.

### III. EXPERIMENTAL RESULTS

We implemented six instances of the CFC circuit described in Fig. 2 in a prototype test chip, fabricated using a standard 180nm CMOS process. The full chip occupies an area of 3.96 mm $\times$ 2.29 mm, and each CFC block occupies an area of 150  $\mu$ m $\times$ 40  $\mu$ m (see Fig. 3 for chip micro-graph). We

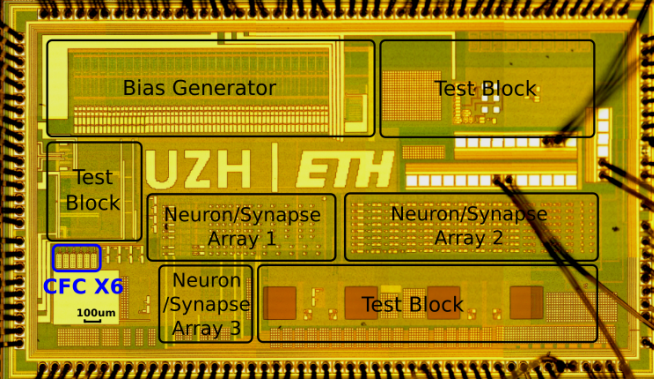


Fig. 3. Die micro-photograph of the test chip with 6 CFC channels (circled in blue) interfaced to different neuromorphic neuron/synapse arrays, for real-time monitoring of neural dynamics.

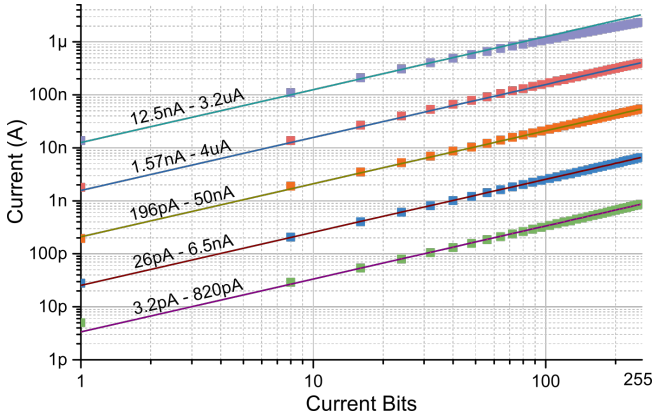


Fig. 4. CFC response (color symbols) to five linear current sweeps (3.2 pA to 820 pA, 26 pA to 6.5 nA, 196 pA to 50 nA, 1.57 nA to 4  $\mu$ A, 12.5 nA to 3.2  $\mu$ A) generated by p-FET transistors biased via an on-chip bias generator (color lines).

interfaced each of the CFC blocks to multiple silicon neuron and synapse arrays for real-time current monitoring. In addition, we connected one of the converters to one p-FET transistor, with its source terminal tied to  $V_{dd}$  and drain terminal connected to the converter's input node. We used an on-chip programmable bias generator [7] to sweep the gate bias voltage of this p-FET transistor and to inject increasing current into the CFC. We programme bias generator to span five different ranges of currents: 3.2 pA to 820 pA; 26 pA to 6.5 nA; 196 pA to 50 nA; 1.57 nA to 4  $\mu$ A; and 12.5 nA to 3.2  $\mu$ A. For each current branch, we swept the input current linearly by appropriately configuring the bias generator digital bits, and calculated the corresponding measured current from the CFC outputs. Figure 4 shows the outcome of these measurements. As shown our circuit can accurately measure currents ranging from approximately 10 pA to 1  $\mu$ A. Currents smaller than 5.5 pA produce no effective output, mainly because of leakage issues in the current mirrors we used to copy current from one block to the next. On the other extreme, currents larger than 1  $\mu$ A lead to distortions, because of the non-linear effects introduced by the finite pulse width of the spikes  $T_{RST}$ , which start to become comparable to the  $\delta T$  values produced by the CFC.

In Fig. 5 we compare the response of the CFC circuit

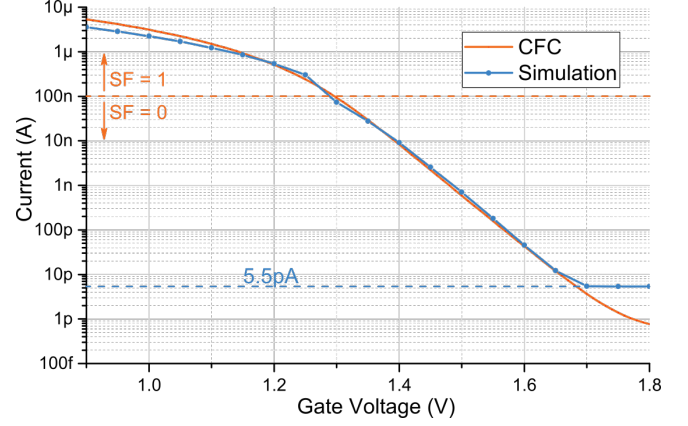


Fig. 5. CFC response to the current produced by a single p-MOS transistor while sweeping its gate voltage (orange line) compared to the transistor's corresponding SPICE simulation output (blue dot line).

to the current produced by a single p-FET transistor while linearly sweeping its gate voltage with the current of that p-FET transistor derived from a corresponding SPICE simulation. As shown, the current derived from the CFC measurements matches the SPICE simulation outcome remarkably well for a wide range of currents, and distorts for currents smaller than 5.5 pA and larger than 1  $\mu$ A. In this experiment, the scaling reference threshold was set to 100 nA.

To provide examples of the dynamic performance of the proposed CFC, we provide measurements of neuromorphic current-mode neuron and synapse circuits [4], as they are being stimulated by input spikes and produce representative synapse and neural dynamics. In Fig. 6 we show the measurements from an Adaptive-Exponential Integrate and Fire (AdExp-I&F) neuron circuit, as it is being stimulated via an excitatory synapse, with an input spike train of 20 Hz. The top plot of Fig. 6 shows the voltage measured from the neuron's integrating capacitor, monitored by a high-gain voltage buffer. Given the current-mode nature of the circuit [4], this voltage actually represents the  $\log()$  of the membrane potential variable. To best measure the dynamics of the variable equivalent to the true membrane potential in this circuit it is necessary to monitor the relevant current, and not voltage. In the second plot of Fig. 6 the current (orange line) is derived from the pulses produced by the CFC (blue pulses); the auto-range detection signal, shown in green, switches shortly after  $t = 600$  ms, due to the large range spanned by the current. To plot the measured current in its full range, we used a semi-log scale (see right axes on figure). In this representation, the measured current resembles very much the measured voltage of the top plot (as expected). On the other hand, in the bottom plot of Fig. 6, we clip the range of the measured current, and plot it on a linear scale, highlighting the neuron's subthreshold dynamics. As shown, it is now evident that the log-domain neuron circuit exhibits an exponentially decaying conductance-based behavior in response to each spike, and a rising exponential dynamics as the current approaches the neuron's firing threshold, faithfully following the behavior of the AdExp-I&F computational model [8].

In Fig. 7 we show measurements taken from a neuromorphic synapse circuit implemented using a log-domain Differential

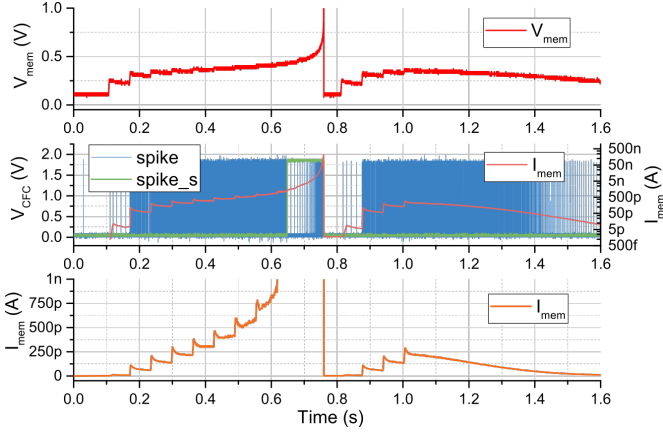


Fig. 6. Neural dynamics in monitored silicon exponential I&F neuron. (Top) neuron's membrane potential from voltage buffer; (Medium) response of CFC and represented membrane current in log-scale; (Bottom) zoom-in view of represented membrane current.

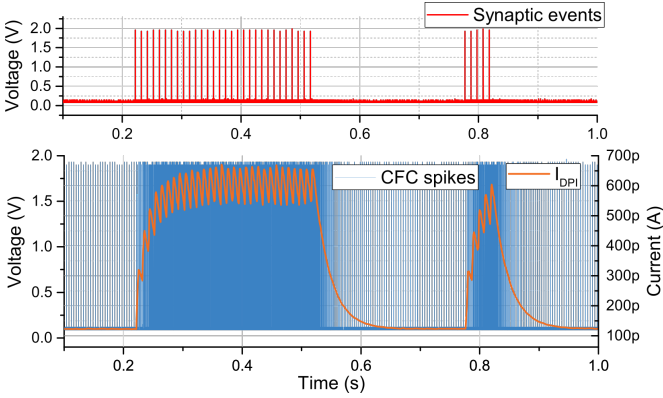


Fig. 7. DPI synapse current dynamics in response to input voltage spikes. (Top) input spike train. (Bottom) derived current measured from the CFC pulses.

Pair Integrator (DPI) circuit [4], in response to input voltage spikes. Using these measurements it is straightforward to derive the synapse model parameters, such as time-constant, and synaptic weight.

The power consumption of this circuit depends on its output rate. Thanks to automatic input range and output rate scaling features, spike rates are kept to low values even for very large input currents. In the worst-case scenario, for an output rate of 100kHz (i.e., the maximum foreseen by this design), the power consumption is approximately 36 nW.

#### IV. CONCLUSIONS

We proposed a novel mixed-signal analog/digital auto-scaling current to frequency converter circuit design for measuring analog currents in neuromorphic electronic systems. The circuit is compact low-power and has a remarkable wide-input range. We validated the design in a 180 nm CMOS process, demonstrated that it has an input dynamic range of up to 6 decades with high current measurement sensitivity, and showed how it is optimally suited for monitoring in real-time the signals produced by log-domain neuromorphic circuits. The compact and low-power nature of this circuit makes it ideal for

being integrated in neuromorphic system that interact with the environment in real-time, and for building closed-loop control and adaptive set-ups accordingly.

#### ACKNOWLEDGMENTS

This work is supported by the EU ERC grant “NeuroP” (257219) and by the EU ICT grant “NeuRAM<sup>3</sup>” (687299).

#### REFERENCES

- [1] C. Mead, “Neuromorphic electronic systems,” *Proceedings of the IEEE*, vol. 78, no. 10, pp. 1629–36, 1990.
- [2] K. Boahen, “Point-to-point connectivity between neuromorphic chips using address-events,” *IEEE Transactions on Circuits and Systems II*, vol. 47, no. 5, pp. 416–34, 2000.
- [3] B. V. Benjamin, P. Gao, E. McQuinn, S. Choudhary, A. R. Chandrasekaran, J. Bussat, R. Alvarez-Icaza, J. Arthur, P. Merolla, and K. Boahen, “Neurogrid: A mixed-analog-digital multichip system for large-scale neural simulations,” *Proceedings of the IEEE*, vol. 102, no. 5, pp. 699–716, 2014.
- [4] E. Chicca, F. Stefanini, C. Bartolozzi, and G. Indiveri, “Neuromorphic electronic circuits for building autonomous cognitive systems,” *Proceedings of the IEEE*, vol. 102, no. 9, pp. 1367–1388, Sep 2014.
- [5] B. Linares-Barranco and T. Serrano-Gotarredona, “On the design and characterization of femtoampere current-mode circuits,” *IEEE Journal of Solid-State Circuits*, vol. 38, no. 8, pp. 1353–1363, August 2003.
- [6] E. Voulgari, M. Noy, F. Anghinolfi, F. Krummenacher, and M. Kayal, “Sub-picoampere, 7-decade current to frequency converter for current sensing,” in *New Circuits and Systems Conference (NEWCAS), 2015 IEEE 13th International*, June 2015, pp. 1–4.
- [7] T. Delbruck, R. Berner, P. Lichtsteiner, and C. Dualibe, “32-bit configurable bias current generator with sub-off-current capability,” in *International Symposium on Circuits and Systems, (ISCAS), 2010*, IEEE. Paris, France: IEEE, 2010, pp. 1647–1650.
- [8] R. Brette and W. Gerstner, “Adaptive exponential integrate-and-fire model as an effective description of neuronal activity,” *Journal of Neurophysiology*, vol. 94, pp. 3637–3642, 2005.