Conference Report: Hierarchical Design Stressed at Design Automation Conference

John P. Gray
California Institute of Technology

Until recently the general attitude of engineers to design automation was confused—they questioned its value yet deplored its limited availability. To increase the amount of DA knowledge in the public domain, the 15th in the series of Annual Design Automation Conferences was held June 19-21 at Caesar's Palace, Las Vegas. Due either to this enlightened choice of venue or to spreading paranoia over handling VLSI designs, this year's conference was extremely well attended—650 delegates, an increase of 50 percent over last year. However, for those expecting to learn of new tools for survival in technologies governed by Moore's Laws, this conference may have been somewhat disappointing. It was largely more of the same—PWB layout, testing, IC layout, design languages, logic design, simulation, CAM, and graphics.

Hierarchical design. Cutting across the traditional lineup of papers, however, was a discernible and increasing emphasis on hierarchical design methods. It was explicit in a number of papers, especially those by Preas and Gwyn and by McWilliams and Widdoes. This interest is encouraging. Hierarchically structuring design—often discussed but seldom practiced—is our only handle on the complexity problems of VLSI. DA professionals ought to be proselytizing design shops or preparing to face the consequences (more brick-bats thrown their way) of conventional systems that run into the acceptable complexity bounds.

SICLOPS program. Preas and Gwyn[1] outlined a method for recursively refining a layout design in a top-down way before proceeding with a bottom-up detailed implementation, using placement and routing procedures. Their approach attempts to automate the true custom-design process, which builds naturally on previous work by allowing modules to be built from standard cell assemblies, macro cells, and general cell assemblies. It also explicitly recognizes the fact that routing, in an environment with a number of cells of various sizes, cannot be contained by fixed channel widths. It will be interesting to see how the method performs on regular structures when a full implementation exists. The paper deservedly shared the best paper award with one by Tokoro et al.,[2] which described a "Module Level Simulation Technique for Systems Composed of LSI and MSI."

Wire-wrap design. A hierarchical design system for a different technology, wire-wrap boards, was described in the papers by Widdoes and McWilliams.[3,4] The system is based on creating hierarchical logic diagrams, using the Stanford University Drawing System (SUDS). The logic diagrams describe macros for standard expansion of components between levels in the design hierarchy. A textual form of the macro definitions is expanded and terminal components bound to physical locations on the wire-wrap board. Finally, optimal wire routes are evaluated.

The authors reported that the system has been used for the top-down design of the S-1 computer with impressively short scales of design time.

Program chairman Rob Smith of the University of Texas at Austin hands over a sack of silver dollars to Brian Preas and Chuck Gwyn of Sandia Laboratories for their paper, "Methods for Hierarchical Automatic Layout of Custom LSI Circuit Masks." They shared the Best Paper Award with Prof. Mario Tokoro (background center) from Keio University, Kokahama, Japan, who presented the paper, "A Module Level Simulation Technique for Systems Composed of LSI's and MSI's," which he coauthored with five of his students. (Photos: Paul Conrow)

0018-9162/78/1000-0066$00.75 © 1978 IEEE

The work also demonstrated the simplifications possible in developing a DA system at a single level of the physical hierarchy. Perhaps it would be too much to hope that this observation would apply to other single-physical-level technologies, like silicon, and that we can look forward to less complex implementations of DA systems. It is also worth noting that the cost of a graphics front end, which is almost always desirable, was highlighted by the gross mismatch in size between the SUDS program and the physical design subsystem.

Cost of DA systems. It has always been difficult to justify the cost of DA systems since the benefits are less tangible than in other areas of manufacturing. In the case explored by Shah and Yan,[5] benefits were identified as increased productivity of manpower and reduced turnaround time for drawing. The general technique presented should be useful in a number of situations—justification of a new DA system, determination of number of work stations, and determination of operating strategy.

Frame stores. The evolution of frame-store based graphics was apparent in the integrated circuit design session. While a number of authors described interactive graphics systems based on frame stores, Weste's paper [6] describing the use of

Unusual terms explained

Complexity. VLSI is currently being fabricated in the range of 10,000 to 40,000 gate equivalents. Continuing decreases in design-rule tolerances and improvements in processes may increase density by an order of magnitude by the mid-80's, greatly increasing the complexity of design—unless countervailing methods are devised.[1]

Cell. The building blocks used by a computer-aided design system to implement an integrated-circuit design are termed cells. The fundamental unit is the *standard* cell. Groups of these cells are interconnected to form a standard cell *assembly*. A still larger unit, the *macro* cell, consists of a custom layout, usually handcrafted, which performs a high-level function. *General* cell assemblies consist of combinations of the foregoing units.[1]

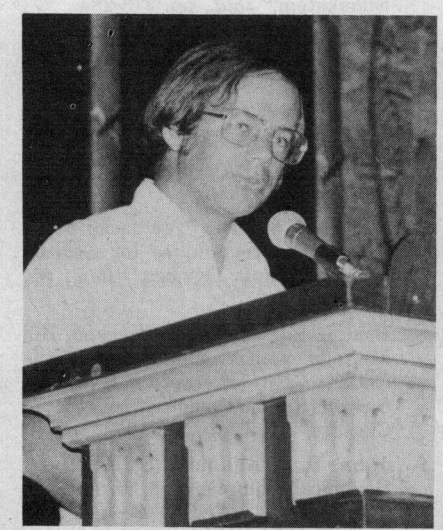
Hierarchical structured design. A large design containing tens of thousands of gate equivalents is decomposed or partitioned into more tractable circuits (or cells) of manageable size. The method may include top-down partitioning and initial layout, followed by bottom-up layout implementation at each hierarchical level.[1]

Moore's law. Gordon Moore, now president of Intel, is credited with forecasting in 1964 that functions per chip would double every year for some time thereafter.

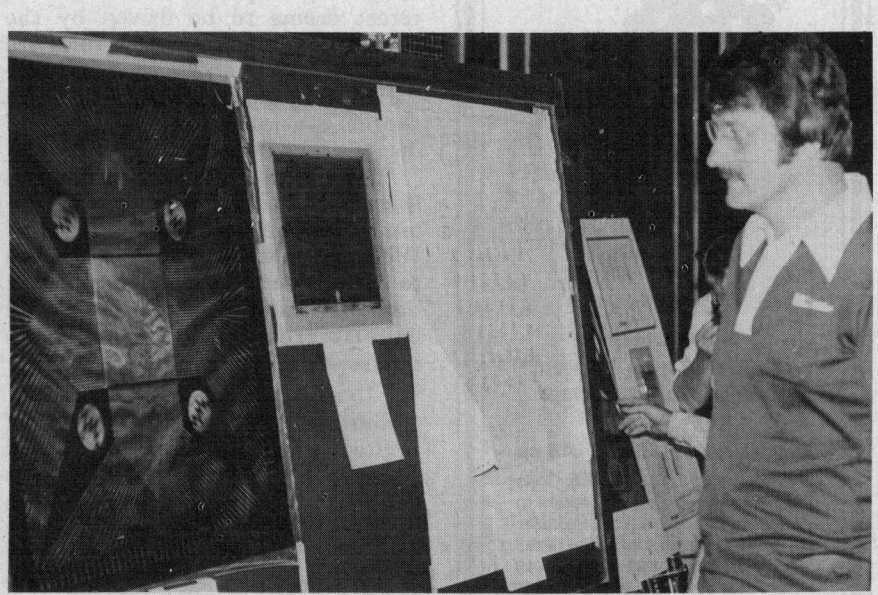
S-1 computer. This high-performance (15 MIPS) processor, composed of 5500 chips ECL-10K was designed and implemented in two man-years with the Structured Computer Aided Logic Design system at Stanford University and Lawrence Livermore Laboratory.[3]

Stick layout. Instead of laying out polygons on several overlapping layers, the designer inputs a "stick" diagram to the computer system. The sticks are single symbols representing the transistors, diodes, contacts (vias), etc., of the design. The sticks are transformed by the computer system into corresponding polygons on several layers according to the design rules in effect.[9]

Symbolic layout. A set of symbols which explicitly define the electrical and logical functions of each transistor, diode, or other device on a chip is manually located on a grid structure. From this input a computer system maps the symbols into polygons, layer by layer, representing the particular device.[7,8]



On the last day of the conference, Dave Hightower of Texas Instruments, as chairman for DAC '79, says, "We'll see you in San Diego on June 25-27, 1979." Steve Szygenda of the University of Texas at Austin chaired this year's conference.



The artwork contest, now two years old, attracted much attention. Here, Bill Kaiser of Bell Laboratories judges one of the entries, which must be generated by design automation programs. "Collection" by Neil Weste, Bell Laboratories, won first prize for technical creativity and "Planar Video Display, 1X Plate and PC Artwork" by Al Carney, Air Force Avionics Laboratory, won for artistic merit.

Digest of Papers:

COMPUTER TECHNOLOGY: STATUS, LIMITS, ALTERNATIVES

February 28–March 3, 1978
(380 pages)

Digest of papers from 30 sessions at COMPCON Spring 78 offers an examination of the present status of the elements of computer technology, an understanding of the limitations of the in-place technologies, and an evaluation of the promise of some of the alternative technologies.

Non-members – $20
Members – $15

Use order form on p. 98.

184: Proceedings,

Conference on Pattern Recognition and Image Processing,

May 31-June 2, 1978 – 516 pp.

Sponsored by the IEEE Computer Society, this conference investigates approaches to flexible and intelligent human interface to pattern and pictorial data. These proceedings consist of over 90 papers covering topics such as medical ultrasound imaging, computed tomography, map data processing, image segmentation and structure, pictorial data bases, and algorithms in pattern classification.

Non-members–$25
Members–$18.75

a frame store within a computational structure pioneered new territory.

There are a number of applications, especially those associated with artwork checking and routing problems, in which the advantages of 2-D representations of the data are clear, provided an adequate interface exists between the frame store and the host computer. Weste's work went as far as retrieving a net list from artwork to drive a transient analysis program. Waters gave details of the application of this type of representation to dimension checking, but did not clarify a compression technique that would stretch the range of use of hardware frame buffers. Unfortunately, this and many other papers were not available before publication, and the proceedings do not fully report all the events of the week.

The primary function of frame stores, to produce color graphics, was also in evidence. In this connection, the color pictures by Weste won first prize for technical merit in the artwork competition organized this year (see "About the Cover," p. 3). A rather abstract rubylith received first prize for artistic merit.

Symbolic layout. The two references to this subject, by Larsen[7] and Infante et al.,[8] did not fully reflect the attendees' strong interest in symbolic layout and its recent successor, "stick" layout, as technology-independent representations. This interest seems to be driven by the rapidity with which design rules are changing. The hope is that, by compiling layouts from symbolic representations, the updating of designs may be simplified.

A special interest group meeting on stick representation was well attended. However, only the work of Williams[9] exists in the open literature to judge the efficiency of the process. Perhaps next year's conference will benefit from this localized enthusiasm.

Routing. The perennial topic of printed circuit board design was well represented by a total of nine papers and a panel discussion, but there was little new material. What was new was attributable to Doreau and Abel[10] who described a topologically based nonminimum distance routing algorithm. In their method the routing problem is transformed into a permutation of nets. The authors claim an acceptable complexity bound for this algorithm when applied to such practical cases as part of a row or column of IC packs on a board. With the current interest in via elimination it is interesting to note that one significant feature of the algorithm is the small number of vias introduced by this routing process.

A combined line search and Lee router was described by Soukup.[11] The presentation involved the use of a large checkered board, colored tokens, and string. The analogy to gaming tables was entirely appropriate to the occasion, which proved to be the latest recorded instance of people losing less money on Lee's algorithm. ■

References

1. B. T. Preas and C. W. Gwyn, "Methods for Hierarchical Automatic Layout of Custom LSI Circuit Masks," *15th Design Automation Conf. Proc.*, June 1978, Las Vegas, Nev., pp. 206-212.
2. M. Tokoro, M. Sato, M. Ishigami, E. Tamura, T. Ishimitsu, and H. Ohara, "A Module Level Simulation Technique for Systems Composed of LSI's and MSI's," *ibid.*, pp. 418-427.
3. Thomas M. McWilliams and Lawrence C. Widdoes, Jr., "SCALD: Structured Computer-Aided Logic Design," *ibid.*, pp. 271-277.
4. ____, "The SCALD Physical Design Subsystem," *ibid.*, pp. 278-284.
5. R. R. Shah and G. Yan, "A Practical Technique for Benefit-Cost Analysis of Computer-Aided Design and Drafting Systems," *ibid.*, pp. 16-22.
6. N. Weste, "A Color Graphics System for IC Mask Design and Analysis," *ibid.*, pp. 199-205.
7. Robert P. Larsen, "Versatile Mask Generation Techniques for Custom Microelectronic Devices." *ibid.*, pp. 193-198.
8. Beatriz Infante, Diane Bracken, Bill McCalla, Sam Yamakoshi, and Ellis Cohen, "An Interactive Graphics System for the Design of Integrated Circuits," *ibid.*, pp. 182-187.
9. John D. Williams, "STICKS—A Graphical Compiler for High Level LSI Design," *AFIPS Conf. Proc.*, Vol. 47, 1978 NCC, pp. 289-295.
10. Michael T. Doreau and Luther C. Abel, "A Topologically Based Non-Minimum Distance Routing Algorithm," *op. cit.*, pp. 92-99.
11. J. Soukup, "Fast Maze Router," *ibid.*, pp. 100-102.