Modeling of MoS2 Tunnel Field Effect Transistor in Verilog-A for VLSI Circuit Design

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Modeling of MoS_2 Tunnel Field Effect Transistor in Verilog-A for VLSI Circuit Design

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***Abstract*—This paper presents the design of an inverter, half adder, and ring oscillator using compact models of MoS_2 channel-based tunnel field effect transistor (TFET). The TFET models (both n and p-type) are written in high-level hardware language Verilog-Analog (Verilog-A) following the analytical model of [1] and the output characteristics of the components are simulated in Cadence/Spectre software. The performance of the designed inverter (a basic building block of VLSI circuit) is analyzed by extracting its different parameters, such as transfer characteristics, power dissipation and consumption, delay, power delay product. The simulated outputs (sum & carry) obtained from the half adder circuit exactly match the truth table of the circuit. Moreover, our observation reveals that the ring oscillator can operate at a higher frequency with lower power consumption in comparison to the existing CMOS and GFET technologies. We have also reported an improvement to the limiting factor of ring oscillator performance i.e. phase noise at two different offset frequencies. With all the output characteristics obtained from the commercial software simulation, we expect our model to be applicable to a real-time low-power VLSI circuit.**

Keywords—TFET, Verilog-A, Cadence, Inverter, Half adder, Ring oscillator

I. INTRODUCTION

Traditional silicon-based transistor technology with its scaling experiences an excessive power loss, drain-induced barrier lowering (DIBL), and quantum tunneling of carriers. These limitations are nearly confronted by the application of band to band tunneling mechanism to ensure sub-threshold swing (SS) below 60mV/decade and two-dimensional materials to establish better electrostatic control of the channel [1-4]. Despite the fascinating electrical and thermal properties, graphene is not suitable to fabricate logic operators due to the absence of bandgap [5]. On the contrary, transition metal di-chalcogenide (TMD) materials possess a scalable bandgap that can generate a high on/off ratio and low static power loss in transistor technology [6, 7]. However, in order to understand the practical application of the transistor, the model should be simulated in a hardware-compatible language. Spice-compatible commercial simulators mainly work on library models like EKV3 or BSIM and are not suitable for the compact modeling of newly designed devices. One way can be Verilog-A coding scheme which has been the *de facto* standard and natural

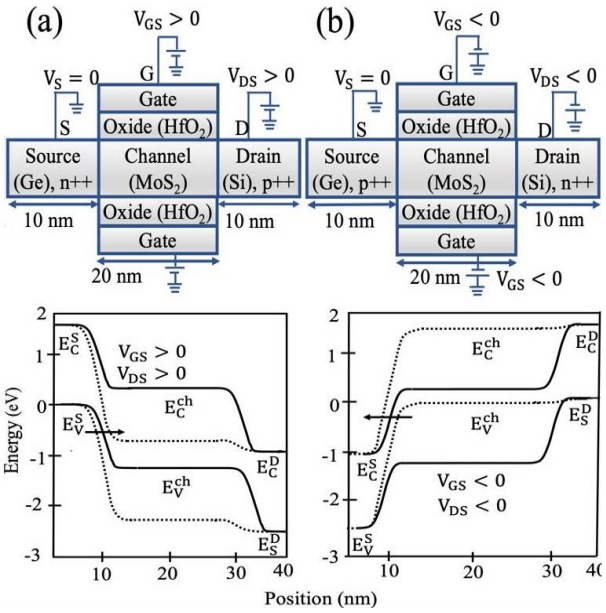

Fig. 1. Schematic diagram and the corresponding band diagrams of (a) n-type TFET, (b) p-type TFET at both off (lines) and on (dotted) state. Arrow direction indicates the direction of carrier flow.

language for defining a compact model since 2004 [8, 9]. It was originally intended for behavioral modeling of both the analog and mixed-signal system design and allows writing the mathematical expressions that describe the physics of any compact model. It is simpler, shorter, and much more convenient than Fortran or C languages, as it automatically generates the simulator interface and the derivatives within the coding scheme. In addition, it does not involve any numerical algorithm and data structure. Spectre works as an electrical simulator in the software package that has been linked to Cadence with the help of a programming interface called compiled model interface. The design of a ring oscillator using compact model nowadays gain popularity due to its advantages in analog circuits such as, high frequency oscillation with low voltage and offers a wide tuning range with fixed or variable frequency [10]. Moreover, the number of inverter stages in the

ring oscillator can be varied to overcome the effects of parasitic capacitances and on-state resistance of the transistor. Nevertheless, to maintain the oscillation, inverters should be uniform to produce input-output signal matching and unit voltage gain.

Several TFET compact models have been reported so far using Verilog-A coding. Biswas *et al.* utilized a compact model of silicon-based TFET to design a ring oscillator, but it showed low operating frequency [11]. Liu *et al.* presented III-V semiconductor-based TFET using lookup table approach in Verilog-A which is not suitable for electronic design automation (EDA) [12]. Fahad *et al.* designed an inverter using a graphene-based TFET model that offers a low on/off current ratio and eventually high static power [13].

In this paper, utilizing a compact model of TFET with MoS_2 channel region, we design a ring oscillator, capable of producing high-frequency oscillation with low power consumption. The underlying reason for this performance is the low SS and high on/off current ratio of the TFET and eventually the fast switching characteristics of the inverter. Moreover, the compatibility of the transistor model in digital circuit is verified by designing a half-adder circuit. We hope that this paper will provide a guideline to design low power electronic circuit components using the newly designed transistor model. The paper starts with a short description of Verilog-A implementation of our transistor model with its I-V characteristics in section II. In section III, the figure of merits of the inverter, obtained from both n and p-type TFET are discussed. Moreover, the output characteristics of the half adder and ring oscillator are presented in section III followed by the conclusion in section IV.

II. Verilog-A Design of TFET

In our previous work, an analytical model of only n-type TFET was outlined whereas in this article, for the sake of inverter design, compact models of both n and p-type are coded in the Verilog-A platform [1]. The model consists of the Landauer formula that includes tunneling probability, mode, and energy levels at three different regions of the transistor. For details about the modeling, the reader can go through [1]. Fig. 1(a) and Fig. 1(b) represent n-type and p-type heterostructure TFETs with their corresponding band structures at applied bias. Both the gate to source voltage (V_{GS}) and drain to source voltage (V_{DS}) were maintained at the positive and negative voltage for n-type and p-type, respectively. Our model has a channel length and width of 20 nm and 5 nm whereas both the source and the drain length are maintained at 10 nm. Germanium and silicon are used as the source and drain material whereas monolayer MoS_2 (thickness~0.65 nm) is the channel material. HfO_2 is used as the oxide layer due to its high k dielectric constant with a thickness of 2 nm. The tunneling mechanism in the transistor depends on the band alignment of the source and channel region. For tunneling to happen, the channel conduction (valence) band of n-type TFET (p-type TFET) should be below (top) of the source valence (conduction) band as shown in the band diagrams of Fig. 1(a) and 1(b). At sufficient drain to source bias, an electrochemical potential develops in both types of TFETs; the carriers start to flow when the tunneling window opens due to the application of gate voltage. The steps of Verilog-A modeling

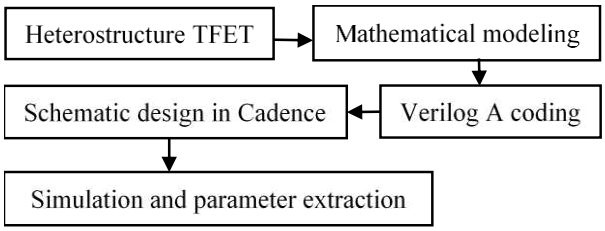

Fig. 2. Flow chart representing the compact model simulation of MoS_2-based TFET in Cadence/Spectre.

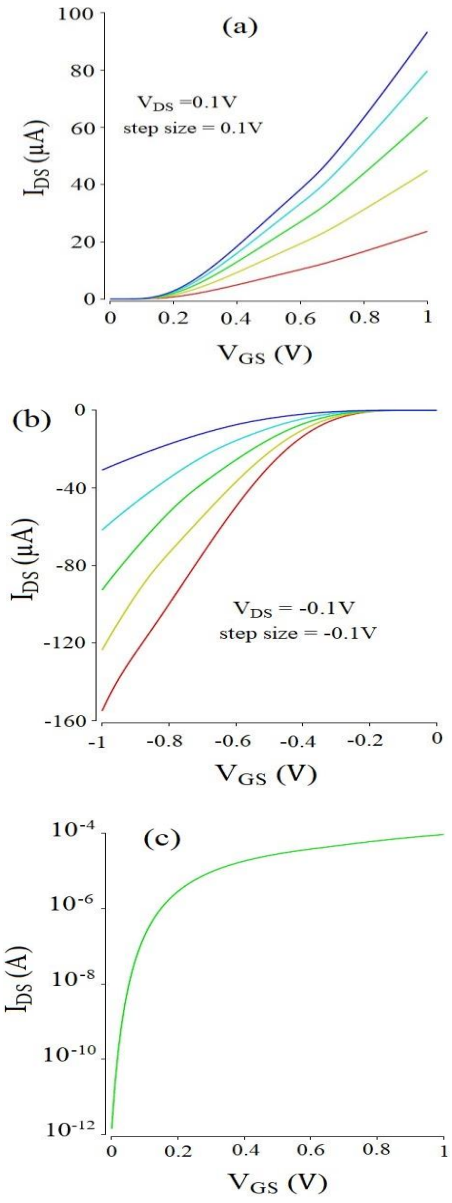

Fig. 3. Linearize plot of IDS vs VGS for (a) n-type TFET. (b) p-type TFET. (c) Logarithmic plot of I_{DS} vs V_{GS} for V_{DS}=0.5 V showing the sub-threshold region of n-type TFET.

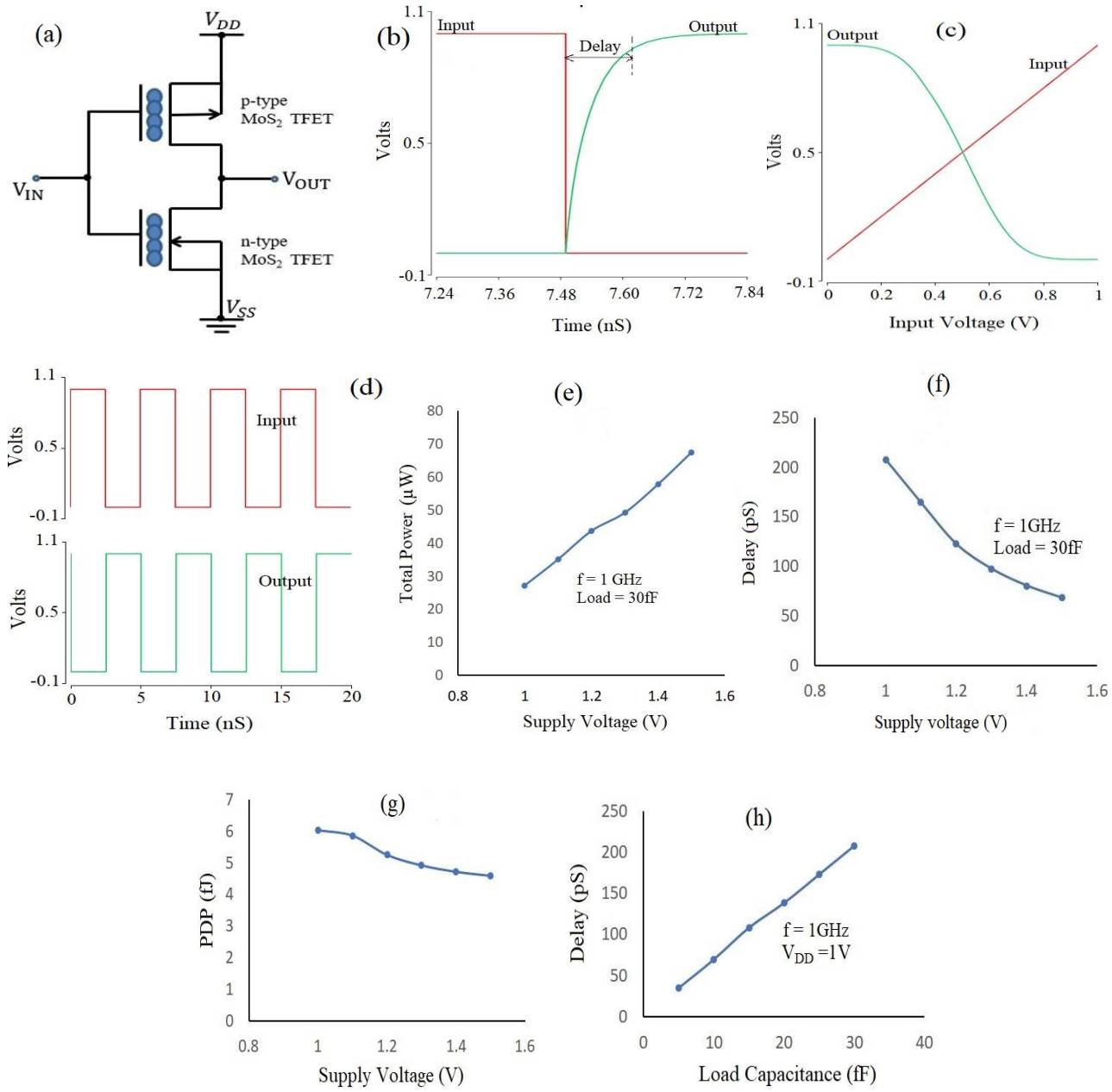

Fig. 4. Inverter circuit with TFET, its output characteristics with red (input) and green (output) line, and the performance parameters against the supply voltage and load capacitance. (a) Inverter circuit, (b) The measurement of inverter delay, (c) Voltage transfer characteristics of the inverter, (d) Output characteristic of the inverter, (e) Total power of the inverter, (f) The delay changes with the supply voltage, at a load capacitance of 30 fF, (g) Power delay product in the scale of femtojoule w.r.t supply voltages, (h) The delay changes with the increase of load capacitance.

in Cadence/Spectre simulator are presented in the flow chart of Fig. 2.

The relation of I_{DS} and V_{GS} with V_{DS} ranging from 0.1V to 0.5V for n-type TFET and -0.5V to -0.1V for p-type TFET as shown in Fig. 3(a) and 3(b). For the TFET simulation, the gate voltage is varied between 0V to 1V for n-type and 0V to -1V for p-type. The graphs show good variation in its output characteristics for different values of the V_{DS}. Fig. 3(c) represents the logarithmic plot of I_{DS} vs V_{GS} characteristics for n-type TFET at V_{DS}=0.5V to indicate the SS, which is 10 mV/decade according to our calculations. The on and off currents are 9.21×10^{-5} A and 1.74×10^{-12} A, which makes the on/off current ratio of 5.27×10^{7}. The above output characteristics verify that the compact model can suitably be applied to address the high-power consumption problem of both the analog and digital circuits.

III. MoS_2 TFET Inverter Design and Performance Evaluation

Unlike graphene, the high I_{ON}/I_{OFF} current ratio, responsible for the fast switching of the transistor, has made MoS_2 a good candidate for the circuit design in VLSI. The power and delay of the digital circuits are strongly dependent on the nature of the dielectric oxide layer and its thickness. The inverter is considered one of the fundamental circuits in the digital system. It consists of a complementary structure of both n and p-type transistors and serves as a building block for the ring oscillator. As shown in Fig. 4(a), a schematic of an inverter that has been designed with our compact model and simulated using Cadence/Spectre. Although the inverter can operate at 0.5V, the output is generated at 1 V to avoid slight distortion because of associated parasitic capacitances. Moreover, there are challenges associated with designing and fabricating high-performance MoS_2 PFETs [14]. Here, we have compensated for the limitations of hole injection at the S/D contacts by increasing the width of the p-type transistor. This is to improve its I_{ON} current and ensures that both the transistors switch relatively at the same time. The inverter delay is measured from the input-output switching characteristics of an inverter at a 90% point. We obtained ~145 ps delay for our inverter as shown in Fig. 4(b), which is much smaller than the earlier work reported in [15]. The slope of DC input-output characteristics of the inverter, shown in Fig. 4(c), indicates its performance and determines the critical point for a range of application. The output characteristics obtained from the inverter as shown in Fig. 4(d), which is simulated with a 0.2 GHz input signal and by considering the rise and fall time of 1 fs. The plot of total power dissipation against supply voltage is shown in Fig. 4(e). The power is simulated with a 30 fF load connected to the inverter output. The load capacitance can be adjusted based on the drive current of the transistor which can be varied by changing transistor's channel width. It is evident from the graph that the total power is increasing with the supply voltage and ranges from 27.2 µW at 1V to 67.4 µW at 1.5V. This is also evident from the relation-

$$P_{Total}=I_{stat} \times V_{DD}+\alpha \times f \times V_{DD}^{2} \times C_L \quad (1)$$

Here, I_{stat} is the static current; f, α, and C_L are the frequency, activity constant, and load capacitance, respectively. Similarly, the inverter's delay reduces with the increase of supply voltage as shown in Fig. 4(f). Unlike power consumption, the highest delay is obtained at the lowest supply voltage which is 207.9 pS at 1 V. This shows that there is a trade-off between power consumption and speed of an inverter which is commonly defined as "power delay product (PDP)." This is an important figure-of-merit for the inverter characterization that has been plotted in Fig. 4(g). This parameter also indicates the design of an inverter based on its application in the VLSI circuit. At the lowest supply power consideration i.e. 1V, PDP rating is 6.024 fJ which implies that our MoS_2 TFET model consumes low energy while performing high data transmission. In addition, Fig. 4(h) depicts the upward trend of the delay with the increase of load capacitance, as it takes more time to charge the larger capacitor.

TABLE I. Truth Table of Half Adder Circuit

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

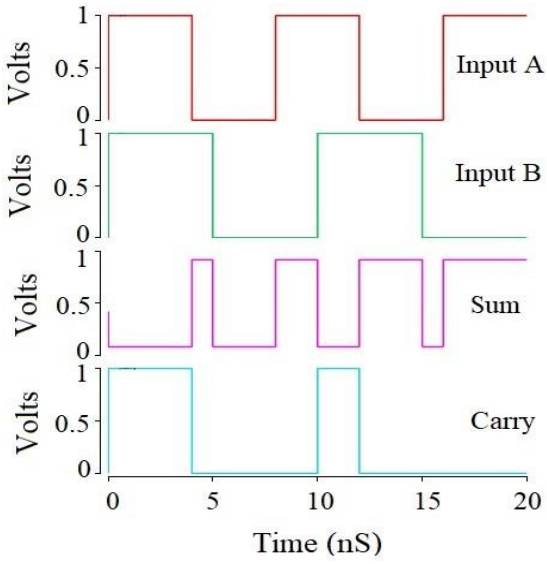

Fig. 5. Sum and carry output characteristics obtained from the input (A & B) of the Half adder circuit.

A. *Half Adder*

Half adder is one of the simplest and functional digital circuits to perform the addition of numbers. In this paper, we have designed XOR and AND gates for the two inputs (A and B) of the half adder to generate sum and carry output signals, respectively. In Fig 5, the simulated sum and carry obtained from the inputs are shown following the Boolean expression and truth table presented in Table I

$$Sum=A \oplus B$$
$$Carry=AB$$

B. *MoS_2 TFET Ring Oscillator*

The ring oscillator consists of a cascade structure of odd number of inverters. Usually, it does not require any input signal, because the output of the last inverter is fed back to the input of the first inverter as shown in Fig. 6. The oscillator is the most important building block of a phase-locked loop (PLL) or frequency synthesizer [16-18]. There are different types of oscillators with their own merits and demerits [19]. The ring oscillator is favored over the LC oscillator because of its wide tuning range, reduced die area, and low power consumption. It is also suitable for data clock recovery circuits. However, it suffers from high phase noise and low Q-factor which deteriorates its performance in RF applications. The output of

TABLE II. COMPARISON AMONG THE PARAMETERS OF THE DESIGNED RING OSCILLATOR

Parameter	This work	CMOS [21]	CMOS [22]	CMOS [23]	GFET [24]	FINFET [25]
Technology (nm)	20	180	180	65	180	45
Power supply (V)	1	1.8	1.8	1.2	1	1
Power Consumption (mW)	0.083	1.16	0.27	-	9.98	2.05
Frequency (GHz)	31.6	2.05	1	25.6	24.12	1.60
Phase noise at 1 MHz (dBc/Hz)	-122.5	-92.89	-94	-95.2	-104.1	-135.2

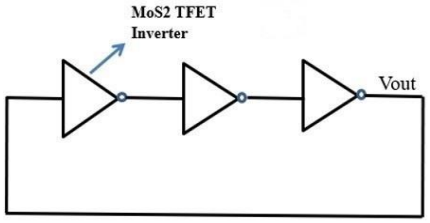

Fig. 6. Diagram of three stage MoS_2 TFET ring oscillator.

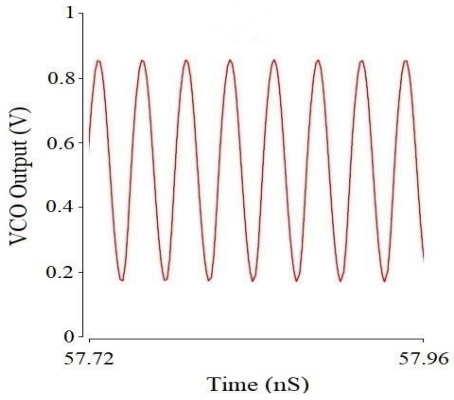

Fig. 7. Oscillation frequency obtained from the designed ring oscillator.

our designed oscillator is shown in Fig. 7, and the frequency of oscillation can be calculated from the relation

$$f_{osc}=\frac{1}{2N(t_r+t_f)} \quad (2)$$

Here, N, t_r, and t_f are the number of delay stages, rise, and fall times, respectively. The operating frequency of the designed three stages MoS_2-based ring oscillator is equal to 31.6 GHz, and the power consumption is 0.083 mW. Thus, our proposed ring oscillator is suitable for high frequency digital application with minimum power consumption. The comparison among the parameters of different types of ring oscillator is presented in Table II.

Phase noise is another important performance indicator of the ring oscillator. Excessive phase noise can cause jitter and frequency instability in PLL if not properly managed. Hence, it is desirable to design a low phase noise oscillator for phase-locked loop application. In Fig. 8, the measured phase noise is -122 dBc/Hz at 1 MHz offset frequency and -126 dBc/Hz at 10 MHz offset frequency. This shows an improvement in phase noise performance when compared to the work in [20, 21].

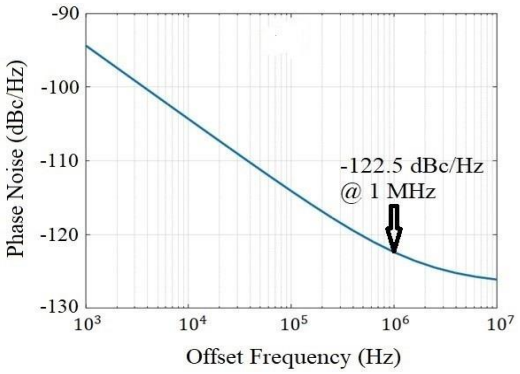

Fig. 8. Simulated phase noise of the ring oscillator.

IV. CONCLUSION

We have implemented compact models of TFET in Verilog-A and Cadence/Spectre simulator. TFET is advantageous in low power application because of its low sub-threshold swing, which is 10 mV/decade in our case. The I-V characteristics of both n and p-type TFETs are also presented. We have characterized our designed inverter from a number of consideration (power, delay, DC input/output, PDP) as it is considered the most integral part of the VLSI circuit. We have also implemented the inverter to design VLSI circuit components particularly a half adder a ring oscillator. After doing a performance analysis of these components, we have shown that the half adder follows exactly the truth table, and the ring oscillator can operate at a higher frequency with low power consumption. Moreover, the VCO shows an improved phase noise of -122 dBc/Hz at 1 MHz detuning frequency.

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