Stability of an Adaptive Switched Controller for Power System Oscillation Damping using Remote Synchrophasor Signals*

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***Abstract*— This paper is concerned with the stability of an adaptive switched controller for interarea power system oscillation damping using remote signals. These signals introduce variable latency into the damping control system due to phasor processing and communication network delays. In previous work, we designed an adaptive controller that dynamically switches among different compensators depending on the latency of the incoming measurements. To prevent switching instability, a long reset time was implemented. We demonstrated the stability of the adaptive system using simulations. In this work, we use the concept of average dwell time (ADT) of switched control systems to develop a sufficient condition that guarantees the stability of our adaptive switching algorithm. Using this condition, we formulate a feasibility problem to compute the minimum average dwell time for the set of designed compensators. We apply the algorithm to a thyristor-controlled series compensator on a two-area power system and show that the adaptive controller is stable for time-varying latency.**

I. Introduction

The advent of synchronized phasor measurement units (PMUs) at many locations across power grids enables the use of such remote signals for interarea oscillation damping. Unlike local signals, remote measurements can provide better observability of interarea modes and thus more effective control using power-electronics-based devices such as a thyristor-controller series compensator (TCSC). However, communication of data from remote PMUs can introduce data loss, corruption, and latency. Data loss and corruption can be partially mitigated using data reconstruction methods or state estimation techniques [1]. On the other hand, latency is inherent in remote signals and is increased by such data processing algorithms. Different levels of congestion in communication network produces varying amounts of measurement latency to be compensated.

In previous work [2], we developed an adaptive switched controller to damp interarea oscillations for a two-area power system using remote PMU signals. The controller consisted of several compensators, each designed for a specific amount of data latency in the PMUs. Thus the adaptive scheme would switch among the compensators depending on the measured latency of the input signal. To prevent instability due to switching among the different compensators, we designed the algorithm to have a sufficiently long reset time, much longer than the typical decay time of the oscillations. Through simulation, we showed that the switching algorithm exhibited stability.

In this work, we formally demonstrate the stability of the adaptive controller design using a theoretical results for switched systems. We employ the concept of average dwell time (ADT) switching sequences to construct a stability proof for our designed adaptive controller. Using these theoretical results, we compute the minimum average dwell time to guarantee stability for a selected set of compensators under our adaptive control scheme. We show that the reset time chosen in our previous work is sufficient to ensure stable operation. Other researchers have also considered stability of networked control systems with time varying delays [3]. However, the main drawback of [3] is that it is more computationally expensive compared to the algorithm introduced in this paper.

II. PMU Data Latency

Phasor measurement units (PMUs) are distributed across wide geographical regions and the data is transmitted across long communication links. Generally the data is first collected by a local utilities at their phasor data concentrators (PDCs), then streamed to the central PDC of the regional system operator. An example of this hierarchical arrangement is shown in Figure 1.

The phasor measurements face a number of delays along the signal path. First, the frequency estimation and phasor calculation algorithms typically require multiple cycles of measured data to compute the phasor quantities. This type of fixed delay sets a floor for the overall time-varying measurement latency. After the phasor is computed, the data is transmitted across communication networks to the local PDC and finally to the central PDC. In addition to the delays across the communication network infrastructure, which can be calculated based on the type of communication link [4], the data also encounters small delays at each PDC due to processing. As an example, we list the estimated delays for the Quebec power system in Table I [5].

We model the measurement latency using the same approach as in our previous work, namely a minimum delay with a variable component, taking the approach used in [6] to calculate total time delay T_{ld} as

$$T_{\mathrm{ld}} = T_s + T_b + T_p + T_r$$

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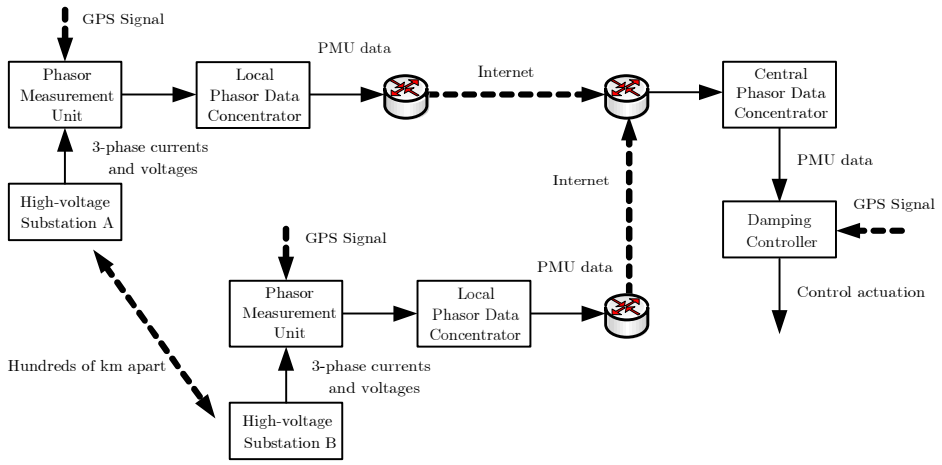

Fig. 1. PMU Data Communication Path

TABLE I
PMU DATA LATENCY IN THE QUEBEC POWER SYSTEM

PMU processing time	73 ms
Local data concentration	16 ms
2,000 km in optical fiber	10 ms
Central data concentration	10 ms
Total estimated data latency	109 ms

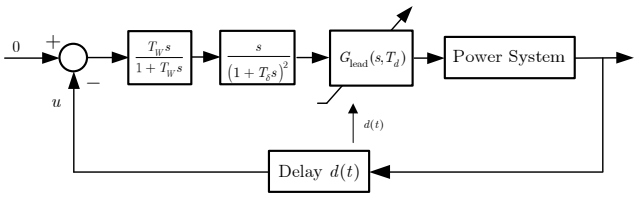

Fig. 2. TCSC Adaptive Control System

where $T_s = P_s/D_r$ is the serial delay, P_s is the packet size in bits, D_r is the transmission rate of the link in bits/s, and T_b is the delay between data packets. Moreover, $T_p = L/\nu$ is the propagation delay, where L is the link length in km and ν is the propagation speed in the link in km/s, and T_r is the routing delay.

III. CONTROL DESIGN

The adaptive controller follows a similar control design as in [2] with some minor changes to reflect a more practical implementation. For damping control with a thyristor-controller series compensator (TCSC), we typically use a derivative filter with a small time constant T_δ in addition to the washout filter and thus no additional phase lead is required. For our controller design, we adapt the controller from [7] and add a phase lead compensator to counteract the phase lag caused by data latency. The overall controller is

$$G_c(s,T_d) = K(T_d)\frac{1+T_{\text{num}}(T_d)s}{1+T_{\text{den}}(T_d)s}\frac{s}{(1+T_\delta s)^2}\frac{T_w s}{1+T_w s} \qquad (1)$$

and the system is shown in Figure 2. Note that we switch among several phase lead compensators which are each designed for a specific level of delay T_d.

As the input signal latency $d(t)$ varies, we use the adaptive algorithm from [2] to select the controller delay T_d such that $T_d \geq d(t)$, but with dwell time considerations to prevent switching instability. The algorithm can be summarized as follows:

Adaptive Control Algorithm

Prespecify a set of T_d values: $0 < T_{d1} < T_{d2} < \cdots < T_{dn}$.

At time $t = t_k$, where t is the time at the controller, the time delay T_{di} is used to set the controller.

for $t = t_k + \Delta t$, where Δt is the sampling period of the PMU data if the next data point is already in the input data buffer, or the incremental time of arrival of the next data point if the input data buffer is empty.

if the data delay is larger than the T_{di}, switch to a controller with the lowest latency T_{dj} which is higher than the data delay.

elseif the maximum latency of all the data in the last T_r s is less than T_{dj}, where $T_{dj} < T_{di}$, switch in the controller with a lower latency T_{dj}.

else continue with the same controller.

end

End algorithm

Note that the reset time T_r is used to limit rapid switching and prevent instability. In the next section, we will derive a sufficient condition to guarantee stability of the closed-loop switched system.

IV. STABILITY OF THE SWITCHED SYSTEM

It is well-known [8] that a switched system might be stable under sufficiently slow switching sequences, such that the transient effects dissipate after each switch. The simplest way to specify slow switching sequences is to restrict the class of admissible switching signals to satisfy a *dwell time* constraint. That is to introduce a number $\tau_d > 0$ such that

the switching times satisfy the inequality $t_{k+1} - t_k \geq \tau_d$. Specifying a dwell time constraint may be too restrictive in the context of controlled switching. Thus, one can consider an enlarged family of switching signals that occasionally have consecutive discontinuities separated by less than τ_d, but for which the average interval between discontinuities is no less than τ_d. This concept was first formalized in [9] as *average dwell time*.

Let $N_\sigma(t,T)$ denote the number of discontinuities of a switching signal σ on the time interval (t,T). We say that σ has average dwell time τ_d if there exist positive numbers N_0 and τ_d such that

$$N_\sigma(t,T) \leq N_0 + \tfrac{T-t}{\tau_d} \qquad \forall T \geq t \geq 0.$$

Our goal is to establish a stability criteria for a class of switched delay system under an average dwell time constraint. We consider a class of switched delay system of the form

$$\dot{x}(t) = A_{\sigma(t)}x(t) + B_{\sigma(t)}x(t-d_t), \tag{2}$$

where $x \in \mathbb{R}^n$ denotes the state of the system, $\sigma(t) : [0,\infty) \to \mathcal{S} = \{1,2,...,N\}$ is the piecewise constant switching signal.

We propose a sufficient condition that guarantees the stability of the adaptive switching mechanism in [2]. We formulate the problem for arbitrary number of modes.

Let us denote the latency of the arriving data by $d_t \in [0, d_{\max}]$. Assume that controller i has been designed to work in the range of $d_t \in [0, d_i]$ for $i \in \mathcal{S}$ with $d_{i+1} > d_i$ and $d_N = d_{\max}$. We consider the following switching mechanism. In mode i,

- If the data latency is larger than d_i, switch to the controller with the smallest delay d_j which is greater than the data latency.
- If the data latency is smaller than d_j where $d_j < d_i$, switch to the controller with a lower delay, considering that the average time between switches is at least τ_d.

Our goal is to find a minimum value of τ_d for which the switched system remains stable. The following theorem provides a lower bound for τ_d.

We define $F_i := \begin{bmatrix} A_i & 0 \end{bmatrix}$ and $H_i := \begin{bmatrix} 0 & B_i \end{bmatrix}$.

Theorem 1: Consider the delayed switched system (2) with $d_t \in [0, d_{\max})$. Assume that controller i has been designed to work in the range of $d_t \in [0, d_i]$ for $i \in \mathcal{S}$ with $d_{i+1} > d_i$ and $d_N = d_{\max}$. If there exist positive definite symmetric matrices $P_i, Z_i \in \mathbb{R}^{n\times n}$, matrices $N_i \in \mathbb{R}^{2n\times n}$ and a constant $\mu \geq 1$ such that

$$P_i \leq \mu P_j \quad Z_i \leq \mu Z_j \quad \forall i,j \in \mathcal{S} \tag{3}$$

$$\Phi_i := \begin{bmatrix} \phi_i & N_i \\ N_i' & -d_i^{-1}Z_i \end{bmatrix} < 0 \tag{4}$$

with

$$\begin{aligned} \phi_i &= F_i' \begin{bmatrix} P_i & 0 \end{bmatrix} + \begin{bmatrix} P_i & 0 \end{bmatrix}' F_i \\ &+ H_i' \begin{bmatrix} P_i & 0 \end{bmatrix} + \begin{bmatrix} P_i & 0 \end{bmatrix}' H_i \\ &+ d_{\max}(F_i + H_i)' Z_i (F_i + H_i) \\ &- N_i \begin{bmatrix} I & -I \end{bmatrix} - \begin{bmatrix} I & -I \end{bmatrix}' N_i' \end{aligned}$$

then the system is stable for any average dwell time switching sequences with $\tau_d > \frac{\log \mu}{\alpha}$ where α is given by

$$\alpha = \frac{\min\limits_i \lambda_{\min}(-(\phi_i + d_i N_i Z_i^{-1} N_i'))}{\max\limits_i \lambda_{\max}(P_i) + \frac{d_{\max}^2}{2} \max\limits_i \lambda_{\max}(Z_i)}. \tag{5}$$

It is worth noting that for a fixed value of $\mu \geq 1$, (3)-(4) are linear matrix inequality conditions. By performing a line search on μ, one should look for the smallest μ for which (3)-(4) are feasible.

Proof: Assume that the system is in the ith mode for $t \in [t_k, t_{k+1}]$. We have

$$\begin{aligned} \dot{x}(t) &= A_i x(t) + B_i x(t-d_t) + B_i x(t) - B_i x(t) \\ &= (A_i + B_i)x(t) - B_i \int_{t-d_t}^{t} \dot{x}(s)\, ds. \end{aligned}$$

We choose the Lyapunov function

$$\begin{aligned} V(t) &= V_1(t) + V_2(t), \\ V_1(t) &= x(t)' P_{\sigma(t)} x(t), \\ V_2(t) &= \int_{-d_{\max}}^{0} \int_{t+\theta}^{t} \dot{x}(s)' Z_{\sigma(s)} \dot{x}(s)\, ds\, d\theta. \end{aligned}$$

Let us compute $\dot{V}(t)$ for $t \in [t_k, t_{k+1})$. We assume that in this time interval $\sigma(t) = i$

$$\begin{aligned} \dot{V}_1(t) &= x(t)' \left((A_i + B_i)' P_i + P_i (A_i + B_i)\right) x(t) \\ &- 2x(t)' P_i B_i \int_{t-d_t}^{t} \dot{x}(s)\, ds \end{aligned}$$

$$\dot{V}_2(t) = d_{\max} \dot{x}(t)' Z_i \dot{x}(t) - \int_{t-d_{\max}}^{t} \dot{x}(s)' Z_i \dot{x}(s)\, ds$$

Therefore,

$$\begin{aligned} \dot{V}(t) &\leq x(t)' \left((A_i + B_i)' P_i + P_i (A_i + B_i)\right) x(t) \\ &- 2x(t)' P_i B_i \int_{t-d_t}^{t} \dot{x}(s)\, ds \\ &+ d_{\max} \dot{x}(t)' Z_i \dot{x}(t) - \int_{t-d_t}^{t} \dot{x}(s)' Z_i \dot{x}(s)\, ds \\ &= x(t)' \left((A_i + B_i)' P_i + P_i (A_i + B_i)\right) x(t) \\ &- 2x(t)' P_i B_i \int_{t-d_t}^{t} \dot{x}(s)\, ds \\ &+ d_{\max} \left(A_i x(t) + B_i x(t-d_t)\right)' Z_i \big(A_i x(t) + \\ &+ B_i x(t-d_t)\big) - \int_{t-d_t}^{t} \dot{x}(s)' Z_i \dot{x}(s)\, ds \\ &= x(t)' \left((A_i + B_i)' P_i + P_i (A_i + B_i)\right) x(t) \\ &- 2x(t)' P_i B_i (x(t) - x(t-d_t)) \\ &+ d_{\max} x(t)' A_i' Z_i A_i x(t) \\ &+ 2d_{\max} x(t)' A_i' Z_i B_i x(t-d_t) \\ &+ d_{\max} x(t-d_t)' B_i' Z_i B_i x(t-d_t) \\ &- \int_{t-d_t}^{t} \dot{x}(s)' Z_i \dot{x}(s)\, ds \end{aligned} \tag{6}$$

TABLE II
PHASE LEAD COMPENSATORS $G_c(s)$

Controller #	Delay (T_d)	Lag (Delay)	Lead	Damp.	K	T_N	T_D
1	10 ms	2.4°	2.4°	5%	0.25	0.0622	0.237
2	50 ms	11.8°	11.8°	4.8%	0.2	0.0597	0.197
3	100 ms	23.6°	23.6°	4.5%	0.15	0.0556	0.159
4	150 ms	35.4°	30.0°	3.9%	0.12	0.0505	0.140
5	200 ms	47.2°	37.2°	3.2%	0.09	0.0440	0.121

Defining $\xi(t) := \begin{bmatrix} x(t) & x(t-d_t) \end{bmatrix}$, For any set of matrices N_i, we have

$$\begin{aligned} 2\xi' N_i \begin{bmatrix} I & -I \end{bmatrix} \xi &= 2\xi' N_i \int_{t-d_t}^{t} \dot{x}(s)\, ds \\ &\leq d(t)\xi' N_i Z_i^{-1} N_i' \xi \\ &+ \int_{t-d_t}^{t} \dot{x}(s)' Z_i \dot{x}(s)\, ds. \end{aligned} \quad (7)$$

Combining (6) and (7), we have

$$\begin{aligned} \dot{V}(t) \leq\ & x(t)' \left((A_i+B_i)'P_i + P_i(A_i+B_i)\right) x(t) \\ &- 2x(t)'P_iB_i(x(t)-x(t-d_t)) \\ &+ d_{\max} x(t) A_i' Z_i A_i x(t) \\ &+ 2d_{\max} x(t)' A_i' Z_i B_i x(t-d_t) \\ &+ d_{\max} x(t-d_t)' B_i' Z_i B_i x(t-d_t) \\ &- 2\xi' N_i \begin{bmatrix} I & -I \end{bmatrix} \xi + d_i \xi' N_i Z_i^{-1} N_i' \xi \\ \\ =\ & \xi' (F_i' \begin{bmatrix} P_i & 0 \end{bmatrix} + \begin{bmatrix} P_i & 0 \end{bmatrix}' F_i \\ &+ H_i' \begin{bmatrix} P_i & 0 \end{bmatrix} + \begin{bmatrix} P_i & 0 \end{bmatrix}' H_i \\ &+ d_{\max} (F_i+H_i)' Z_i (F_i+H_i) \\ &- N_i \begin{bmatrix} I & -I \end{bmatrix} - \begin{bmatrix} I & -I \end{bmatrix}' N_i' \\ &+ d_i N_i Z_i^{-1} N_i') \xi \end{aligned}$$

Thus, we have $\dot{V}(t) \leq \xi'(\phi_i + d_i N_i Z_i^{-1} N_i')\xi$. With α given in (5), one can show that

$$\dot{V}(t) \leq -\alpha V(t).$$

Therefore, the Lyapunov function decreases between switchings. Following (3), at a switching instant t_k, we have $V_{\sigma(t_k)}(t_k) \leq \mu V_{\sigma(t_k^-)}(t_k^-)$. Using the result of [8, Theorem 3.2], we conclude that the system is stable for any average dwell time switching with $\tau_d > \frac{\log \mu}{\alpha}$. ■

It is worth noting that the number of decision variables in (4) is a linear function of the number of modes. However the number of decision variables in [3] grows quadratically with the number of modes. In particular, if N denotes the number of modes and n is the dimension of the closed-loop systems, the number of decision variable in (4) is $N(3n^2+n)$ while [3] requires $N(5N+1)n(n+1)/2$ decision variable.

V. SIMULATION RESULTS

A. Two-Area Power System

To illustrate the capability of our design, we consider a two-area, four-generator system adapted from [10] and shown in Figure 3. We use the same parameters from [2], such that the system has significant interarea power transfer and is prone to unstable oscillations following a short circuit fault. In this system, Generators 1 and 2 in Area 1 are coherent and Generators 11 and 12 in Area 2 are coherent and all generators are represented using detailed machine models with excitation systems.

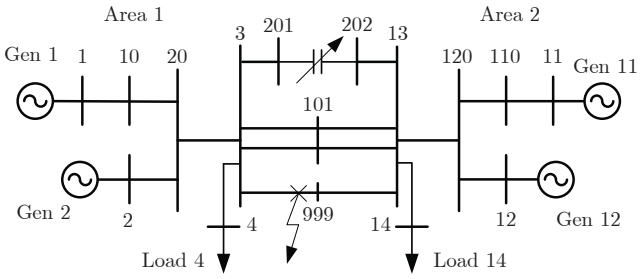

Fig. 3. Four-Machine, Two-Area System

The TCSC is located in series with one of the interarea lines, and a short circuit fault is applied near Bus 999 to excite the system. We choose the difference between the averaged angles $\overline{\theta}_a$ in each area as our input signal

$$\overline{\theta}_a = 0.5(\theta_1 + \theta_2) - 0.5(\theta_{11} + \theta_{12})$$

where θ_i is the phase angle of the voltage at Bus i. This input signal exhibits good observability of the interarea mode, and is often present in PMU deployments. Further discussion on the choice of input signal can be found in [2].

B. Multiple Compensators for Time-Varying Data Latency

In designing an adaptive controller for time-varying latency, we select delay levels starting at 50 ms, at increments of 50 ms, up to 250 ms. We also include a delay level of 10 ms to show the nearly-ideal case.

We implement the overall controller from (1), where the time constant of the high-pass washout filter is $T_w = 10$ s and the time constant of the derivative filter is $T_\delta = 0.04$ s, the same as in [7]. The adaptive parameters $K(T_d)$, $T_1(T_d)$, and $T_2(T_d)$ are given in Table II.

C. Average Dwell Time

Based on Theorem 1, we formulate a linear matrix inequality (LMI) feasibility problem and calculate the ADT for the designed controllers in Table II. The LMI feasibility problem becomes prohibitively large as the number of switched controllers and system states increases. To improve the optimization convergence and obtain a solution in a reasonable amount of time, we reduce the state-space model

of the power system before applying the TCSC controller. There are two parts to the process.

First, we remove the system modes, which are located at the origin of the root-locus. These poles correspond to the fact that the machine angles have multiple stable solutions with periodicity 2π. We perform a simple transformation on the angles to eliminate these poles, which has the effect of slightly shifting the frequency of the interarea mode.

The second step is to reduce the order of the power system dynamic model. After removing the 2 system modes, we have a plant with 35 states. We then perform a balanced reduction to reduce the system to 3rd order. Because the interarea mode is unstable and the TCSC does not significantly affect the other states, the interarea mode is kept in the 3rd order system and its behavior closely resembles the original system. Figure 4 compares the root-locus plots of the reduced model and original system.

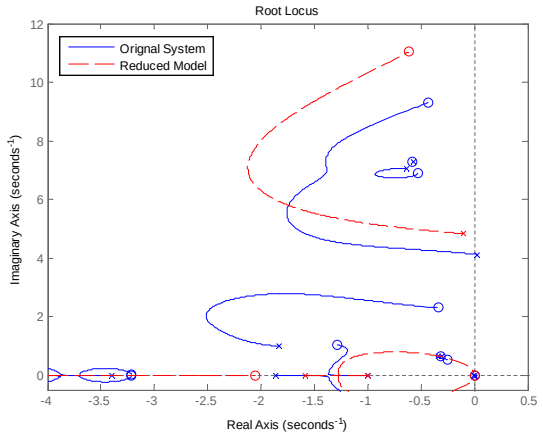

Fig. 4. Root-Locus Plots for Original and Reduced Systems

Let $(A_p, B_p, C_p, 0)$ and $(A_c^i, B_c^i, C_c^i, D_c^i)$ be the state space realizations for the reduced plant and the controller in mode i, respectively. Assume that $A_p \in \mathbb{R}^{n_{pl} \times n_{pl}}$ and $A_c^i \in \mathbb{R}^{n_{cn} \times n_{cn}}$. The matrices in (2) which correspond to the closed-loop matrices are given by

$$A_i = \begin{bmatrix} A_p & B_p C_c^i \\ 0_{n_{cn} \times n_{pl}} & A_c^i \end{bmatrix}$$

$$B_i = \begin{bmatrix} -B_p D_c^i C_p & 0_{n_{pl} \times n_{cn}} \\ -B_c^i C_p & 0_{n_{cn} \times n_{cn}} \end{bmatrix}.$$

Using Theorem 1, we can show that for the groups of controllers in Table III, the described switching mechanism stabilizes the closed-loop system. Note that as additional controllers are combined, the minimum average dwell time increases to guarantee stability.

D. Adaptive Controller Performance

This adaptive algorithm is applied to the 2-area system for the same short-circuit disturbance. The adaptive control performance is shown in Figure 5. In this 15-second simulation, a data buffer function is created in PST. We

TABLE III
AVERAGE DWELL TIME RESULTS

Controller #	Delays (ms)	Min. ADT (s)
(4,5)	(150,200)	0.083
(3,4,5)	(100,150,200)	0.162
(2,3,4,5)	(50,100,150,200)	0.253
(1,2,3,4,5)	(10,50,100,150,200)	1.182

simulate data latency with variable arrival time based on a Poisson stochastic process, with a minimum latency of 90 ms. The parameters of the probability distribution function are chosen such that the data latency is in the range $d(t) \in [90, 110]$ ms in 99% of cases. For a 1-s interval during the disturbance, latency variability is increased to represent a brief congestion. We set the minimum reset time to $T_r = 10$ s, such that it is significantly larger than the minimum average dwell time.

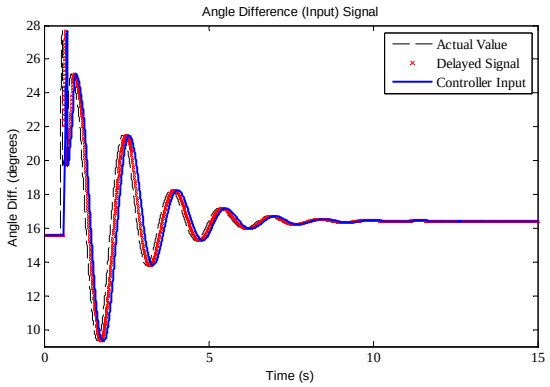

Fig. 5. Damping Performance of the Adaptive Controller

Figure 5 shows the angle difference signal $\overline{\theta}_a$ measured instantaneously at the buses, the time that the signal $\overline{\theta}_a$ actually arrives at the controller, and the $\overline{\theta}_a$ waveform that is used as the damping controller input. A close-up is shown in Figure 6. Note the initial delay for the phasor data $\overline{\theta}_a$ to be picked up by the data buffer.

In Figure 7, we show the phase compensation selection by the adaptive algorithm. The algorithm starts with $T_d = 100$ ms compensator and switches to the $T_d = 200$ ms

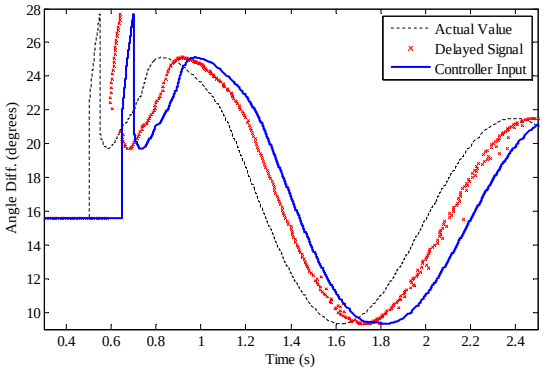

Fig. 6. Performance with Data Latency and Controller Delay

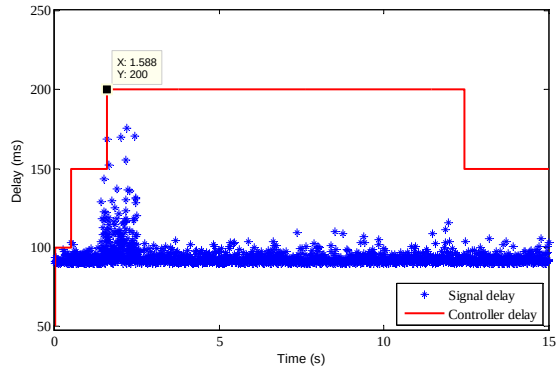

Fig. 7. Adaptive Compensator Selection

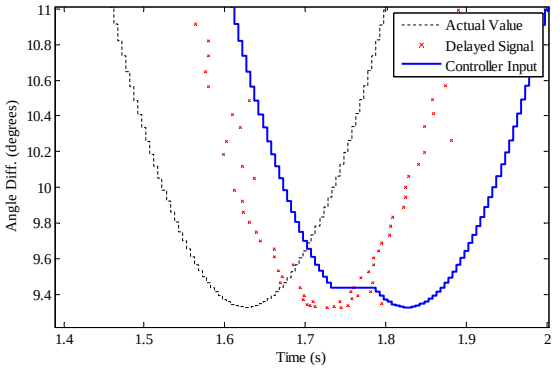

Fig. 8. Close-Up of Input Signal during Compensator Switching

compensator before the fault and it does not affect the performance. At $t = 1.588$ s, a data point arrives with greater than 150 ms latency, so the algorithm switches to the $T_d = 200$ ms compensator. We see that 150 ms later (at $t = 1.738$ s), the controller holds the last data point in input queue for 50 ms while it switches to the $T_d = 200$ ms compensator (Figure 8).

After switching in the 200 ms latency compensators, the controller performance is still excellent. To damp the oscillations, the controller saturates as it drives the effective reactance of the TCSC branch connection Buses 3 and 13 to a minimum, as shown in Figure 9.

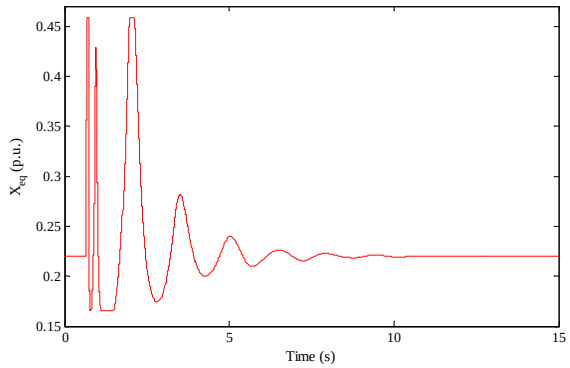

Fig. 9. TCSC Control Action

VI. Conclusion

In this paper, we analyzed the stability of an adaptive control scheme for a power system interarea damping controller using remote PMU data with time-varying latency. The adaptive control consists of a controller switching algorithm based on the latency of PMU data, and a phase compensation design of the controller for a given set of latency. Latency requires adding phase lead compensation, and we use a bank of phase-lead controllers governed by a latency-monitoring, adaptive algorithm to switch among them. We developed a sufficient condition to guarantee that this switched control system is stable as long as an average dwell time constant is met. Finally, we illustrated the control design and demonstrated the performance using a 2-area power system.

Future work includes the development and analysis of adaptive control algorithms for multiple actuators considering packet loss, late data arrivals, and cooperative control. Another topic for future research is to design a set of controllers that are robust both to the input signal delays and to the variation in the operating conditions of the system.

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