A Cyclic CMOS Time-to-Digital Converter With Deep Sub-nanosecond Resolution

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Abstract

A novel cyclic time-to-digital converter (TDC) is proposed in this paper. The measured resolution (or LSB width equivalent) can reach 68 picoseconds, and the corresponding single-shot errors are around 1/2 LSB width. Under a single 3.3V power supply, the stand-by current consumption is measured to be 0.3 mA only, including the I/O pads. The operation current consumption is measured to be 370 uA under 100 k/sec measurement rate.

Introduction

Time interval digitization is an important technique for many applications, such as laser range finder, phase meter, and PM or FM demodulators, ... etc. [1-3]. The conventional un-integrated TDC circuit is very bulky (i.e., 10 cm * 16 cm), and has high power consumption of 5W in the discrete ECL-based circuit to maintain the subnanosecond resolution. At the end of 1995, a novel CMOS TDC circuit with a linear delay line structure was proposed to get 780 picoseconds resolution, 15 *m*W power consumption, but with a poor single shot accuracy, i.e. 3 *ns* [4]. The mismatch among pulse-shrinking delay elements limits the accuracy of the TDC. The power wasting calibration of the TDC must be done continuously to keep the reference pulse just disappeared in the last stage of the delay line.

Another kind of CMOS TDC with a cyclic delay line was announced to greatly improve the linearity [5]. The effective resolution was measured to be 286 picoseconds with all single-shot errors less than 143 picoseconds. Its structure is replotted in Fig. 1, and the same pulse-shrinking delay element used as in the linear CMOS TDC [4] is shown in Fig. 2. By adjusting the bias voltage V_{bias}, the pulse shrinking per cycle can be easily controlled. For calibration, the reference pulse is required to circulate in the cyclic delay line enough times to get satisfactory resolution by properly setting V_{bias} only. It is not necessary to make the reference pulse just shrunk out at some specific cycle or stage of the delay line as the former TDC with the linear delay line does. The calibration is done under requirement instead of continuously. By the way, the input pulse will visit each element in the cyclic delay line one time per cycle. The pulse shrinking time must be the same from cycle to cycle. Theoretically and practically, the cyclic TDC will not have any nonlinearity problem. But, the bias adjustment is still required to ensure the resolution fine enough. It is case dependent and must be done externally.

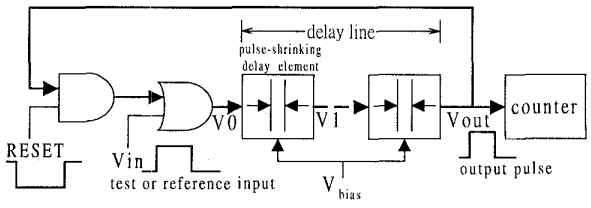

Fig. 1

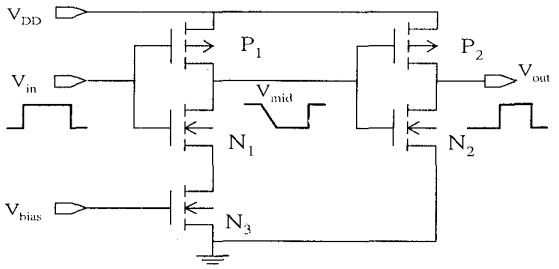

Fig. 2

Later, a FPGA-based TDC without the need of any continuous calibration or external bias adjustment was proposed in 1997 [6]. The resolution is as low as 200 picoseconds, but some of the measured single shot errors are larger than 1/2 LSB width. Furthermore, too many trial-and-errors must be adopted in the design phase to get satisfactory implementations. The FPGA TDC is not only design-time-consuming but also unsuitable for mass production. Another major disadvantage is that the element matching becomes a significant issue again. It is more difficult to control the element matching in FPGA than in customer-designed ICs. The resolution of the FPGA TDC will be limited.

To overcome all the shortcomings, a new TDC circuit without the need of any continuous calibration, bias adjustment, nor trial-and-error implementation is proposed in this paper.

Circuit Description

Fig. 3 shows the block diagram of the new TDC. The cyclic structure of the delay line is reserved for its perfect linearity, but the body of the delay line is realized by even number of NOT gates instead of pulse-shrinking delay elements to reduce the pulse shrinking per cycle. The input pulse circulates in the cyclic structure. It is shrunk by merely one stage of the pulse-shrinking element each cycle. The effective resolution will be exquisite. The most important modification is made on the pulse-shrinking delay element in Fig. 2. The new version of the pulse-shrinking element is depicted in Fig. 4 conceptually.

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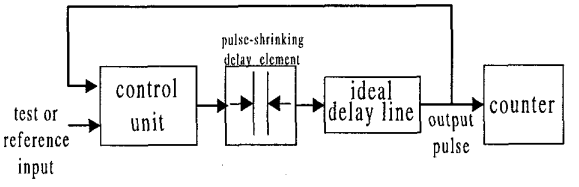

Fig. 3

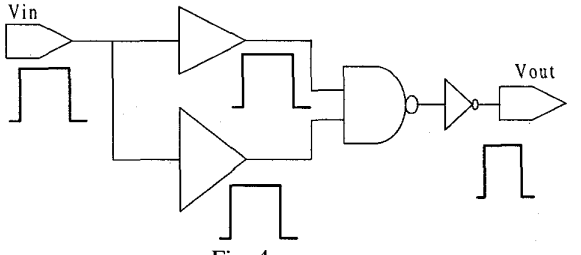

Fig. 4

The input pulse is fed into the large and the small signal buffers separately, then the output pulses with different delay are ANDed to get the final shrunk pulse. The degree of pulse shrinking is thoroughly decided by the aspect ratio of the two signal buffers in Fig. 4. The circuit becomes fully digital, and no bias adjustment is needed for pulse shrinking control. Theoretically, the more match the two signal buffers, the less shrinking the output pulse. We can easily vary the aspect ratio of the two signal buffers to get any effective LSB width of the TDC as required. The corresponding resolution could be made extremely fine.

The circuit practically realized for the new TDC is shown in Fig. 5. During the design phase, It was found that the LSB width of the TDC can't be made close to zero even if both buffers in Fig. 4 are designed to be equal. The two input n-MOS transistors of the NAND gate experience different body effect, for the n-MOS transistor of one input is stacked over that of the other. So these two buffers can't control the pulse-shrinking capability of the TDC independently, and are eliminated completely in the realized circuit. On the contrast, the inhomogeneous dimension of the two NAND gates and the other NOT gates in the delay line buffers makes the input pulse undergo different rising and falling time at the interface boundaries between the NAND gates and the NOT gates. This machanism can be used to accurately control the pulse shrinking per cycle in the new cyclic TDC.

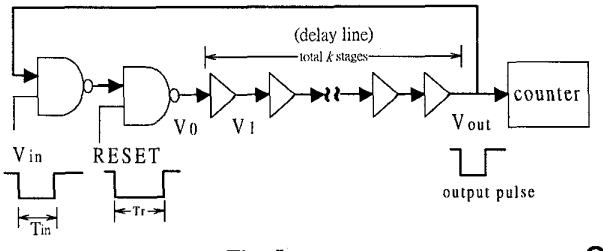

Fig. 5

For better understanding, the conceptual delay line shown in Fig. 6 is used instead to demonstrate the impact of the inhomogeneity of the delay line on the rising and falling time of the input pulse.

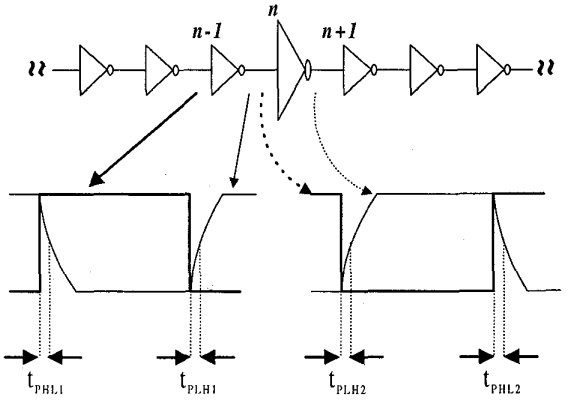

Fig. 6

Suppose that all the NOT gates have the same dimension except the ***n***-th inverter whose width is the β times of those of the others. To simplify the derivation, the input pulse is supposed to be stepwise at each stage for the first order approximation only. When the pulse goes from the ***(n-1)***-th stage to the ***n***-th stage, the falling time and the rising time can be given [7]:

$$t_{PHL1} = \frac{2C_{L_n}V_{TN}}{k_{N_{n-1}}(V_{DD}-V_{TN})^2} + \frac{C_{L_n}}{k_{N_{n-1}}(V_{DD}-V_{TN})}\ln\left(\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right) \quad (1)$$

$$t_{PLH1} = \frac{-2C_{L_n}V_{TP}}{k_{P_{n-1}}(V_{DD}+V_{TP})^2} + \frac{C_{L_n}}{k_{P_{n-1}}(V_{DD}+V_{TP})}\ln\left(\frac{1.5V_{DD}+2V_{TP}}{0.5V_{DD}}\right) \quad (2)$$

where $k_{N_{n-1}}$, $k_{P_{n-1}}$ are the transconductance parameters of the ***(n-1)***-th NOT gate, and C_{L_n} is the effective input capacitance of the ***n***-th NOT gate. Assume $-V_{TP} = V_{TN}$, then the pulse shrinking time from stage ***n-1*** to stage ***n*** can be analyzed as $t_{PLH1} - t_{PHL1}$:

$$\Delta W_{n-1} = C_{L_n}\left(\frac{1}{k_{P_{n-1}}} - \frac{1}{k_{N_{n-1}}}\right)\times \left[\frac{2V_{TN}}{(V_{DD}-V_{TN})^2} + \frac{1}{(V_{DD}-V_{TN})}\ln\left(\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right)\right] \quad (3)$$

Similarly, the pulse shrinking time from stage ***n*** to stage ***n+1*** can be analyzed as $t_{PHL2} - t_{PLH2}$:

$$\Delta W_n = -C_{L_{n+1}}\left(\frac{1}{k_{P_n}} - \frac{1}{k_{N_n}}\right)\times \left[\frac{2V_{TN}}{(V_{DD}-V_{TN})^2} + \frac{1}{(V_{DD}-V_{TN})}\ln\left(\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right)\right] \quad (4)$$

Since the width of the ***n***-th NOT gate is the β times of those of the remaining NOT gates, we have $k_{N_n} = \beta k_{N_{n-1}}$,

$k_{P_n} = \beta k_{P_{n-1}}$, and $C_{L_n} = \beta C_{L_{n+1}} = \beta C_{L_{n-1}}$. The total pulse shrinking time can be found by adding (3) and (4):

$$\Delta W = (\beta - \frac{1}{\beta}) C_{L_{n-1}} (\frac{1}{k_{P_{n-1}}} - \frac{1}{k_{N_{n-1}}}) \partial_i \quad (5)$$

where $\partial_i = \frac{2V_{TN}}{(V_{DD}-V_{TN})^2} + \frac{1}{(V_{DD}-V_{TN})} \ln\left(\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right)$ is a constant factor which is more or less layout independent. If the delay line is homogeneous for β=1, the pulse shrinking time will be zero, quite reasonably, from (5). On the other hand, the input pulse will be shrunk or expanded for $\beta \neq 1$. To confirm the derivation, the simulated results for different β values are shown in Fig. 7. The device sizes used for β=1 are 3μm/1μm for p-MOS, and 1μm/1μm for n-MOS. For higher order analysis, many important factors must be taken into consideration, such as: exponential-decay-like input pulse, the impedance reflection of the following stages, and the dependence of threshold voltage on the device geometry (or layout equivalent) ... , etc.

In reality, there are two NAND gates in the cyclic delay line implemented in Fig. 5. The induction is far more complicated, but the input pulse still undergoes different rising and falling time at the interface boundaries around the inhomogeneous gates. In reality, no mater how many inhomogeneous gates reside in the delay line, the pulse-shrinking machanism will work all the same.

For the last few cycles, the input pulse will become too narrow to make the counter toggle its states. A big offset error will occur for TDC measurements when the pulse shrinking time per cycle is relatively small. However, the offset error can be perfectly eliminated by carefully calibrated measurement processes. Assume the TDC output codes are N and N' for the reference period T_{ref} and twice of the reference period $2T_{ref}$ (by dividing the reference clock of T_{ref} by 2) respectively. Then

$$T_{ref} = \alpha N + T_{offset} \quad \text{and}$$
$$2T_{ref} = \alpha N' + T_{offset}$$

Where α is the effective resolution, and T_{offset} is the measurement offset. We have

$$\alpha = \frac{T_{ref}}{N'-N}$$
$$T_{offset} = \frac{N'-2N}{N'-N} T_{ref}$$

With α and T_{offset}, the measured width of an input pulse T_{in} with output code n can be calculated:

$$T_{in} = \alpha \times n + T_{offset} = \frac{n+N'-2N}{N'-N} T_{ref} \quad (6)$$

The above calibration technique can also be used to compensate the error caused by supply voltage or temperature variations. If necessary, the calibration can be redone just before any measurement to ensure the best accuracy.

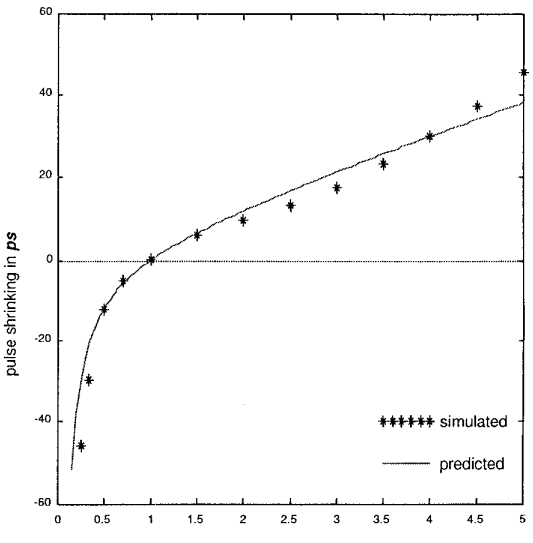

Fig. 7

Measured Results

The new TDC has been fabricated by a standard 0.35-μm SPDM CMOS process. The cyclic delay line is composed of 43 buffers and a pulse-shrinking delay element. The aspect ratios are 12μm/1μm, 8μm/1μm for p-MOS and n-MOS transistors in NAND gates; 6μm/1μm, 2μm/1μm for p-MOS and n-MOS transistors in buffers. The photomicrograph of the new TDC is shown in Fig. 8. The size of the circuit is 0.35 mm × 0.09 mm only, excluding the I/O pads. The static dissipation current, including the I/O pads, is 0.3 uA only. The average current consumption is measured to be 370 uA under measurement rate 100 k/sec, output code 200(the ratio of operation time over idle time is 3.8 us/6.2 us), and a single 3.3V supply.

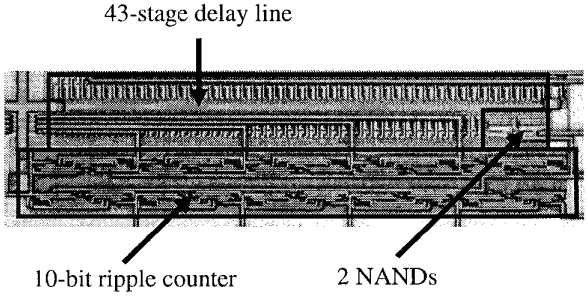

Fig. 8

To find out the effective resolution and the measurement offset of the new TDC, a series of pulses with different width were sent to this TDC for coding. The same input pulses were also measured with a Standford Research Systems SR620 universal counter and a Tektronix TDS680B real-time digital oscilloscope. The measured

results of single-shots along with the theoretical prediction line are depicted in Fig. 9. Due to the implemented TDC with a short delay line of 43 buffers only, the output code is limited around 200. The valid output code range can be further increased by enlarging the delay line of the implemented TDCs. It can be seen that the experimental data agrees with the prediction very well. From (6), the effective resolution α and the measurement offset T_{offset} are calculated to be 68 *ps* and 1.86 *ns* respectively. Fig. 10 shows the error between the single-shot measurements and the theoretical calculation. All the single-shot errors are less than 1 LSB width. In practice, the TDC with cyclic delay line structure possesses perfect linearity. It is reasonable to believe that the errors, corresponding to such deep subnanosecond resolution, may be mostly induced by the jitter effect of the pulse generator and the inherent measurement error of the universal counter. The dead time of the single-shot measurements is at most a few microseconds, depending on the width of the measured pulse. A measurement rate of 100kHz at least is promised.

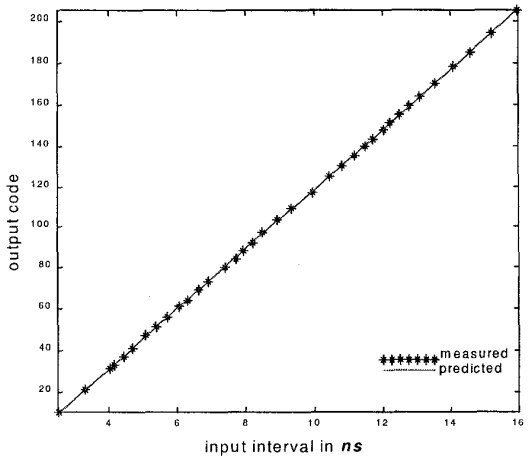

Fig. 9

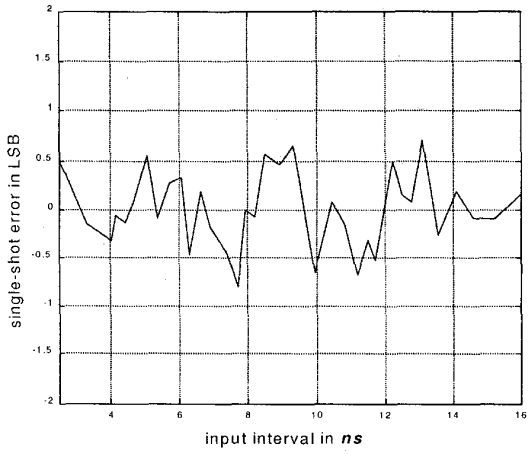

Fig. 10

Conclusions

An extremely low-powered and highly accurate cyclic CMOS time-to-digital converter without biasing circuit has been presented. Being fabricated in a 0.35-μm SPDM process, this new TDC with only 43 delay line buffers can measure input interval up to 19 *ns* and reach an exceedingly fine resolution of 68 *ps* by experiments. If the TDC is used to measure longer input interval directly, it simply needs to increase the number of buffer stages in the cyclic delay line proportionally. Only when the induced long dead time causes problems, can this TDC be considered to act as an interpolator and cooperate with the counter method to greatly increase the linear measurement range [8]. No bias adjustment or continuous calibration is needed. This enables the TDC to be shunt down between measurements to save more system power. With its extreme simplicity, miniature size, and fine resolution, the TDC is the best candidate for highly accurate portable applications.

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