5.5V Tolerant I/O in a 2.5V 0.25μm CMOS Technology

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Abstract

Robust high-voltage tolerant I/O that do not need process options is presented, demonstrated on 5.5V tolerant open-drain I/O in a 2.5V 0.25μm CMOS technology. Circuit techniques limit oxide stress and hot-carrier degradation, resulting in hundreds of years extrapolated lifetime for 5.5V pad voltage swing, 2.2V supply voltage, 10MHz switching frequency. The shown concepts are also implemented in other types of I/O and can easily be scaled towards newer processes.

Introduction

With newer CMOS generations transistors get smaller and the nominal supply voltage decreases (1) in order to increase the performance (speed) while reducing the cost (area and power consumption). Simultaneously the maximum *tolerable* voltage across transistor terminals decreases (2-3) to limit transistor degradation due to hot-carriers and high oxide-fields.

For compatibility with standardized protocols or with ICs from previous generations a large number of chips in advanced CMOS processes must be able to interface at voltages higher than their nominal supply voltage. For example 5V interfacing is required for ICs realized in processes with a nominal supply voltage of e.g. 2.5V.

Three approaches can be followed to make high-voltage tolerant I/O. All these approaches aim at reliably handling high-voltages, e.g. while ensuring sufficient lifetime, in a CMOS generation with a significantly lower nominal supply voltage. Firstly technological solutions can be pursued (e.g. multiple gate-oxides (1,4) or extended drain devices) which yield high-voltage tolerant transistors at the cost of a more expensive process: masks and processing steps must be added to the baseline process. Secondly extended-drain devices in baseline CMOS technology (5) can be used; for these high-voltage tolerant transistors no process options are used but the performance-per-area is relatively poor compared to baseline transistors. Thirdly, solutions using only baseline transistors can be pursued: innovative circuit solutions are used to achieve high-voltage tolerance. With this type of high-voltage tolerance the voltages across all transistors' terminals are limited to sufficiently low values for the baseline transistors.

This paper describes a 5.5V tolerant I/O circuit in a standard 0.25μm 2.5V CMOS process without the need for process options, hence using only standard transistors.

Lifetime threats

Three effects limit lifetime of MOS transistors. Firstly the electrical field across the gate-oxide must be limited to about 5.5MV/cm (2) which typically corresponds to a tolerable oxide voltage 20% higher than the process's nominal supply voltage. Secondly hot-carrier degradation must be sufficiently small. This effect depends on among others the transistor's length and its biasing conditions. A typical hot-carrier-based lifetime versus biasing plot is given in Fig. 1. Note that especially the drain-source voltage of a MOS transistor strongly affects the lifetime. A third lifetime threat is junction breakdown. For modern CMOS processes this junction breakdown occurs at voltages of at least a few times the nominal supply voltage and is therefore not a real concern for circuits that should operate at voltages up to roughly 2.5 times the nominal supply voltage.

In the presented high-voltage I/O, high oxide fields and hot-carriers are limited using only circuit techniques, hence without the need for process options. The junction breakdown voltage is a boundary condition: the tolerable pad voltages can never (reliably) exceed the drain-bulk breakdown voltage. Note that in triple-well processes junction breakdown is less of an issue if the well-voltages are properly controlled.

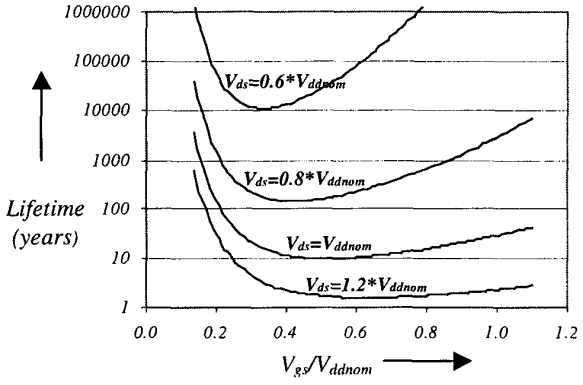

Fig. 1 Channel-hot-carrier lifetime as a function of V_{ds} and V_{gs} (typical behavior for 0.25μm CMOS)

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High voltage I/O: open drain output

The high-voltage I/O circuits without process options, described in literature, can typically handle up to 1.8 times the nominal supply voltage (6,7). These circuits use a single cascode to limit the voltage across the transistor's terminals. Fig. 2a shows such a high-voltage tolerant open-drain output driver; the open-drain configuration is used in this paper for illustration purposes. Note that an open-drain circuit needs an external pull-up resistance and typically has a significant capacitive load (e.g. the ESD and pad capacitance).

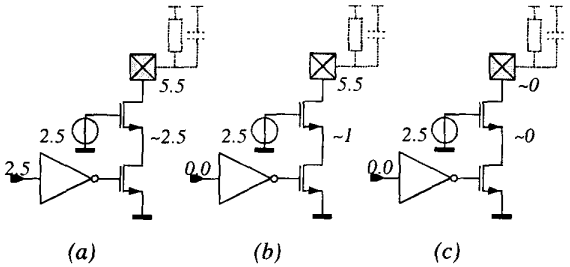

Fig. 2 Single-cascode open-drain output circuit: (a) in steady-state high (b) in transient high-to-low (c) in steady-state low

The voltages in Figs. 2a to 2c correspond to conditions for which the maximum pad-voltage exceeds twice the nominal supply voltage for the process. In steady-state high, see Fig. 2a, the oxide fields in all transistors are sufficiently small and there is no hot-carrier degradation because the transistors are 'off'. If the output of the I/O is steady-state low, see Fig. 2c, clearly all oxide fields and the hot-carrier degradation are sufficiently small for a 2.5V CMOS technology. However, in a transient from the 'high-state' to the 'low-state', see Fig. 2b, the lower transistor is switched 'on' and consequently also the cascode transistor is switched 'on' by pulling its source down. As a result the drain-source voltage of the cascode is large during the transient which causes significant hot-carrier degradation, and hence lifetime problems.

Clearly a single-cascode solution cannot be used to build robust 5.5V tolerant I/O circuits in a 2.5V CMOS process: at least a double-cascode solution is needed. An example of a double cascode solution is given in Fig. 3a. In this circuit the gate bias of the upper cascode transistor must be variable in order to limit the oxide-field in that transistor in at least one of the steady states. There are two demands on the variable source for the upper cascode transistor: the voltage must in some way "*track*" the pad voltage *very fast* (both tracking and the high speed are required for lifetime reasons) and the voltage must be *lower bound* (for proper operation of the I/O in steady-state-low mode).

A circuit implementation of the variable voltage source to bias the upper cascode transistor is shown in Fig. 3b.

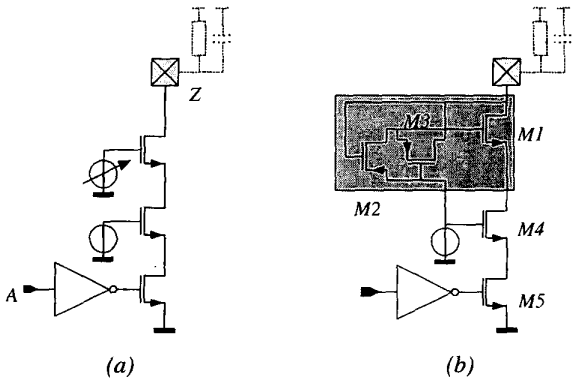

Fig. 3 Double-cascode open-drain output circuit
(a) principle circuit (b) circuit implementation

With this circuit, if the output is steady state 'high', the upper cascode transistor M1 is switched as MOS-diode (by M3), see Fig. 4a for the approximate voltages in this state. In steady-state high a small current flows through M1 because of, among others, leakage though M4 and because of (weak-avalanche) currents in drain-bulk and source-bulk junctions. With the body-effect of M1 the voltage shift created by M1 can exceed 1V in modern CMOS processes.

If the output is 'low' (steady state) the two cascode transistors M1 and M4 are biased identically, M1 via M2. Hence in steady-state 'low' operation transistors M1 and M4 together act as one cascode transistor, see Fig. 4c.

In transients between steady states the very short control loop for the upper cascode's gate voltage ensures a timely and smooth transition between the steady-state modi of operation. In the transient from high-to-low the sources of M1 and M4 are pulled down by about the same voltage thereby ensuring sufficient lifetime for M4. Due to the diode-configuration of M1 (for pad voltages higher than the supply voltage) also for this transistor the lifetime is assured. This situation is shown in Fig. 4b.

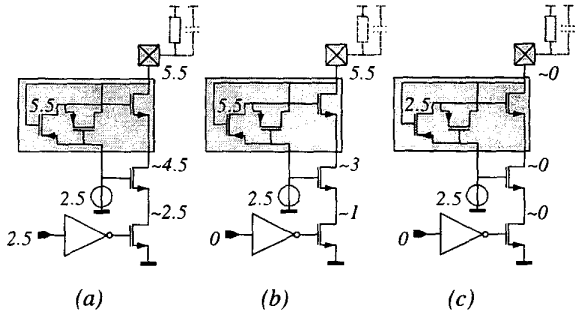

Fig. 4 Double-cascode open-drain output circuit: (a) in steady-state high (b) in transient high-to-low (c) in steady-state low

With the circuit in Fig. 3b and Fig. 4, voltages up to 5.5V can reliably be handled in a chip realized in a baseline 2.5V CMOS process, running at 2.5V. If tolerance to even higher voltages is required, or for 5.5V tolerance at lower supply voltages, circuit blocks consisting of M1-M2-M3 can be stacked. The leftmost part of Fig. 5 shows the circuit implementation of a triple-cascode open-drain output driver; this circuit tolerates 6.5V in a baseline 2.5V CMOS process chip running at 2.5V or reliably handles about 5.5V for the same chip operated at 1.8V.

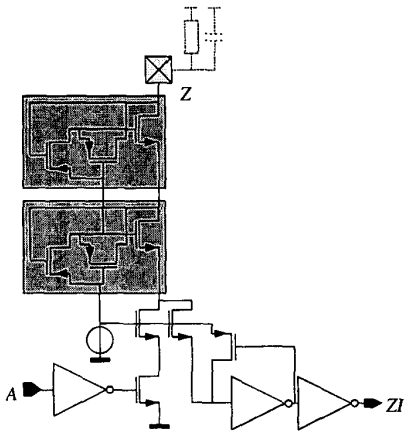

Fig. 5 Robust 5.5V tolerant open-drain I/O in a baseline 0.25um CMOS technology

With the same cascode structure also high-voltage tolerant *input* circuits can be realized, shown on the right hand side of Fig. 5. Note that the cascode blocks are shared for the pad-driver and for the input circuit. The total circuit in Fig. 5 hence implements 5.5V tolerant I/O in base-line 0.25um CMOS technology running at 1.8V supply.

Static power consumption

For a lot of applications, e.g. for battery powered systems, the static power consumption is very important. In the presented circuit, there is no DC current path from the internal supply voltage to ground. Consequently the static power consumption is due to only 'leakage'. In fact, the main static power dissipation in the circuit is due to the total leakage through M3, caused by weak-avalanche currents through junctions and due to ordinary sub-threshold leakage. This leakage typically is in the nA-range at room temperature.

The dynamic power dissipation is mainly due to capacitive charging and discharging of the ESD and pad capacitances. The dynamic power dissipation of the circuit itself is negligibly small compared to the power required for the ESD and pad; it is mainly due to driving M5 in Fig. 3b.

High voltage I/O: push-pull I/O

So far only open-drain I/O was presented. Addition of the complementary output circuit with proper levelshift circuitry yields high-voltage tolerant push-pull I/O, shown in Fig. 6. The block in the right lower corner implements the circuit shown in Fig. 5. Also in the levelshift block driving the upper (P) side of the circuit high voltage tolerance must be ensured which, in our current implementation, is done using the techniques in Fig. 3b.

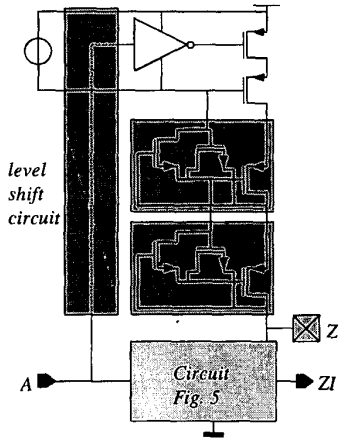

Fig. 6 5.5V tolerant push-pull I/O in baseline 0.25um CMOS

Measurements

Measurements (DC and transient) were done on a number of samples to verify both the functionality and lifetime. As explained earlier, degradation of high-voltage I/O is maximal in transients between states; therefore lifetime estimations are based on degradation-data obtained at maximum switching frequency of the I/O circuit.

Fig. 7 shows measured behavior of the 5.5V-tolerant open-drain output circuit. The RC-timeconstant of the pull-up resistor and the load capacitance (ESD-, pad- and probe capacitance) determines the rising edge of the output signal.

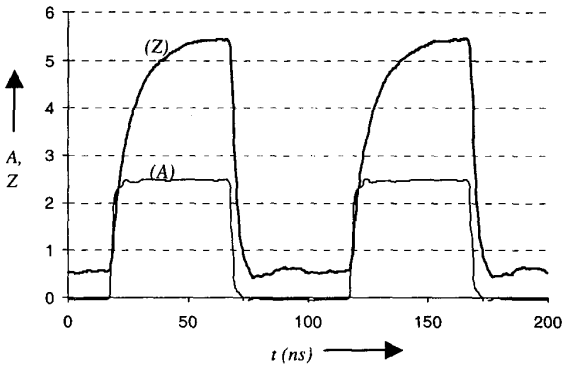

Fig. 7 Measured behavior of the 5.5V tolerant open-drain output

For illustration purposes this external pull-up resistor was relatively low ohmic which results in a relatively high voltage in the 'low' state. Note that the I/O itself and the capacitive load determine the falling edge.

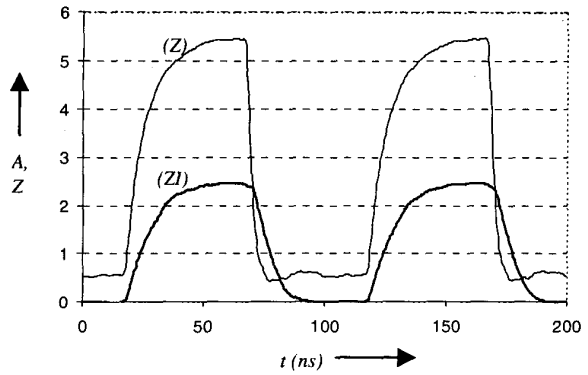

Fig. 8 Measured behavior of the 5.5V tolerant input

Fig. 8 shows the behavior for the input part of the I/O, operating on the output signal created by the I/O itself. The input circuit was designed to drive internal loads only. For these measurements the input circuit had to drive a pad and an external probe; this relatively large capacitive load limits the steepness of the edges of the ZI-signal.

For lifetime measurements the maximum pad-voltage was 7.5V, the supply voltage was 1.5V. Taking into account the enhanced transistor degradation-speed for this circuit at these conditions the lifetime is extrapolated to be at least hundreds of years under normal worst-case operation conditions (5.5V output swing, 2.2V supply voltage, 10MHz, slow processing, 120 deg C).

Fig. 9 shows a microphotograph of two 5.5V tolerant open-drain I/O circuits in a 0.25µm CMOS technology. Other I/O circuits designed using the presented techniques include slew-rate controlled I/O and push-pull I/O up to 50MHz switching frequency.

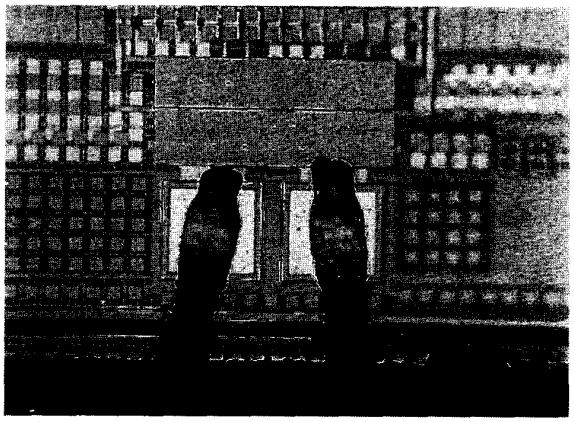

Fig. 9 Chip micrograph of two 5.5V tolerant I/O circuits in baseline 0.25µm CMOS technology

Acknowledgment

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