Integrated VCO Design for MICS Transceivers

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Abstract— **The 402-405 MHz MICS (Medical Implant Communication Service) band has recently been allocated by the US Federal Communication Commissions (FCC) with the potential to replace the low frequency inductive coupling techniques in implantable devices. This paper investigates the designs of VCO (Voltage Controlled Oscillator) architectures that will be essential building blocks of such wireless implantable devices. Three different integrated quadrature VCOs that meet the requirements of the MICS standard are designed in 0.18 µm TSMC CMOS process to propose an optimum choice. The fabricated VCO's are a four stage differential ring VCO, an LC tank VCO directly loaded with a poly-phase filter and an 800 MHz LC tank VCO with a high frequency master-slave divider. All three architectures target a VCO gain of *Kvco* = 15 MHz/V with 3 calibration control and 2 FSK (Frequency-Shift Keying) control signals and are designed for 1.5 V supply voltage.**

I. INTRODUCTION

Design of implantable miniature devices to record or to transmit real-time physiological parameters (e.g. ECG, EEG, EOG, EMG, Neural, Blood Flow, Blood Pressure etc.) from a patient body in medical environments is becoming very important research area. FCC has recently allocated a new band at 402-405 MHz with 300 KHz channels to enable the wireless communication of such implantable devices to deliver high level of comfort, mobility and better patient care [1][2]. With the advance of radio frequency IC (RFIC) technology, this frequency band promises full integration (comparing to inductive link designs) which results in miniaturization and low-power consumption. It provides faster data transfer and increases the communication range. The availability of the 402-405 MHZ band internationally thus offers us an attractive frequency choice for future medical implant devices.

Recently, some low power CMOS transceivers, working at 433 MHz and 435 MHz bands, have been reported [4][5]. These designs achieve low power operation, leaving the matching networks or voltage-controlled oscillator (VCO) tank inductor off-chip. The VCOs presented in this paper are designed for a fully integrated 402-405 MHz direct conversion frequency-shift-keyed (FSK) transceiver. This architecture is selected because of the simple demodulation process of FSK signals when used with an I/Q direct conversion architecture [5][6]. In the transmit mode of this architecture, the PLL loop opens and the base-band digital data directly modulate the VCO with an offset tone of ± Δf = 70 KHz fitting optimally into one of ten 300 KHz channels. The detailed specifications of this architecture were discussed in [6].

II. PLL ARCHITECTURE

The block diagram of the PLL architecture proposed for the targeted application is shown in Fig. 1. A fractional-N PLL

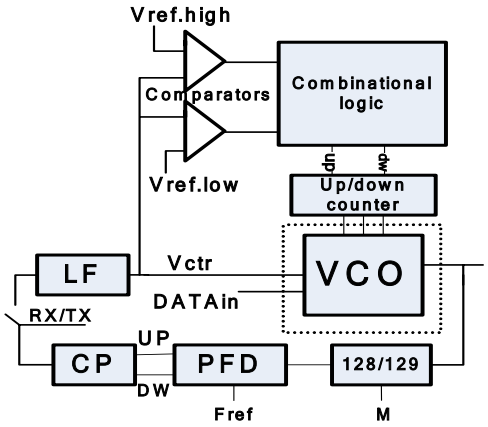

Fig. 1. Block diagram of the PLL with calibration for an MICS transceiver.

with 128/129 division ratio is considered with a reference oscillator of ~3.14 MHz to cover the whole 3-MHz available band in MICS (402-405 MHz). All of the VCO's designed here employ the direct modulation where the base-band data arrange the frequency tones of FSK signals in the transmit mode. In order to minimize the center frequency variations in the transmit mode, the VCO gain is kept very low. This reduces the susceptibility of the oscillation frequency to the noise on the control voltage. However, having a narrow tuning range might leave the VCO frequency out of the desired band, considering the effect of process variations. To prevent this to happen, a second static calibration loop is utilized to maintain the VCO frequency in the desired frequency range.

Two comparators track the control voltage and step the VCO frequency up or down with three-bit resolution, in case the control voltage exceeds the predefined limits. An 8 overlapping frequency clusters are arranged via the available tuning range while still keeping the VCO gain low in every cluster. Overlapping regions between the clusters is kept large enough to prevent unstable switching among the clusters due to noise and temperature variations. Moreover, by setting the thresholds of these comparators properly, the VCO is easily kept in the linear regions of its total tuning range.

The phase noise requirement of a VCO for the targeted application (i.e. MICS regulation) is quite relaxed. Because of the fixed distance and upper bound on the radiated power (i.e. EIPR), the dynamic range is not too high (set by the path loss in 2m, ~30 dB [2]). For this reason, the down conversion of the noise in the adjacent channel due to the phase noise of the oscillator is not very serious. Assuming a signal-to-noise ratio (SNR) of 10 dB due the next channel, the phase noise requirement of the VCO can be given by [6]

$$L(160\text{KHz}) = -30 - 10 - 10\log 20k = -83 \text{ dBc/Hz} \quad (1)$$

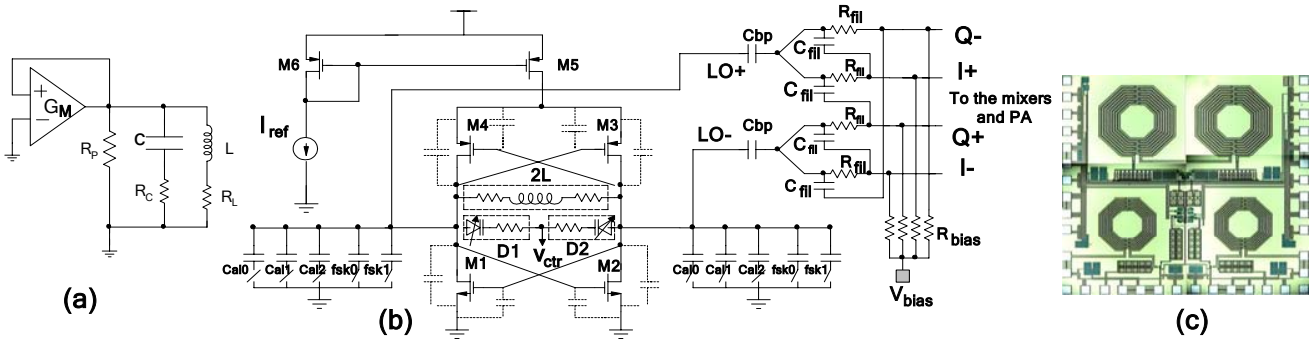

Fig. 2. LC tank VCO directly loaded with poly-phase filter, (a) basic LC-tank oscillator configuration with tank parasitics, (b) schematic of theVCO, (c) the microphotograph of the VCO directly loaded with a poly-phase filter and a two stage power amplifier.

where the transmission data rate is selected 20 kb/s to cover the majority of physiological signals [3][4][6]. All of the different VCOs presented in the following sections were designed for the same specifications described so far, targeting the minimum power consumption with 3-bit calibration control (~15 MHz/V VCO gain in every cluster) and 2-bit FSK control (± Δf = 70 kHz to 80 KHz). They are followed by the same two-stage single-ended power amplifier carefully sized to deliver around -7 dBm power to a 50-Ω antenna with an integrated 13.9-nH RF-choke spiral inductor and 9-pF by-pass capacitors (MIM). This output stage consumes 2.2 mA current from a 1.5 V supply.

III. A 400 MHz LC Tank VCO Directly Loaded With a Poly-Phase Filter

A poly-phase filter loaded with 400 MHz LC tank VCO is designed (Fig.2). Using a poly-phase filter to generate quadrature phases is a popular approach for low power, I-Q mismatch tolerant applications. A topology that uses nMOS – pMOS cross coupled pairs with pMOS tail current source was chosen for the core VCO design. Using both nMOS and pMOS pair gives double amplification for a given current. In addition, this circuit is optimized to have more symmetry in the output waveform leading to a further phase noise reduction. Due to its lower flicker noise pMOS transistor was used as a tail current source.

In order to reduce the phase noise we used large oscillation amplitude with large inductors having very low resistive losses. This is a efficient way of reducing the phase noise. An 8-turn 22.4 nH spiral inductor with a trace width of w=12 µm and gap of s =1.5 µm is used for this design. Only top metal layer (metal6) was used for the spirals which results in a total series resistance of *Rind* =20 Ω at 400 MHz. The quality factor of this inductor at 400 MHz is 5.2. The total tank capacitance corresponding to this inductance value is C_{tot}=7.07 pF. This total capacitance represents all the parasitic capacitances associated with the FET's, capacitive loading due to poly-phase filter, 3-bit binary weighted MIM-Caps for calibration, and varactor diodes for tuning. Moreover, two switchable 7-fF metal2-metal3 capacitors were used for FSK modulation. The basic configuration for an LC tank oscillator is given in Fig.2-(a). The transconductance required to satisfy the unity loop gain at the oscillation frequency is 6.5 mS for this design [9].

The VCO is directly loaded with a single stage poly-phase filter as shown in Fig.2-(b) (only single stage is used to limit the filter loss). R_{fil} and C_{fil} were chosen very carefully to maximize the filter input impedance while keeping capacitance value large enough compared to total parasitic capacitance in order not to deteriorate the I-Q mismatch. The total input capacitance of mixer and power amplifier driver together with the parasitic capacitance of the poly-resistors to substrate is around 38 fF in the design. Thus, C_{fil} was chosen to be 132.7 Ff (four times bigger than total parasitic capacitance) which would lead to a resistor value of R_{fil} = 3 kΩ. The capacitive part of the filter impedance is absorbed into the total tank capacitance to generate 400 MHz center frequency.

The design has been fabricated in 0.18 µm *TSMC* CMOS process. The total die area including the bonding pads, a fully integrated power amplifier with the RF choke coil and the by-pass capacitors is 1.2 mm x 1.2 mm (Fig. 2-(c)). LLP-40 leadless 40-pin RF package is used for the measurements. The oscillator can sustain the oscillation with a current as low as 800 µA. The measured spectrum and the tuning characteristics are shown in Fig. 3. The desired tuning characteristics were obtained with a total tuning range of 90 MHz spread into 3-bit controlled 8 clusters. The VCO gain inside every cluster is around 15 MHz/V as expected. The phase noise measurement is done with Agilent E5052A. The phase noise at an offset of 160 kHz is -98 dBc/Hz, which is way below the prerequisite value for the application. The phase noise plot is shown in Fig.4-(a). Fig.4-(b) shows the phase noise values at the offsets of interest for various power levels.

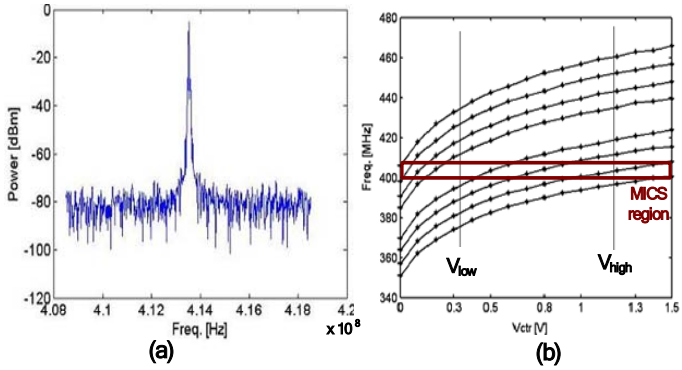

Fig. 3 (a) The measured spectrum of the VCO with poly-phase filter, (b) the measured tuning characteristics of this VCO.

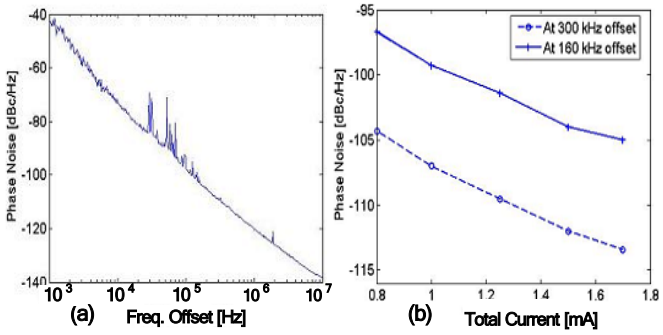

Fig. 4 (a) The measured phase noise of the VCO with poly-phase filter, (b) phase noise for various VCO core current levels.

IV. An 800 MHz LC Tank VCO with a Master-Slave Divider

Another way to generate quadrature signals is to use a master-slave divide-by-2 circuit following a VCO operating at double frequency. An 800 MHz LC tank VCO with an analog master-slave divider is designed for MICS band frequencies. The divider outputs drive the same mixer and power amplifier load as in the case of the first design. Since the fast analog D-flip-flops of the divider circuit need to be driven with high swing inputs, a VCO topology with only nMOS cross coupled pair is used to have a higher swing at the oscillator output. The circuit schematic of the design including the divider is shown in Fig. 5. Two 13.69-nH spiral inductors with 7 turns are used for this 800-MHz LC tank. The top metal (metal6) with conductor width w=9 µm and conductor spacing s=1.5 µm yields a series resistance of 13 Ω. Q factor for this inductor is around 4.2 at the frequency of 800 MHz. The total of 2.89 pF tank capacitance includes varactor diode capacitances, 3-bit binary weighted switchable MIM-caps, parasitic gate-source and drain-source capacitances of the cross coupled nMOS pair and the parasitic input gate capacitance of the divider circuit. Two 5-fF metal2-meatl3 capacitances are used for direct FSK modulation by the baseband binary data. The total effective series resistance of the tank was estimated to be 16 Ω with an additional up to 3-Ω varactor series resistance.

A very common topology shown in Fig. 5-(b) was used for fast divide-by-2 operation. In this design M3 and M4 would not allow a large voltage drop at the drains of M1 and M2,

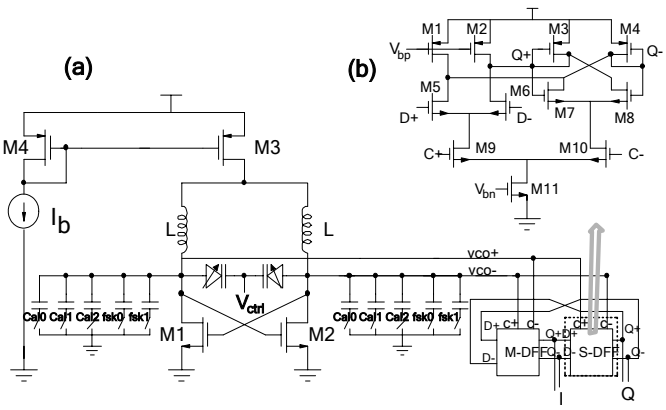

Fig. 5. The schematic for 800 MHz VCO with master-slave divider.

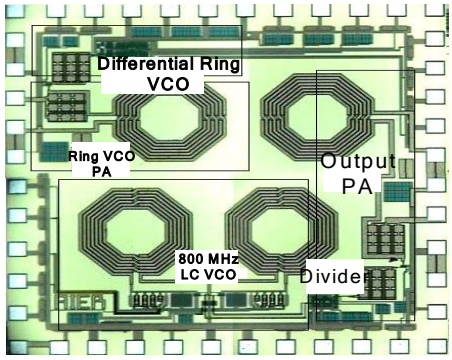

Fig. 6. The microphotograph of the chip including an 800 MHz LC tank VCO with dividers and a four stage differential ring VCO.

which otherwise would push M11 into triode region in case of a large VCO output driving this stage, particularly in the case of a low supply voltage [10]. The divider circuit can directly drive the mixers and the PA consuming 400 µA from a 1.5-V supply.

The design has been fabricated in 0.18 µm *TSMC* CMOS process. The total die area including the bonding pads, a fully integrated power amplifier with the RF choke coil, and the by-pass capacitors is 1.1 mm x 1.2 mm (Fig.6). The upper left corner of the die accommodates a four stage differential ring VCO with the driving buffers and the PA, which will be described in the next section. The VCO core and the divider circuit consume 2.2 mA from a 1.5-V supply. The measured tuning characteristic of the design is shown in Fig. 7-(a). The desired tuning characteristics were obtained with a total tuning range of 70 MHz spread into 3-bit controlled 8 clusters. The linear tuning region of this VCO is much less compared to linear tuning range of the 400 MHz design. However, due to large overlapping margins across the clusters, the comparator thresholds can be set accordingly to keep the VCO in the linear part of the tuning curve as shown in Fig. 7. The VCO gain inside every cluster is around 17 MHz/V. The FSK control bits in this case caused 120-kHz tones around the center frequency. The measured phase noise plot is shown in Fig. 7-(b). The phase noise at an offset of 160 kHz is -97.7 dBc/Hz, a value that is very close to the -98 dBc/Hz value obtained from the previous design.

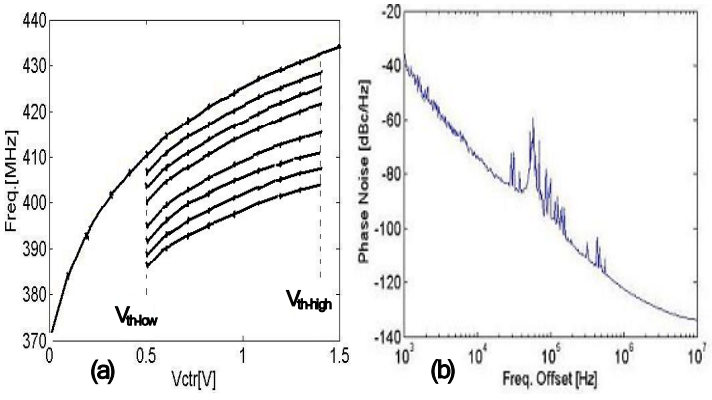

Fig. 7. (a) The tuning characteristic of 800 MHz oscillator followed by a divider, (b) the phase noise of 800 MHz oscillator followed by a divider.

V. A Four Stage Differential Ring VCO

Since the phase noise requirement of the application is relatively relaxed, a four stage differential ring VCO is also designed as a low power alternative to LC tank VCO's. There is no extra step to generate the quadrature outputs in the case of this four stage ring VCO. The design is laid out on one corner of the die with 800 MHz VCO given in Fig. 6. The area of the design, most of which is occupied by the on chip inductor of the PA, is considerably less compared to the LC tank VCO's. The same PA and mixer loads as in the case of LC tank designs are driven by the differential buffers following the ring VCO circuit in the chip.

Ring oscillators are generally avoided in communication circuit applications due to their poor phase noise and linearity performance relative to LC tank oscillators. However, some researchers have investigated the ways to improve the phase noise and linearity of the ring VCO's [11]. In this design, a four stage differential VCO was optimized to achieve the desired tuning and FSK modulation characteristics satisfying the phase noise requirement (-83dBc/Hz at 160 kHz offset). The schematic of the design including an individual delay element is shown in Fig. 8. Every delay cell in this VCO gets three bit calibration control and two bit FSK control signals. These two bit FSK data turn long channel devices M11 and M12 on and off, causing the total sink current change in slight amounts such that frequency deviations will be around 80 kHz. The delay cell topology proposed in [11] is modified to have additional calibration and FSK control. This topology is particularly suitable for the application due to two main reasons. First, one can obtain a very low VCO gain, *Kvco,* by properly sizing the devices M5 and M6 relative to the devices M3 and M4. Second, the tuning devices M5 and M6 would stay in saturation even for very small control voltage levels.

The circuit was optimized in simulations to obtain -82 dBc/Hz phase noise at a 160 kHz offset. *Spectre* was used for phase noise optimization. The simulated current consumption of the VCO core including the differential buffers was 700 µA from a 1.5-V supply. The measured spectrum and the tuning characteristic of the ring VCO are shown in Fig 9.

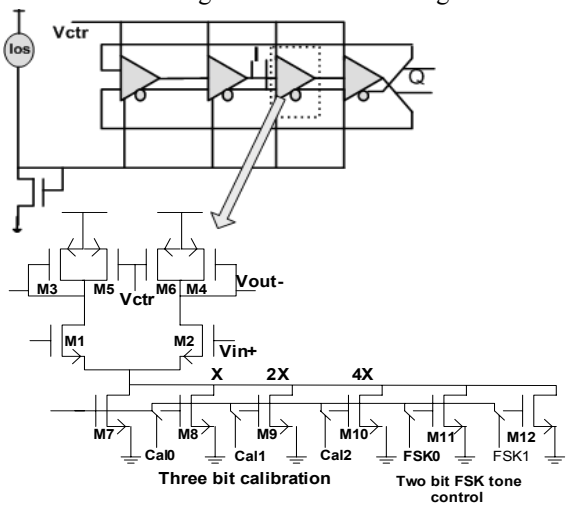

Fig. 8. The schematic of the four stage differential ring VCO.

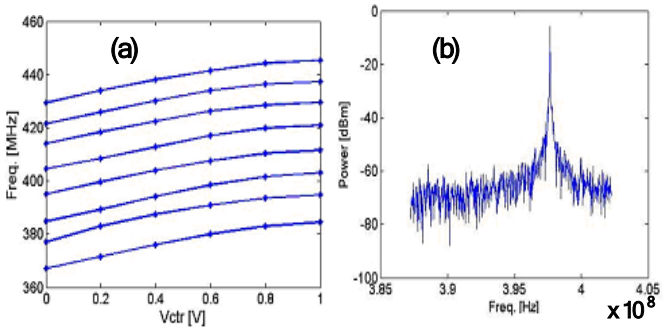

Fig. 9. (a) The tuning characteristic and (b) the measured spectrum of the four stage differential ring VCO.

VI. Comparison and Conclusion

Three different fully integrated VCO's including the driving buffers and the power amplifiers are designed, fabricated and measured using 0.18 µm TSMC CMOS to evaluate the best option for an MICS band transceiver operating at the new 402-405 MHz. Although it consumes very low power and occupies very small die area, the poor frequency stability of the ring VCO makes it difficult to obtain a reasonable FSK tone for 300 kHz channel spacing in the MICS band. In addition, the measured phase noise was 5 dB more than the predefined maximum level. The 800 MHz LC tank VCO with master-slave divider achieves almost the same phase noise performance at the expense of approximately twice higher power consumption, compared to the 400 MHz LC tank VCO directly loaded with poly-phase filter. The linearity of the tuning curve of 800 MHz design is worse than the 400 MHz one. In conclusion, a carefully designed 400 MHz LC tank driving a poly-phase filter was proven to be the best option among three designs.

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