Comparative Studies of Common Control Schemes for Reference Tracking and Application of End-point Prediction

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***Abstract*-This paper analyzes the reference tracking behavior of Buck converters using several control schemes including voltage-mode, current-mode and V^2-control from both large-signal and small-signal domains. Loop gains applicable to reference tracking are highlighted, and reference-to-output transfer functions are derived for the cases when end-point prediction (EPP) is applied to enhance the response. A novel V^2-controlled Buck converter with EPP is fabricated. The measured reference tracking response shows 10 times improvement in speed.**

I. Introduction

When dynamic voltage scaling (DVS) is becoming widely used to reduce the power consumption of VLSI circuits [1], power supplies (usually Buck converters) are required to have fast reference tracking speed in response to the step change of reference voltage. However, with so many different control schemes available (especially those with multiple loops from different feedback quantities and paths), most literatures focus on overall loop stability and load transient response; while dynamics of reference tracking are rarely discussed. In fact, in some control schemes, the loop gains applicable to reference tracking can be different from that to load transient.

Similar to the step response of an opamp, the tracking response of a Buck converter can be divided into large-signal (limited by maximum/minimum duty-ratio or output inductor) and small-signal (determined by the 3-dB bandwidth of reference-to-output transfer function) portions. This paper analyzes the following 4 types of control schemes shown in Fig. 1 from both large-signal and small-signal perspectives: (a) voltage-mode with dominant pole compensation (VMDP), (b) voltage-mode with type 3 compensation (VMT3), (c) current-mode control (CMC), and (d) V^2-control [2]. Identical power stages (L=4.7μH, C_o=10μF, R_c=0.1Ω and 1MHz switching frequency) are used for all control schemes for fair comparison. It is found that both VMT3 and CMC can be designed to have fast tracking speed; while VMDP and V^2-control are inherently slow in tracking. Principle of end-point prediction (EPP) [3] is reexamined and appropriately applied to a V^2-controlled Buck converter. The reference-to-output transfer function of the prototype is derived and verified by simulation, and the measurement result confirms the significant speed improvement.

II. Analysis Of Voltage- And Current-Mode Control

A. Voltage-Mode with Type 3 Compensation

VMT3 is widely used for its high crossover frequency (f_{c_LG}) in loop gain. It is around 150kHz in this design example for robust operation. Since there is only 1 feedback loop via the error amplifier, the reference-to-output transfer function, $G_{vr}(s)$, is related to the feedback factor, $b = R_2/(R_1+R_2)$ and loop gain, $T(s)$, as follows [4]:

$$G_{vr}(s) = \frac{\hat{v}_o}{\hat{v}_{ref}} = \frac{1}{b}\frac{T(s)}{1+T(s)}, \quad (1)$$

where $\hat{v}_o$ and $\hat{v}_{ref}$ are the perturbed output voltage and reference voltage, respectively. When sufficient phase margin is used in the design of loop gain, the resulting 3-dB bandwidth of $G_{vr}(s)$ is close to f_{c_LG}. Fig. 2(a) shows simulated tracking response in which the tracking of 480mV is finished in ~15μs. It is also fast in the large-signal domain in the sense that the inductor current profile is close to a triangular shape (straight-up and down) as proposed in [5]. It is because the compensation capacitors are in the pF range, so that error amplifier output, V_c, can move quickly to saturate the duty-ratio.

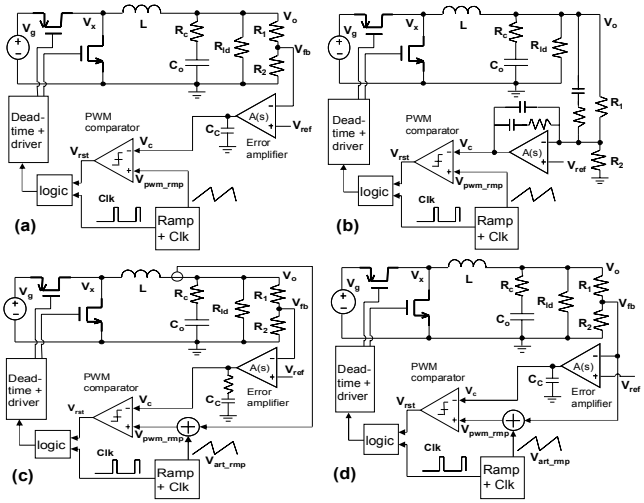

Fig. 1. Common controls for Buck converter: (a) VMDP. (b) VMT3. (c) CMC. (d) V^2-control.

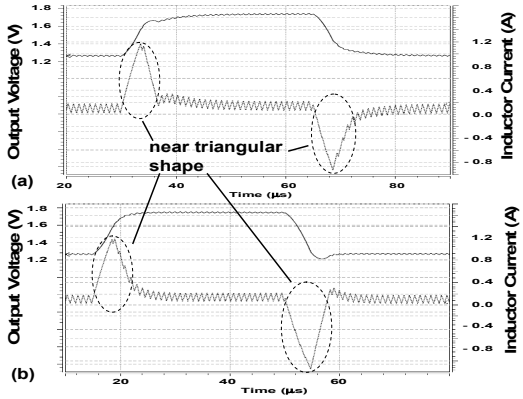

Fig. 2. Simulated reference tracking of Buck converter using (a) type 3 compensator, (b) current-mode control.

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B. Current-Mode Control

Despite the need for a current sensor, CMC has good audio susceptibility and a simplified control-to-output transfer function (mainly a low-frequency pole) [6]. A pole-zero cancellation is used to extend f_{c_LG} to around 150kHz in this design example. Then, $G_{vr}(s)$ for CMC is also given by (1) and the tracking response should be comparable to that of VMT3. Fig. 2(b) verifies the deduction. The large-signal portion is also limited by output inductor rather than V_c due to the small pF range compensation capacitor. It should be noted that loop gain used here is obtained by breaking the loop at V_c [6] rather than at the output of PWM modulator, since reference injection point is at the input of error amplifier.

C. Voltage-Mode with Dominant Pole Compensation

VMDP has the simplest compensation network but its f_{c_LG} has to be much lower than LC pole frequency (23kHz in this design) to maintain stability. A large compensation capacitor C_c in nF range is often used to achieve this; hence the tracking response to a step change in V_{ref} is also slow (in the range of 100μs for a step >300mV). In [3], an EPP scheme is proposed to enhance tracking response (Fig. 3). The idea is to bypass the slow compensation network by feed-forwarding V_{ref} to the PWM modulator. The gain of feed-forward is determined based on the target that error amplifier output, V_a, is essentially unchanged in steady state before and after a step change of V_{ref}. Hence, the change of PWM control voltage, V_c, is mostly contributed by the change of V_{ref} rather than V_a. When V_m (amplitude of ramp signal V_{pwm_rmp}) is set to bV_g, where V_g is the converter input voltage, EPP can be conveniently implemented since the required feed-forward gain is unity.

Fig. 4 shows the small-signal block diagram of VMDP with EPP path in dotted line. $G_{vr}(s)$ for VMDP can then be derived as:

$$G_{vr}(s)=\frac{\hat{v}_o}{\hat{v}_{ref}}=\frac{1}{b}\frac{T(s)}{1+T(s)}\left(1+\frac{1}{A(s)}\right)\approx\frac{1}{b}\frac{T(s)}{1+T(s)}\left(1+\frac{s}{GBW_{A(s)}}\right), \quad (2)$$

where $GBW_{A(s)}$ is the gain-bandwidth of A(s). The approximation can be made since A(s) is a first-order low pass function with high dc gain. It can be seen that EPP effectively adds an LHP zero at $GBW_{A(s)}$ to $G_{vr}(s)$. Since T(s) should be designed to have enough phase margin at f_{c_LG}, T(s)/(1+T(s)) have a 3-dB bandwidth near f_{c_LG}, which is equal to $GBW_{A(s)}$ under the condition of $V_m = bV_g$. Hence, zero introduced by EPP effectively cancels the first pole of T(s)/(1+T(s)), and extends the 3-dB bandwidth to the later poles, which is around the LC pole frequency. The above analytic result expressed in (2) is plotted in Fig. 5, in which the simulated $G_{vr}(s)$ is also plotted and it verifies the correctness of analytical result. The simulated $G_{vr}(s)$ is obtained by using a modified version of the CAD tool presented in [7]. Besides ac simulation, HSPICE transient simulation is also performed. From Fig. 6, it can be seen that the linear settling portion has an envelope of frequency around the LC pole frequency, which is still inferior to the case of VMT3 and CMC. Such a ringing phenomenon happens when there is abrupt change of V_{ref} (<1μs); but not quite noticeable in [3] since the slope of V_{ref} step is gradual (~in range of tens of μs).

For the large-signal portion, since EPP essentially makes a direct jump of duty-ratio from previous steady state to current steady state, duty-ratio is not saturated in the process. This can be seen in the zoomed portion of inductor current in Fig. 6. Inductor current rises up in a seesaw manner rather than a straight-up manner as in the case of saturated duty-ratio for VMT3 and CMC. This forms another speed bottleneck and makes VMDP slower than VMT3 and CMC in tracking speed.

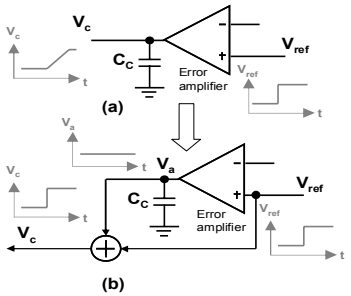

Fig. 3. Implementing end-point prediction (a) original error amplifier (b) adding a feed-forward path from V_{ref}

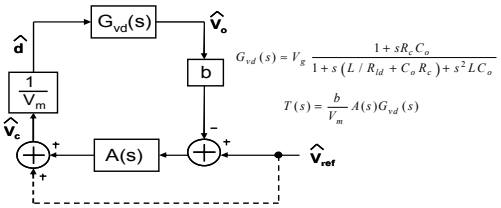

Fig. 4. Small-signal block diagram of VMDP with EPP

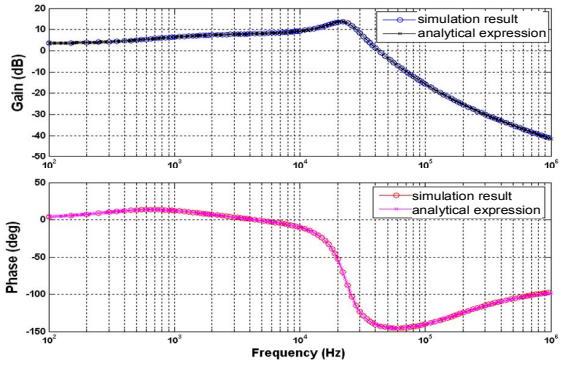

Fig. 5. Reference-to-output transfer function of VMDP with EPP.

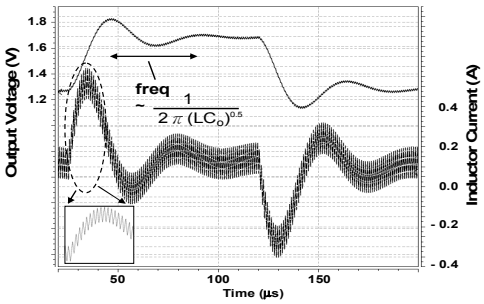

Fig. 6. Simulated reference tracking of VMDP with EPP.

III. Proposed V²-Control With End-Point Prediction

V^2-control is similar to CMC in the sense that it also uses inductor current waveform as ramp (through output capacitor equivalent series resistor, ESR, rather than an explicit current sensor). However, since output voltage is embedded as the DC of ramp signal, it achieves very fast load response due to the easily saturated duty-ratio during load transient. Ref. [2] presents a small-signal model of V^2-control. For clarifying definition of loop gains and relating them to the context of reference tracking, a simplified small-signal model is re-derived here.

Fig. 7 shows the steady state waveform of V^2-control. The ramp signal is centered at bV_o, and an artificial ramp (inverted sawtooth signal) is added for slope compensation when duty-ratio > 0.5 as in CMC. From Fig. 7, the control equation can be written as:

$$v_c = bv_o + \frac{DT_s}{2}\left(bR_c\frac{v_g - v_o}{L}\right) + m_a DT_s\,, \qquad (3)$$

Perturbing (3) gives the following (assuming V_g constant):

$$\hat{v}_c = bK_1\hat{v}_o + K_2\hat{d}\,, \qquad (4)$$

where K_1 and K_2 are given by:

$$K_1 = 1 - \frac{R_c T_s D}{2L} \qquad K_2 = bR_c T_s\frac{v_g - v_o}{2L} + m_a T_s\,. \qquad (5)$$

From (4), a small-signal model shown in Fig. 8 can be constructed. It is consistent with Fig. 3 in [2], with $K_1 \approx 1$ and $1/K_2 \approx F_{m1}$. The sampling effect is not included here as it only affects high frequency (~half switching frequency) accuracy. From Fig. 8, two different loop gains, $T_{vo}(s)$ and $T_{vc}(s)$, can be obtained by breaking the loop at V_o and V_c, respectively:

$$T_{vo}(s) = \frac{b}{K_2}G_{vd}(s)\left(K_1 + A(s)\right), \qquad (6)$$

$$T_{vc}(s) = bA(s)\frac{1}{K_2}\frac{G_{vd}(s)}{1 + bK_1/K_2\left(G_{vd}(s)\right)}\,. \qquad (7)$$

These 2 loop gains can also be expressed as:

$$T_{vo}(s) = T_{fv}(s) + T_{sv}(s) \qquad T_{vc}(s) = \frac{T_{sv}(s)}{1 + T_{fv}(s)}\,, \qquad (8)$$

where fast voltage loop $T_{fv}(s)$ and slow voltage loop $T_{sv}(s)$ are:

$$T_{fv}(s) = b\frac{K_1}{K_2}G_{vd}(s) \qquad T_{sv}(s) = \frac{b}{K_2}G_{vd}(s)A(s)\,. \qquad (9)$$

The difference between $T_{vo}(s)$ and $T_{vc}(s)$ can be seen in Fig. 9. $T_{vo}(s)$ has a much wider crossover frequency than $T_{vc}(s)$. As a result, load transient is much faster than reference tracking since closed-loop output impedance, $Z_{o,cl}(s)$, and reference-to-output transfer function are given by:

$$Z_{o,cl}(s) = \frac{Z_{o,ol}(s)}{1 + T_{vo}(s)} \qquad G_{vr}(s) = \frac{1}{b}\frac{T_{vc}(s)}{1 + T_{vc}(s)}\,, \qquad (10)$$

where $Z_{o,ol}(s)$ is the open-loop output impedance.

Even from the large-signal viewpoint, V^2-control is also slow in tracking speed due to the similar large C_c at the error amplifier output. EPP is proposed here to enhance the tracking speed of V^2 controller. The prediction target is to keep slow error amplifier output unchanged before and after tracking; but the consideration of choosing the gain of feed-forward is different. The change of PWM ramp signal, V_{pwm_rmp}, (see Fig. 1(d)) after tracking would be $b\Delta V_o = \Delta V_{ref}$. For V^2 controller in steady state, PWM modulator "regulates" V_{pwm_rmp} against its control signal, V_c, closely (within tens of mV, see Fig. 7). Such a small difference is overwhelmed by the large $b\Delta V_o$ during tracking so that the required ΔV_c would also be $b\Delta V_o = \Delta V_{ref}$. Hence, the required gain of feed-forward is simply unity (same as the case of VMDP). It should be noted that since amplitude of artificial ramp is small for V^2-control (as it is only used for slope compensation), the above "overwhelming principle" is valid. Moreover, the overwhelming ΔV_{ref} saturates duty-ratio during tracking, so that the inductor current should change in a straight-up-and-down manner during tracking (similar to the cases of VMT3 and CMC).

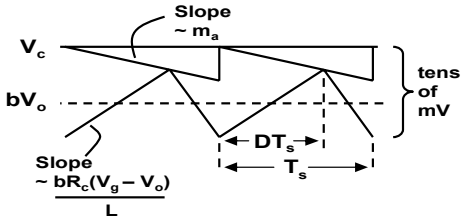

Fig. 7. Steady state waveform of V^2-control.

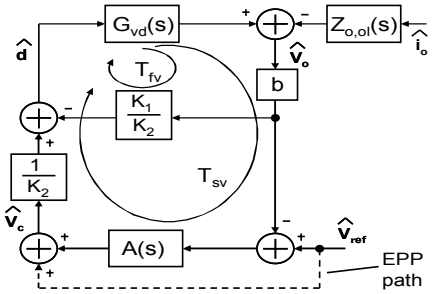

Fig. 8. Small-signal block diagram of V^2-control with EPP.

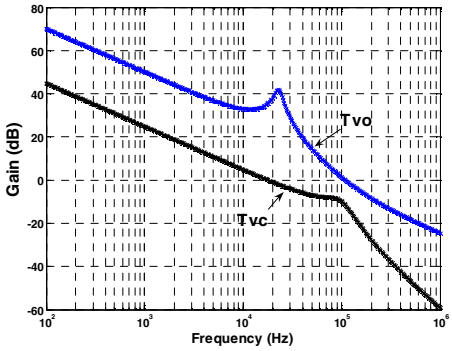

Fig. 9. Two loop gains of V^2-control

The small-signal reference-to-output transfer function of V^2-control with EPP is the same as (10) except that a LHP zero at ~$GBW_{A(s)}$ is added as in the case of VMDP. As mentioned in [2], the control-to-output transfer function (i.e. eq. (7) without the term bA(s)) is flat up to high frequency near half switching frequency. Hence, $T_{vc}(s)$ has crossover frequency near $GBW_{A(s)}$; implying that $T_{vc}(s)/(1+ T_{vc}(s))$ has the first

pole around $GBW_{A(s)}$, which is again cancelled by the EPP-introduced zero. Fig. 10 shows how the bandwidth of $G_{vr}(s)$ is extended by EPP.

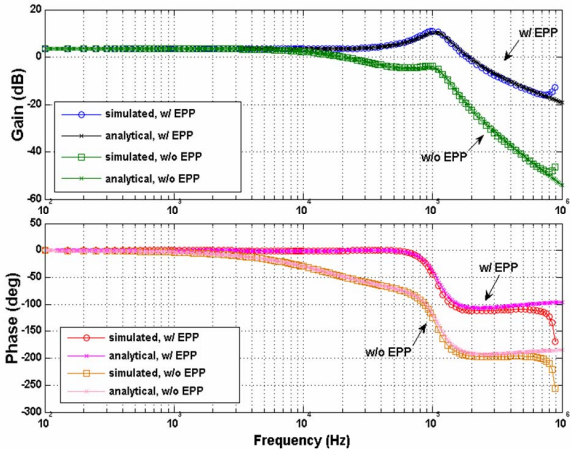

Fig. 10. Reference-to-output transfer function of V^2-control.

IV. Measurement Results

The proposed Buck converter was fabricated in AMS 0.35-µm CMOS process. Fig. 11 shows the die photo of the chip, which has a dimension of 1.65µm x 1.1µm, including pads. Since large negative inductor current is anticipated for fast draining output voltage during reference down-tracking, plenty of well-contacts are added to Power PMOS to reduce the resistance of body diode when reverse current flows through it during the dead-time after Power NMOS is off and before Power PMOS is on. Similar precaution is taken on substrate-contacts of Power NMOS for reference up-tracking and on the current-handling ability of metals.

The power stage uses the same setting as mentioned in section I, with input voltage as 3V (as used in all control schemes analyzed in this paper). Fig. 12 shows the measured reference tracking response of the prototype. With feedback factor b = 2/3, the time needed for tracking a reference step change between 0.84V and 1.16V (equivalent to 480mV change of output voltage) is around 12µs, which is comparable with the simulation results of VMT3 and CMC. It is also noted that the duty-ratio is saturated (indicated by the straight-up-and-down of inductor current) as expected in section III. The linear settling part near the end of tracking period is also very fast (in the order of hundred kHz as expected in section III). Compared with the estimated tracking time of >100µs for conventional V^2-control, the proposed end-point predicted V^2-control achieves a speed improvement of about ten times.

V. Conclusion

In this paper, four common control schemes, namely voltage-mode with type 3 compensation, current-mode control, voltage-mode with dominant pole compensation, and V^2-control are analyzed in both small-signal and large-signal domains for their reference tracking speed. It is found that the former two can be designed with wide loop gain crossover frequency to have fast tracking speed; while the latter two are inherently slow due to the slow compensation network required by stability criteria. End-point prediction is applied to both cases to enhance the tracking speed. A prototype chip of V^2-controlled Buck converter with end-point prediction experimentally proves the ten times tracking speed improvement over the conventional V^2-control. The small-signal reference-to-output transfer function is analytically derived and verified through a Matlab CAD simulator. Two loop gains that are useful in output impedance and tracking consideration, respectively, are highlighted and distinguished from each other.

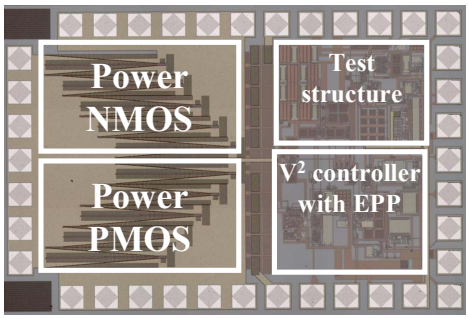

Fig. 11. Die photo of proposed V^2-controlled Buck converter with EPP.

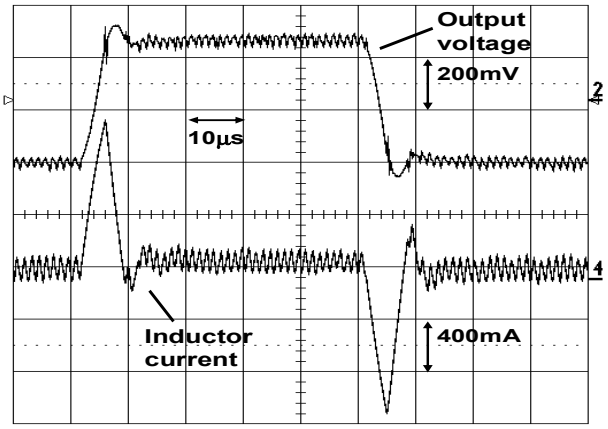

Fig. 12. Measured reference tracking of proposed V^2-control with EPP.

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