A 3.1-8.0 GHz MB-OFDM UWB Transceiver in 0.18µm CMOS

Hui Zheng, Shuzuo Lou, Dongtian Lu, Cheng Shen, Tatfu Chan, and Howard C. Luong

Department of Electronic and Computer Engineering
The Hong Kong University of Science and Technology
Clear Water Bay, Kowloon, Hong Kong

Abstract- **This paper presents a complete CMOS dual-conversion zero-IF2 transceiver for 9-band MB-OFDM UWB systems from 3.1 to 8.0 GHz. The transceiver integrates all building blocks including a variable-gain wideband LNA, a single mixer for both RF down and up conversions in RX and TX, a fast-settling frequency synthesizer, and IQ ADCs and DACs. Fabricated in a standard 0.18-µm CMOS process, the receiver measures maximum S11 of -13dB, maximum NF of 8.25 dB, in-band IIP3 of better than -13.7 dBm, and variable gain from 25.3 to 84.0 dB. IQ path gain and phase mismatch of the receiver chain are measured to be 0.8 dB and 4° respectively. The transmitter achieves a minimum output P-1dB of -8.2 dBm, sideband rejection of better than -42.2 dBc, and LO leakage of smaller than -46.5 dBc.**

I. INTRODUCTION

Driven by an increasing demand of short range and high data rate wireless communications, ultra-wideband (UWB) technology with target data rates up to 480Mb/s within 10-m distance becomes more and more attractive. The UWB system utilizes the unlicensed 3.1 – 10.6 GHz frequency band with a transmit power below the FCC limit of -41.25 dBm/MHz. According to MultiBand OFDM Alliance (MBOA) specification, the UWB spectrum is divided into 14 bands, each with a bandwidth of 528 MHz [1]. Support for the first 3 bands (Band Group 1) shall be mandatory.

All existing MB-OFDM UWB transceiver systems make use of direct-conversion architecture [2]-[4] due to its obvious advantage of having no image problem. However, such architecture would impose stringent requirement on ultra-wideband and high-frequency LO signals with accurate IQ outputs, which would inevitably degrade the synthesizer's performance in terms of power, phase noise, and sideband rejection. To avoid such stringent requirement for wideband LO signals, dual-conversion zero-IF2 architecture with proper frequency plan was adopted for the first 9-band UWB receiver front-end [5]. Such dual-conversion zero-IF receiver architecture can also have much less problems with dc offsets, LO leakage, and frequency pulling.

As significant extension of the receiver front-end reported in [5], this paper presents a single-chip UWB-OFDM transceiver that fully integrates not only the RX and the TX but also a complete analog baseband with the IQ ADCs and DACs. The transceiver meets all the system specifications for the first 9 frequency bands (Band Groups 1, 2 and 3) from 3168 MHz to 7920 MHz.

As illustrated in Fig. 1, the first variable LO1 signal down-converts RF signals to a fixed IF1 frequency at 2.904 GHz, and the second fixed IQ LO2 signals further down-convert the IF1 signals to zero IF2. However, image signals exist during the first-step conversion and need to be rejected. To achieve sufficient image suppression without an image-rejection filter, upper-sideband mixing with LO1 signals from 6.336 GHz to 10.56 GHz is proposed. With such a frequency plan, the image frequency band is located from 9 to 13.7 GHz, which is completely outside of the desired signal band. With proper pre-filtering from the external pre-selection filter and the on-chip LNA, more than 30 dB image rejection can be easily achieved.

As a unique feature of this transceiver, a single RF mixer is proposed for both RF-to-IF1 down conversion in the RX and IF1-RF up conversion in the TX.

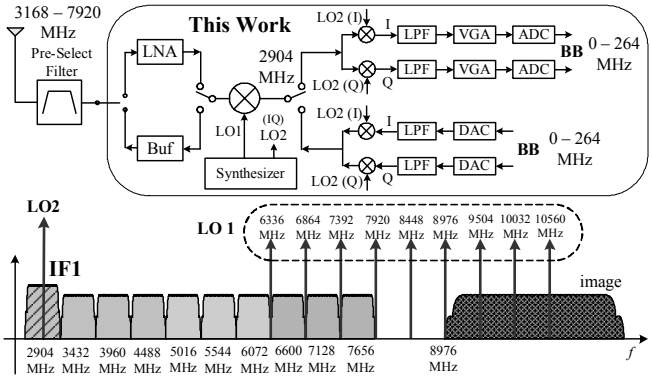


Fig. 1 Proposed dual-conversion zero-IF2 transceiver architecture and frequency plan for LO signals

II. SYSTEM AND BUILDING BLOCKS DESIGN

As proposed by MBOA, an UWB receiver operated in only the first 3 bands (Mode 1 only) needs to have noise figure of better than 6.6 dB. However, for UWB devices operated in the first 9 bands (both Modes 1 and 2), the NF can be relaxed to around 8 dB. The MBOA standard derives the receiver sensitivity requirements ranging from -80.8 dBm (for 53.3 Mb/s) to -70.4 dBm (for 480 Mb/s) at different data rates. To reach the full-scale of the ADC input, the receiver chain is required to deliver a maximum voltage gain of 80 dB. The FCC part 15 limits the transmission output spectral density of an UWB device to -41.25 dBm/MHz. Under fast frequency hopping mode within one band group, the total output power of transmitter is around -9.25 dBm. Assuming a minimum communication distance of 0.2 m, the maximum power received at the antenna is -39.5 dBm. In our proposed

transceiver, a total gain variable range from 25 dB to 84 dB is implemented in the receiver chain to cover the full dynamic of the input signals, out of which 12-dB variable gain is from the LNA and 40-dB variable gain is from the VGA.

The receiver linearity requirement is determined by both in-band and out-of-band interferences. An RF band-pass band-selection filter from 3.1 GHz to 8 GHz is employed in front of the LNA to perform preliminary filtering of out-of-band interference. Further out-of-band filtering is accomplished not only by the LNA but also by a band-pass filter constructed by the LC-tank in first-stage mixer. The channel-selection filtering is done by a low-pass filter before VGA. MBOA standard defines a total of 128 sub-carriers of 4.125 MHz each wherein the 0^{th} sub-carrier at DC is not used. Thereby, AC-coupling capacitors are connected at the output of the 2^{nd}-stage mixer and at the output of the channel-selection low-pass filter with overall corner frequency around 2 MHz to remove dc offset.

Similar to the receiver chain, two-stages filtering is employed at transmitter part to remove the DAC alias and the unwanted spurs to fulfill the transmit mask requirement: a low-pass filter located at DAC output and an LC-tank filter at the output of the second-stage BB-IF1 up-conversion mixer. In addition, the RF band-selection filter at the output also can help to attenuate the out-of-band spurs. The MBOA standard imposes an EVM requirement of -19.5 dB at highest data rate. With an output power of -10 dBm, an output compression point OP-1dB of better than -6dBm is needed for the transmitter to meet the EVM requirement. Moreover, in order for the IQ mismatch to have negligible effect in the EVM, sideband rejection of better than -30 dB should be achieved [2]. Thanks to the low transmit power requirement, a wideband PA can be eliminated. Instead, an output buffer stage is included to achieve both the desired power level and the required output matching.

Since the LNA sets the baseline NF of the receiver, NF of less than 5 dB (including the loss of the off-chip single-end-to-differential balun) is needed. To suppress the noise contribution from the later stages, a 3-stage LNA with maximum gain of larger than 22 dB is designed, which employs T-coil load in the 1^{st} stage and series inductive peaking in the last two stages for wideband operation. Common-gate input at 1^{st} stage together with capacitive coupling at the input is adopted for wideband input matching. On the other hand, variable gain of more than 12 dB is implemented at the 3^{rd} stage by current steering to relax the linearity requirement of the following building blocks when large signals are presented at the LNA input. Detailed design and consideration of the LNA can be found in [5].

A combined mixer is proposed for both RF down-conversion in the RX and for the RF up-conversion in the TX, and its schematic is shown in Fig. 2. Unlike in the conventional Gilbert-type mixer, the LO switches of the combined mixer are moved to the bottom of the transconductors so that they can be shared between the RX and TX. With such a combined mixer configuration, the capacitive loading to the synthesizer's LO1 output is reduced by half. In addition, the LO1 input devices can be laid out very close to the synthesizer output, which minimizes the interconnection between the synthesizer and the mixer so as to further reduce the loading and to avoid a need of power-hungry on-chip buffers. The transconductors and the loads are switched by the controlling signals EN and ENB to enable down-conversion or up-conversion for RX-mode or TX-mode operation one at a time, respectively. On the other hand, in this mixer topology, large voltage swings at source nodes of the gm transistors (Nodes A & B) are required to completely switch the transconductors. Consequently, series peaking inductors L3 and L4 are inserted to extend the bandwidth to maximize the voltage swing at Nodes A and B. For the IF1-RF TX-mixer, T-coil is selected as the load to achieve wideband output. Further, an output buffer with 50-Ω load is added at the output to obtain output impedance matching for direct connection to the off-chip pre-selection filter without a need of a power amplifier. Since the IF1 frequency is fixed at 2.9 GHz, LC tanks with Q of around 5 are employed as the loads for both the RF-to-IF1 RX-mixer and the BB-to-IF1 TX-mixer. As mentioned previously, the LC tanks also works as a band-pass filter to provide additional narrow-band filtering.

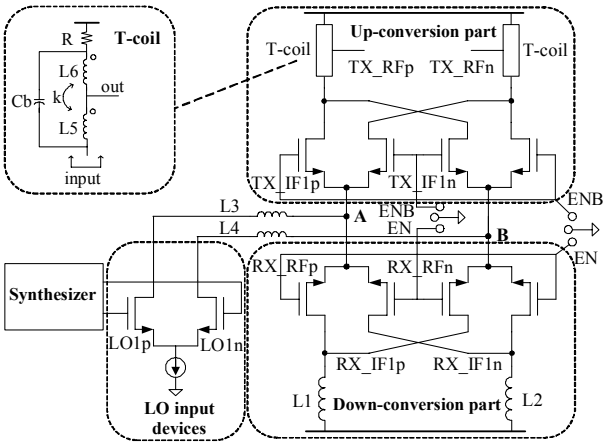


Fig. 2 Schematic of the proposed combined mixer for both RF down-conversion in RX and up-conversion in TX

A third-order Elliptic ladder low-pass channel-selection filter is employed for both IQ channels in the receiver chain to achieve adjacent-channel attenuation of better than -24 dBc. The filter is based on Gm-C architecture and has a -3dB bandwidth of 260 MHz and a fixed gain of 5 dB. A 3-stage VGA with variable gain range from 10 to 50 dB is designed. The first two VGA stages employ current steering to achieve a variable gain from -4 dB to 17 dB with a linear-in-dB exponential control circuit. Common-mode feedback and DC-offset cancellation circuitry are also included in the first two stages. The last stage has a constant gain of 17 dB for better linearity, which is followed by a source follower as an interface buffer to drive the large input capacitors of the ADC stage.

A 6-bit 528-MS/s ADC with folding and interpolating architecture is designed as shown in Fig. 3. The input signals and the reference voltages generated by a resistor ladder are connected to 20 pre-amplifiers, which are followed by a distributed track-and-hold (T/H) circuit. Four folding amplifiers, each consists of 5 differential pairs, are interpolated at the outputs by resistors to drive an array of 16 comparators. The outputs of the comparators are combined with the outputs

of a coarse 2-bit ADC by the digital encoder to obtain the final binary output bits. To reduce the offset of the pre-amplifiers, AC coupling capacitors and bias resistors with differential reference voltages are implemented as shown in Fig. 3. With this modification, only one differential pair is needed for signal combination, which results in lower offset, lower power, and higher operation frequency. The low-corner frequency is designed to be 2 MHz since the DC carrier is not used in the UWB systems.

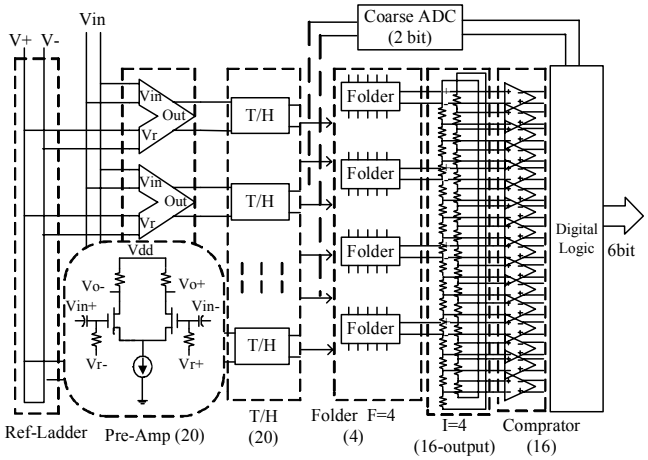


Fig. 3 Block diagram of the designed ADC

The TX's analog baseband is composed of two 6-bit 1-GS/s current-steering IQ DACs and 3rd-order RC low-pass filters. The DACs employ segmented architecture with 5 thermometer-coded MSBs and 1 binary-coded LSB. Four-quadrant two-dimensional centroid switching sequence is implemented to minimize the systematic error. Cascode current unit cells are adopted to increase the output impedance of the current source and to achieve better current matching.

The fully-integrated on-chip frequency synthesizer needs to provide fast band switching time of less than 9.5 ns. To ensure that the system SNR will not degrade by more than 0.1 dB due to intercarrier modulation, the synthesizer is expected to achieve an RMS noise of 3.5 degree. The designed synthesizer employs a fixed-frequency PLL with IQ outputs at 8.448 GHz and wideband single-sideband mixer (WB-SSB) to generate the variable LO1 and the fixed IQ LO2 signals required for the transceiver [6].

III. Experimental Results

The proposed 9-band UWB transceiver is fully integrated and fabricated in TSMC 0.18-µm CMOS process (VTn = 0.52 V, VTp = - 0.54 V) with 6 metal layers. Fig. 4 shows the die photograph, which occupies an area of 5.3×2.94 mm^2. All the internal pads are included only for probing purpose.

With an external reference signal of 66 MHz, the synthesizer measures the integrated phase noise of 3.78^o at 8.448 GHz band and LO sideband rejection of better than -28 dBc. The ADC achieves SNDR of better than 31.9 dB with an input signal up to 250MHz at the clock frequency of 500 MS/s. Fig. 5(a) shows the FFT plot at 250MHz input of the ADC. A sampling clock frequency of 900MHz is used for DAC, which is actually limited by the maximum frequency of data generator (HP80000). The worst-case SFDR of 33 dB with input frequency up to 250 MHz is measured. Fig. 5(b) shows the DAC's SFDR of 47.2 dB with a 225-MHz signal input.

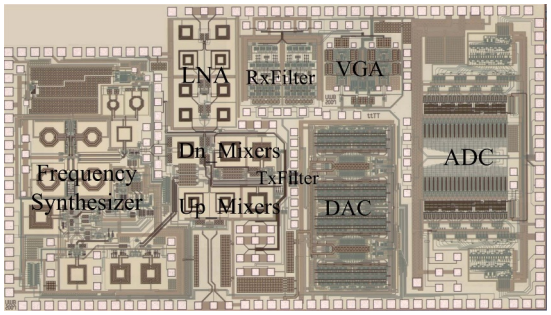
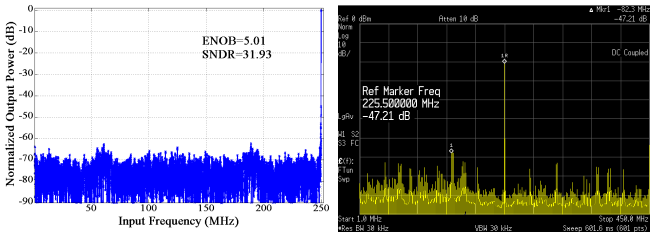


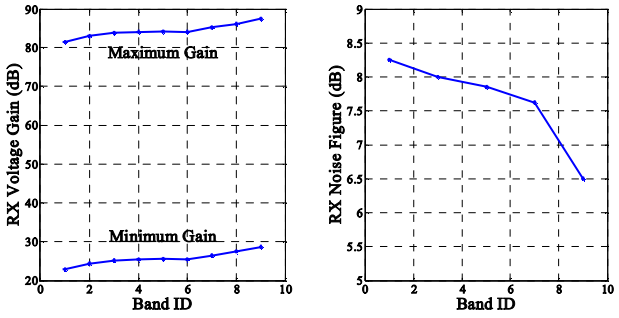
Fig. 4 Die Photograph



(a) (b)

Fig. 5 (a) ADC output spectrum with 250 MHz input; (b) DAC output spectrum with 225 MHz input @ 900M clock

As shown in Fig. 6(a), the receiver measures a total of 58.7 dB voltage gain range from 25.3 to 84.0 dB. Fig. 6(b) plots the measured NF under the maximum gain setting for different bands with a maximum NF of 8.25dB at lowest band. S11 of better than -13 dB is measured over the whole 9 frequency bands from 3.1 GHz to 8.0 GHz as has been reported in [5].



(a) (b)

Fig. 6 Measured RX (a) gain range; (b) NF at different band

From Figs. 7(a) and (b), the receiver input IP-1 dB of -19.9 dBm and in-band IIP3 of -12.65 dBm are measured for the 2nd frequency band with the minimum gain setting, respectively.

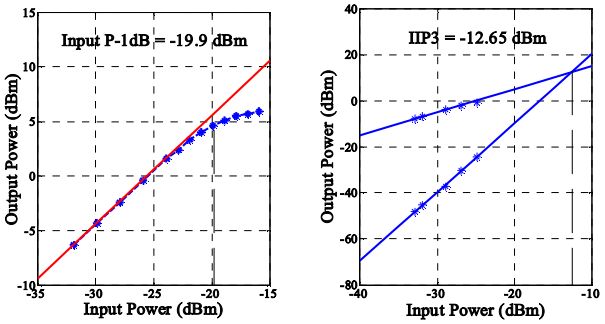
As plotted in Fig. 8, the receiver chain measures a -10 dB bandwidth of 325 MHz, and adjacent-channel attenuation of 39 dB at the VGA output.

Fig. 9 plots the IQ phase and gain mismatches of the receiver chain versus the baseband frequency IF2, which are measured to be better than 4 degree and 0.8 dB, respectively.

P-1dB of larger than -8.2 dBm is measured at the output of the transmitter. A minimum output sideband rejection of - 42.2

dBc at the 9th band is achieved as shown in Fig. 10(a). LO leakage of better than -46.5 dBc is also measured. To roughly evaluate the EVM performance without UWB EVM equipment setup, WLAN 802.11a OFDM (QPSK) modulation signals with code rate of 1/2 and bit rate of 12 Mbps are used. Fig. 10(b) shows the constellation diagram at the TX output for the 1st band with an output power of 3 dB back-off from the maximum, which measures an EVM of -25.3 dB (5.45%).

Operated under a 1.8-V supply, the receiver including IQ ADCs draws a total current of 291mA, and the transmitter including IQ DACs consumes 65mA while the synthesizer draws 57mA. Table 1 summarizes the measured performance of the proposed 9-band UWB transceiver.



(a) (b)

Fig. 7 (a) RX input P-1 dB plot; (b) RX in-band IIP3 plot at 2nd band

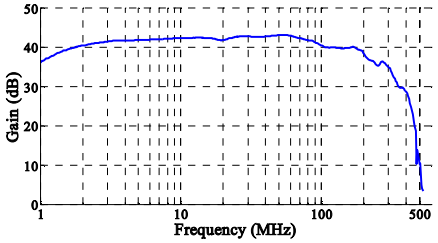


Fig. 8 RX bandwidth plot at VGA output

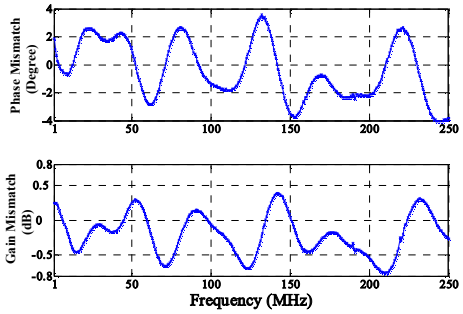
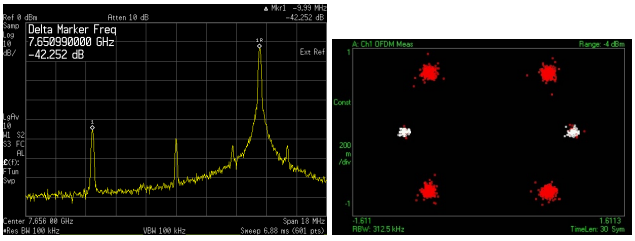


Fig. 9 RX IQ path phase & gain mismatch vs. baseband frequency



(a) (b)

Fig. 10 (a) TX output spectrum at 9th band; (b) TX constellation

IV. Conclusion

A single-chip 3.1-to-8.0 GHz UWB transceiver fully integrating the transceiver front-end and a complete analog baseband with IQ ADCs and DACs together with a fast-settling synthesizer was successfully demonstrated in a 0.18-µm CMOS process. A single mixer for both RF down conversion in RX and up conversions in TX was demonstrated. Operated under 1.8-V supply, all the measurement results show that the transceiver can meet all the specifications for a MB-OFDM UWB system covering the first 9 frequency bands.

Table 1. Summary of the measured performance of the transceiver

	BG 1 (3.1 – 4.75 GHz)	BG2 (4.75 – 6.3 GHz)	BG 3 (6.3 – 7.9 GHz)
Receiver			
Voltage Gain (dB)	> 81.5	> 84.1	> 85.2
NF (dB)*	8.12	7.85	7.04
S11	< -13	< -18	< -20
In-Band IIP3 (dBm)**	-12.65	-13.7	
Input P-1dB (dBm)**	-19.9	-21.7	-22.6
In-Band IIP2 (dBm)	22		
IQ Mismatch	< 0.8 dB (gain) ; < 4 Degree (Phase)		
Transmitter			
Output P-1dB (dBm)	> -8.2	> -7.2	> -7
Sideband Rejection (dBc)	< -43	< -43	< -42.2
LO leakage (dBc)	< -47.3	< -47.1	< 46.5
EVM ***	- 25.3 dB (5.45 %) @ 3 dB back-off		
Synthesizer			
PN @ 10MHz (dBc/Hz)	< -129.7	< -127.3	< -126.7
RMS Noise (degree)	< 3.22	< 4	< 4.8
LO Sideband Rejection (dBc)	< -36	< -28	< -27.9
Other Parameters			
Supply Voltage	1.8 V		
Current Consumption (mA)	101 mA (RX w/o ADC) 20 mA (TX w/o DAC) 57 mA (Synthesizer) 190 mA (IQ ADC); 45 mA (IQ DAC)		
Chip Area	5.3×2.94 mm^2		

* The NF is averaged within each band group (3 bands each)
** The in-band IIP3 and P-1dB is measured with minimum gain
*** The EVM is measured with WLAN 11a QPSK signals

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