Portable and Scalable High Voltage Circuits for Automotive Applications in BiCMOS Processes

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2019 Custom Integrated Circuits Conference - Education Sessions

Outline

- Motivation : Automotive ICs
- Smart Power Drivers – Case Study : Squib Driver Unit
- Pin and Design FMEA
- High Side Current Sensing
- Low Side Current Sensing
- Biasing Schemes
- Diagnostics
- Additional Automotive Requirements
- Conclusion

Motivation : Automotive ICs

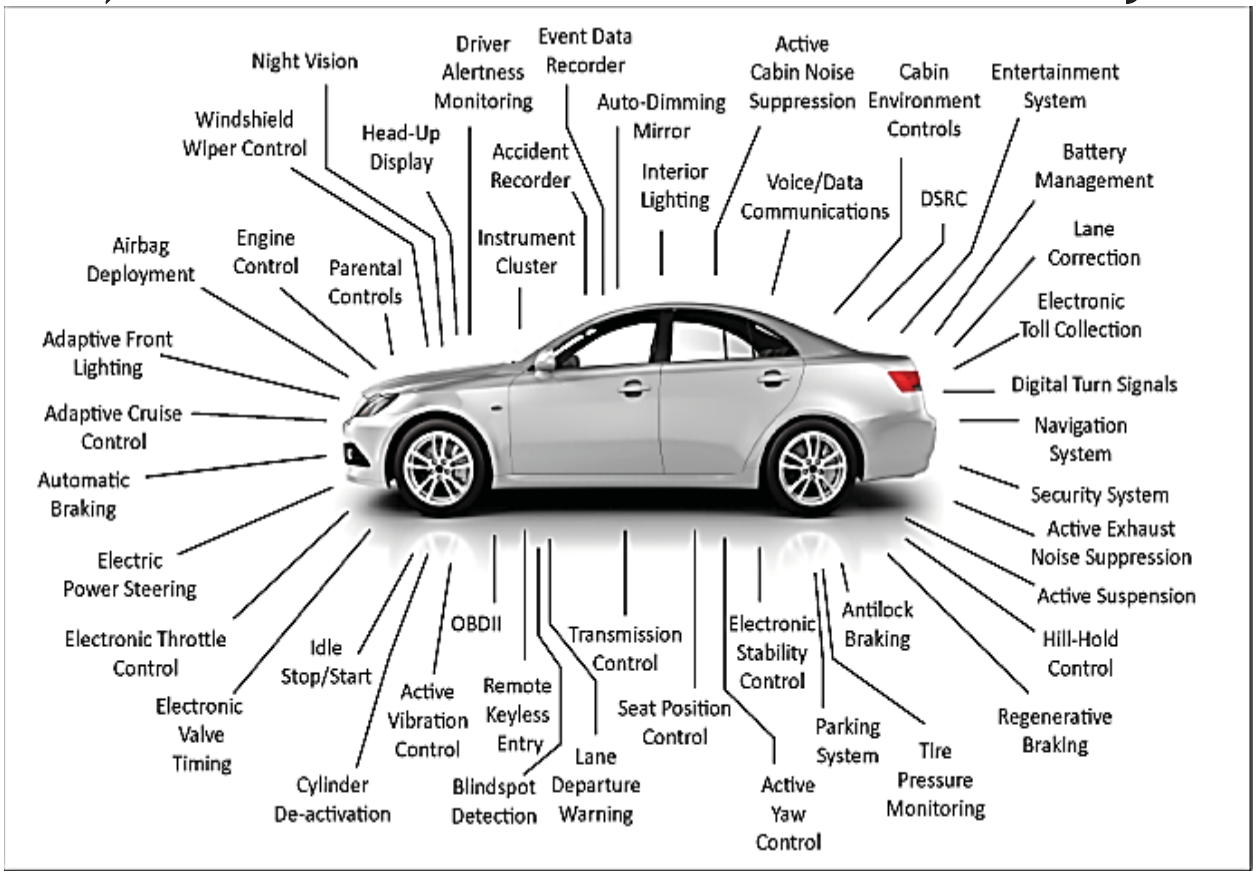
- Motivation - Automotive ICs
- Automotive SOCs – Overview
- Automotive SBCs
- Power Semiconductors (LDMOS, DE-NMOS)
- Temperature, Reliability and Loads
- High Side and Low Side Configuration

Motivation – Automotive ICs

- Electronic control in Automotive is increasing (less hydraulics/mechanics). Power semiconductors are the key.

Benefits

- Longer life expectancy for vehicles.
- Connected cars, higher road safety.



[Clemson University of Vehicular Electronics Laboratory]

Automotive SOCs-Overview

Electronic content in Automotive => Integrated circuits.

- Trend

  Larger integration.

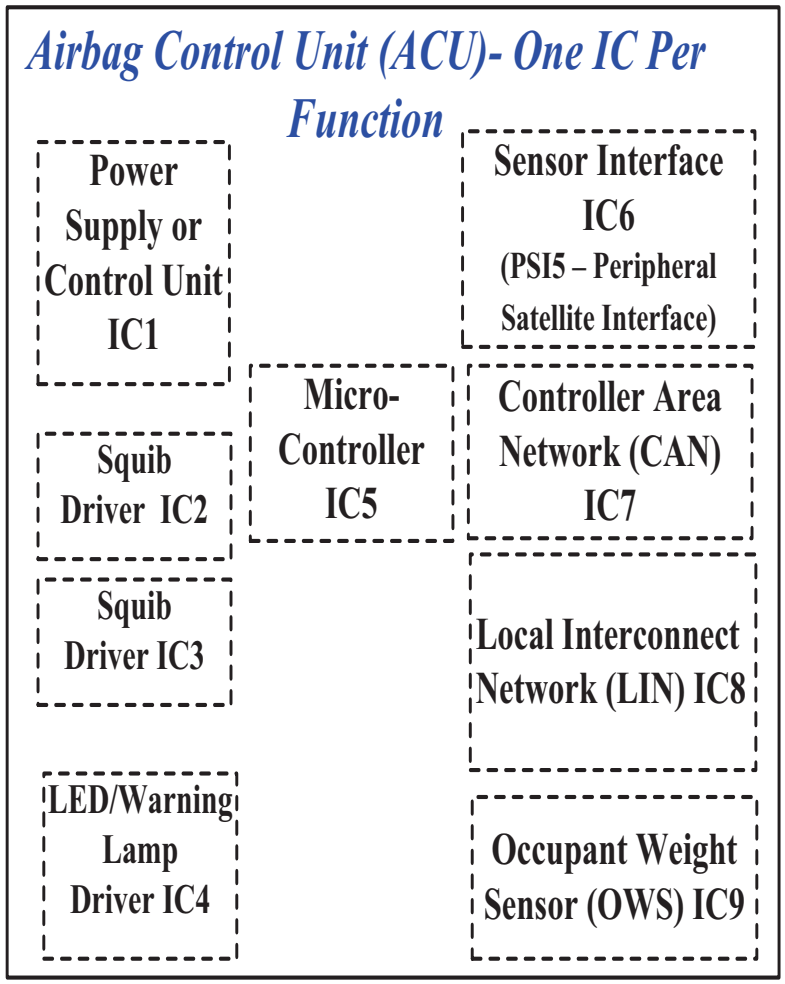
- Low Cost

  Lesser Bill of Materials, Smaller PCB size.

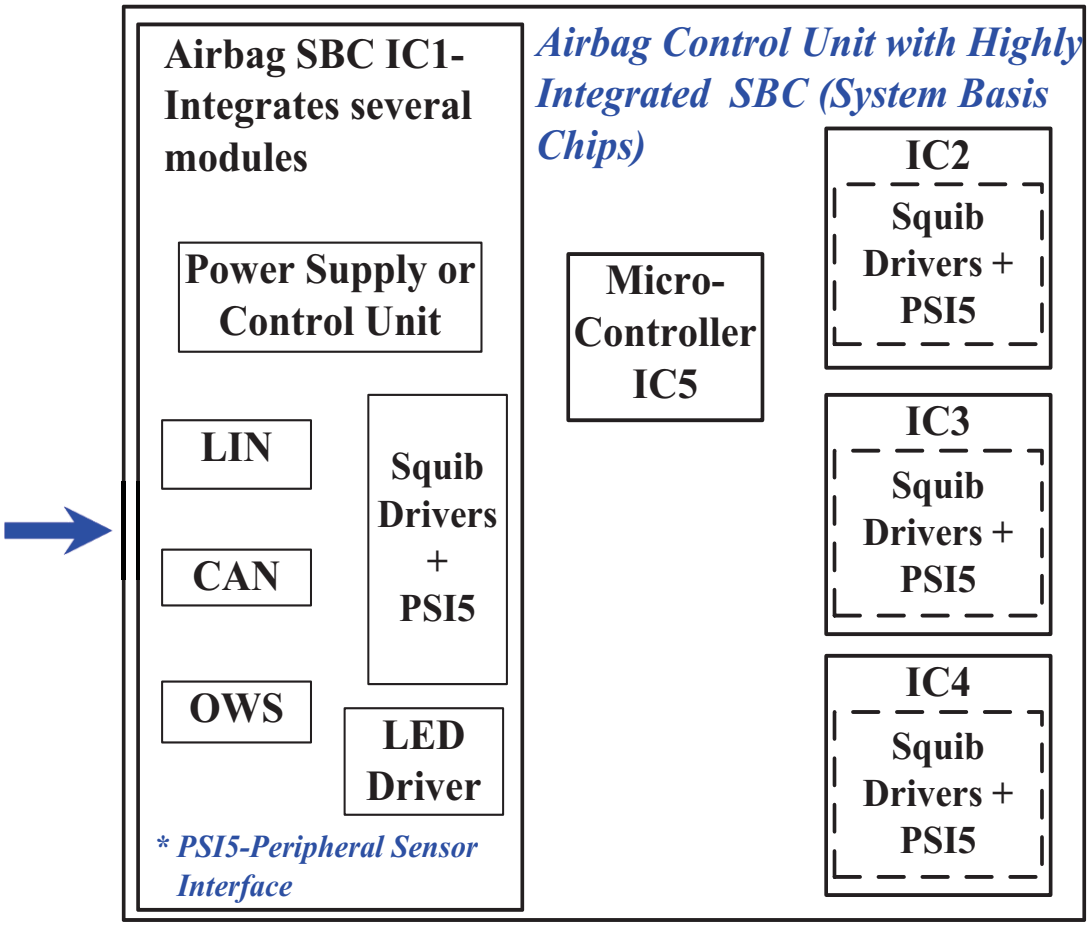
Large Scale integration – Challenges

- Power dissipation, package, On chip Cross talk/Noise between modules.
- Longer time for release to market (Longer validation time).
- Larger die -> higher defect density (0 dppm target is challenged !)

Automotive System Basis Chips (SBC)- Airbag Control Unit (ACU) Example



Prior Electronic Content
Individual ICs for each function



State of the Art - Increased Electronic Content. More squib channels, sensors, increased functionality, smaller PCB.

Key Components

- Power ICs -> powerFETs and their drivers are the key.
- These high voltage components dissipate high power.
  (Higher V_{ds}*I_d).
- LDMOS (Laterally Diffused Metal Oxide Semiconductors) is heavily used. Low Rds_on, ~ 500mΩ or lower @ smaller area.
- -2V to 40V requirements. Some applications need -18V.

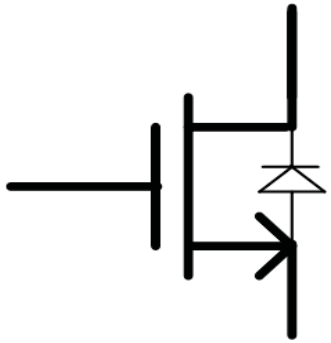
Technology

Bipolar, CMOS and LDMOS (BCD) + Resistors, Capacitors.

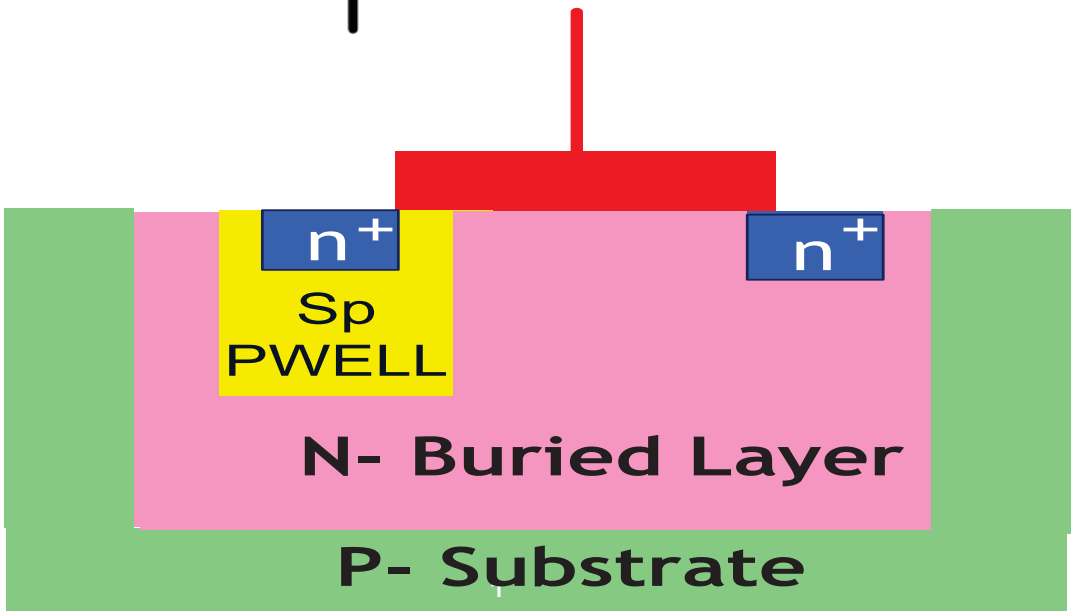
LDMOS when replaced by Drain Extended NMOS => BiCMOS.

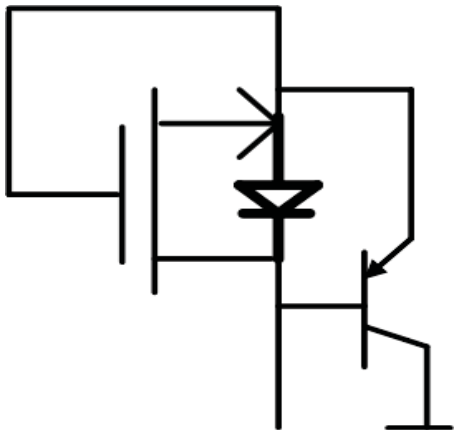
LDMOS Transistors and Body Diodes

- Laterally Diffused MOS (LDMOS) is mainly used for powerFETs.
- In built body diode is effectively used in designs.



LDMOS FETs
V_{ds_max}= 40V.. 60V
V_{gs_max}=12V or 5V

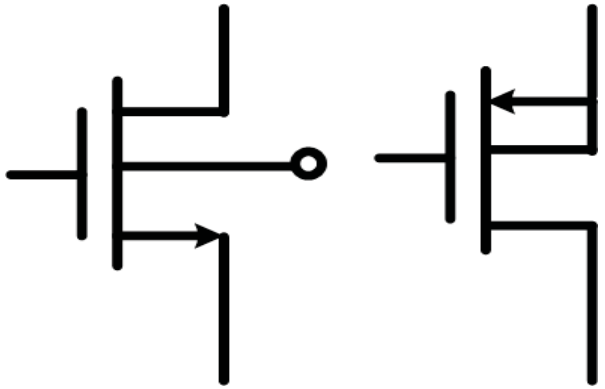




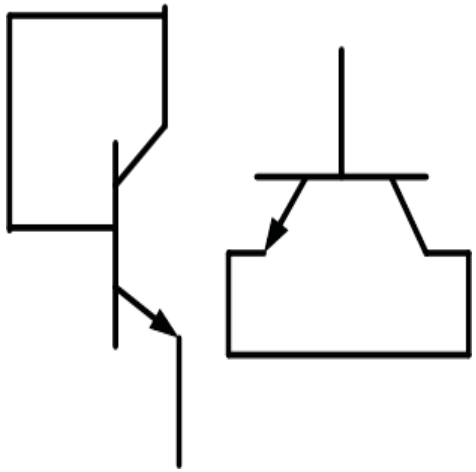
LDMOS as a Diode
(Parasitic PNP leakage)

High Voltage (HV) Components

Drain Extended (DE) NMOS and PMOS

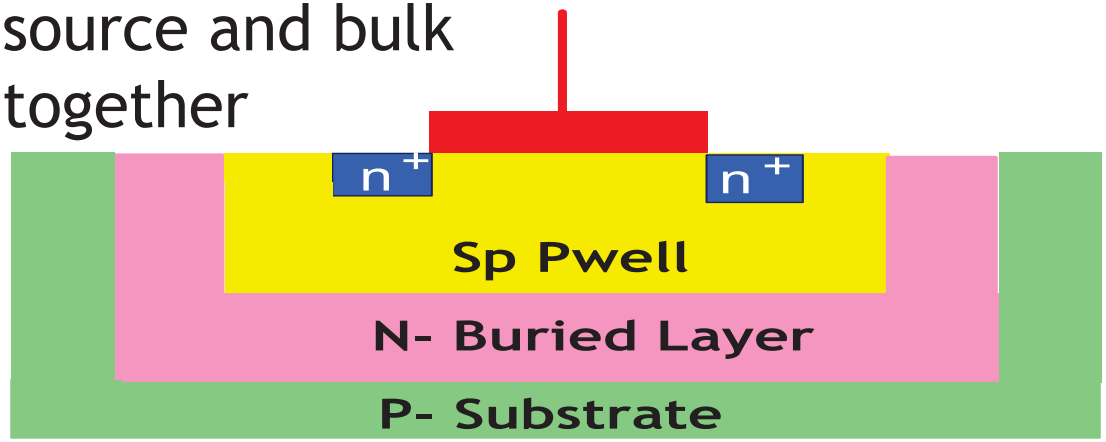


DE-NMOS/PMOS
V_{ds_max}= 40V.. 60V
V_{gs_max}=12V or 5V
In some DE-NMOS, s-b can be tied together



C-B or C-E Shorted NPN (Zener behavior).

DE-NMOS with isolation to connect source and bulk together

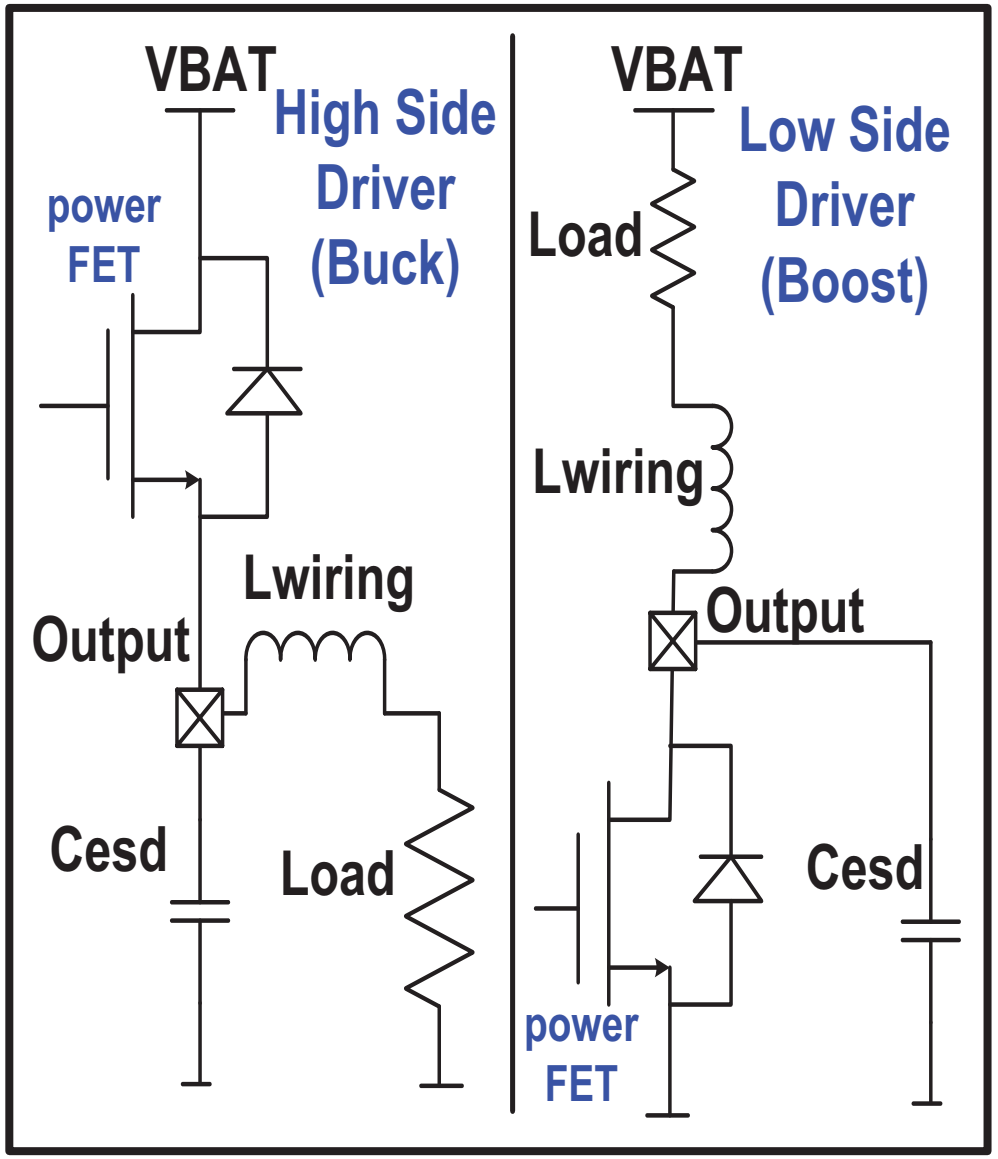


Temperature, Reliability and Loads

- High Power Dissipation , High Junction Temperature
  - Junction temperature rise within powerFETs ~ 400°C.
  - No Vgs, Vds,Vsb rating violation. Operate within electrical Safe Operating Area (SOA).
- Multiple Supply Voltage (MSV), Power Supply faults
  - No Inadvertent activation or de-activation of powerFETs, power stages.
- Load : Inductance range (1µH to 3mH). Stability is critical.
- Diagnostic circuits : No false flags.

High Side, Low Side Configuration

- Automotive ICs need to
  - Handle inductive loads without external free-wheeling path.
  - Withstand single fault ("Output" Short to battery **(SCB)** or ground **(SCG))** **multiple times.** (0 Ohm Load).



Smart Power Drivers
Case Study - Squib Driver Unit (SDU)

- Introduction to ACU, SDU, PCU Terminologies
- SDU Requirements (Powered/Unpowered)
- SDU Specification

Airbag Control Unit (ACU)

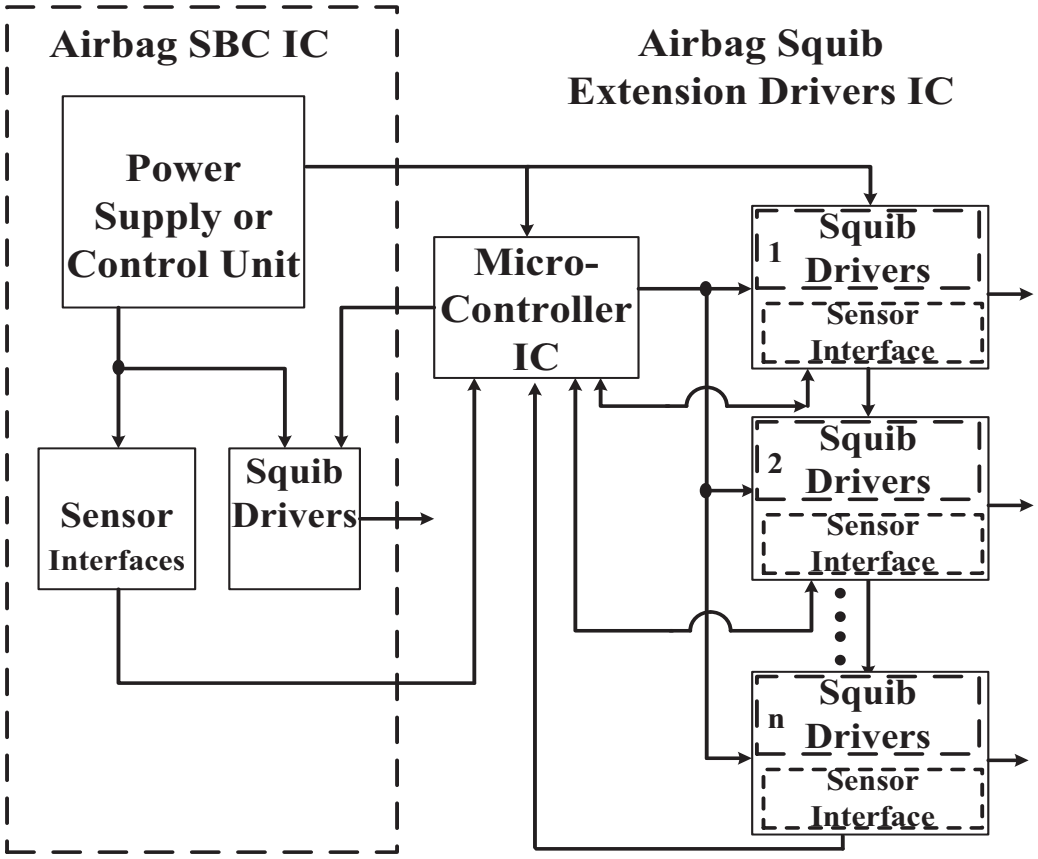
- Airbag Control Unit (ACU) contains System Basis Chips (SBC), Squib Driver Extension ICs and Micro-Controller.

Airbag SBC

- Power Control Unit (PCU), Squib Driver Unit (SDU) and Sensor Interfaces like PSI5.

Squib Driver Extension ICs

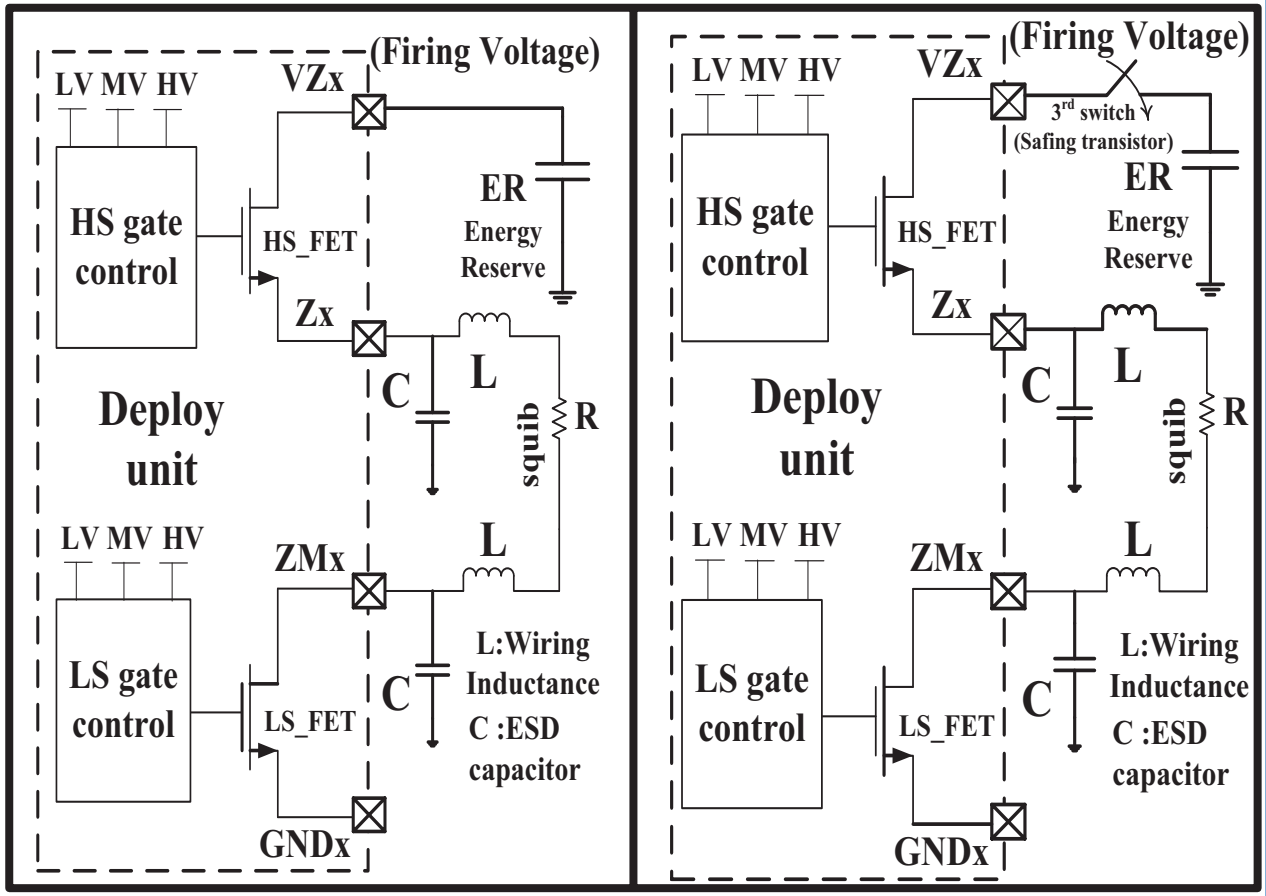
- Extension ICs have Squib Drivers and PSI5.



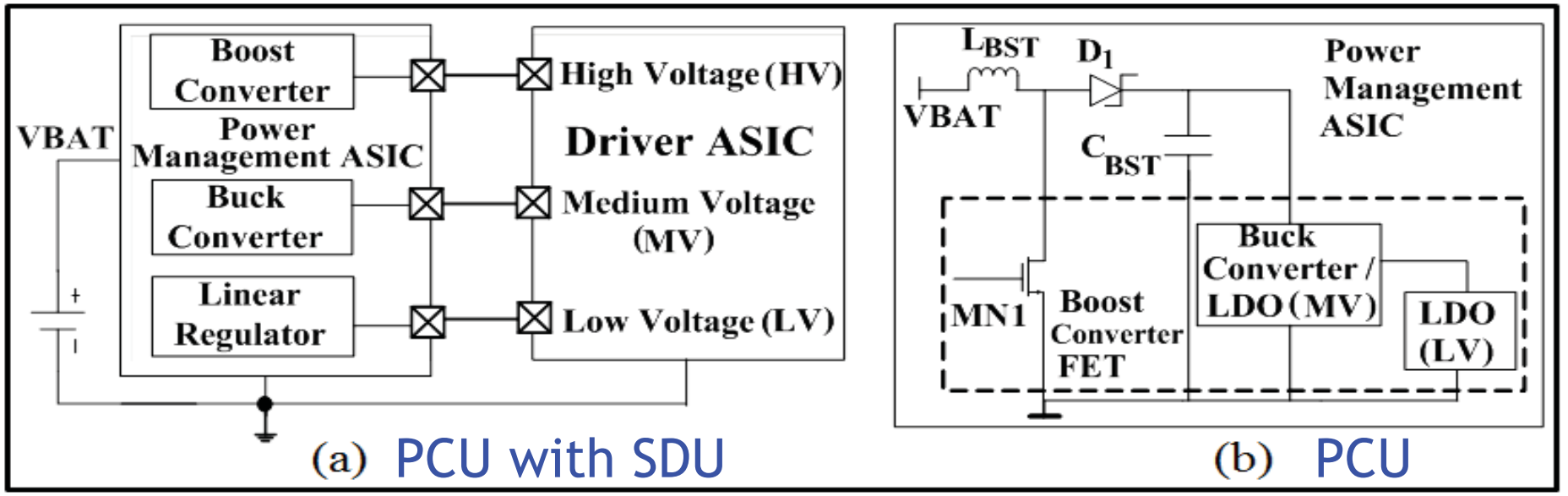
Squib Driver Unit (SDU)

- SDUs provide current to ignite squibs for deploying airbags.
  Deployment loop : High Side (HS) FET + Low Side (LS)FET.
- HS_FET regulates the current. LS_FET in Rds_on mode.

- **Multiple Supply -** (HV : 33V..38V,
  MV : 5V,
  LV : 1.8V or 3.3V).
- **Diagnostics -** Voltages, leakage, resistance checks.
- 75% of the pins are **40V** rated.



Power Control Unit (PCU)



- Boost Converter_HV (33V to 38V): Gate Driver Supply and Diagnostics.
- Buck Converter(5V to 6V)_MV : Bandgap, Bias current generator, level shifters.
- Linear Regulator (3.3V)_LV : Digital core supply and IO Buffers.
- Deployment voltage VZx can be either HV rail or regulated down to 25V.

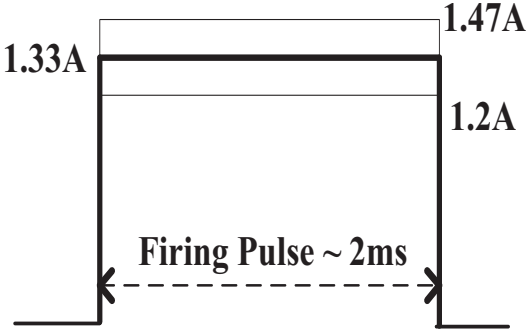
Squib Driver Requirement

Powered State

- HV,MV,LV, VZx rails are available. HS, LS Drivers activated => Time limited regulated current (Energy<9mJ or 7mJ) from HS_FET ignites the squib to deploy the airbag.

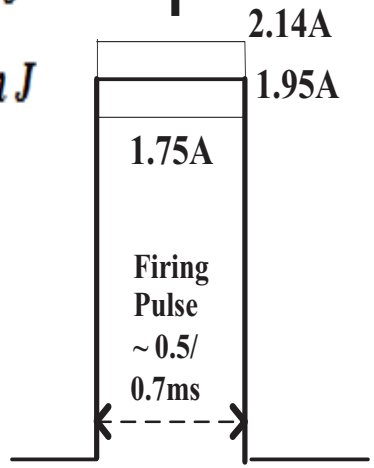
$$I^2RT = (1.47A)^2.(2\Omega).2ms = 8.64mJ$$

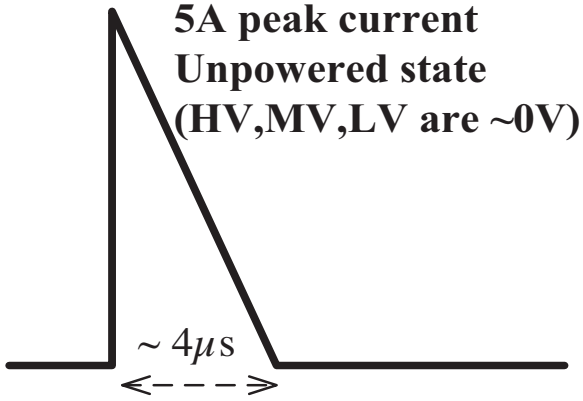
$$I^2RT = (2.14A)^2.(2\Omega).0.7ms = 6.4mJ$$



Unpowered State

- When One of the rails is not available or Fast SCG or SCB during the unpowered state of SOC, high current or Energy ~6mJ is not allowed.
- Current should be limited to 5A for 4µs. (No fire spec)

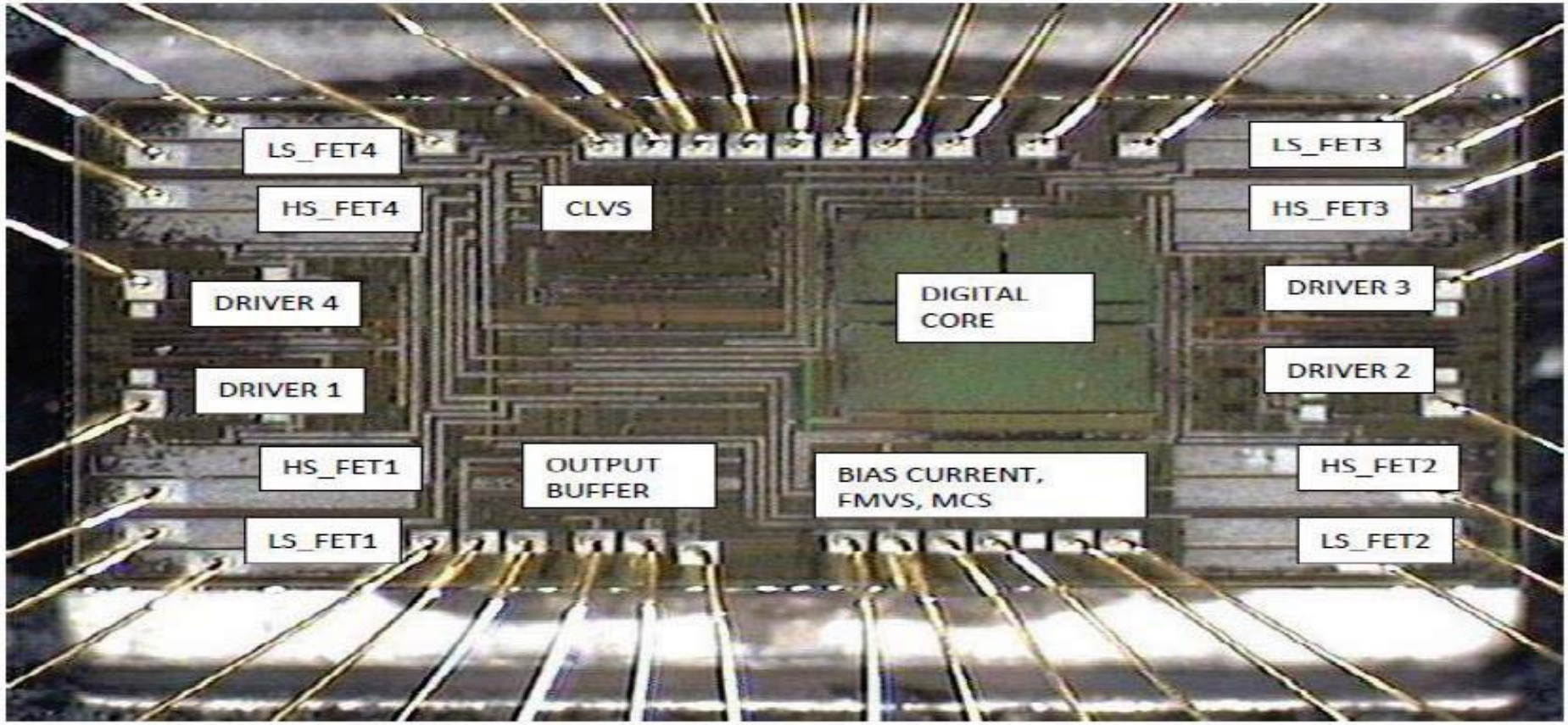




SDU Specification

Spec Parameter	Target	Comments
HS_FET Current Regulation	2A +/-10% and 1.35A +/-10%	Airbag deployment currents. Inductance range 1µH to 3mH.
LS_FET Current Regulation	3A +/- 15%	Protection for LS in case of SCB. Inductance range 1µH to 3mH.
HS/LS FETs Surge Current Limitation	5A,4µs	To prevent inadvertent deployment
Quiescent Current of the Driver	5mA	No diagnostics current sources are enabled
Diagnostic Reference	8.4V	100pF to 220nF cap range, Current Limited Voltage Source (CLVS)
Diagnostic Output Max	5.4V	Input can range 100mV to 30V
Deployment Voltage	25V to 35V	35V (Energy Reserve Capacitor).
Leakage Current on Drain of HS/LS_FET	< 1µA	Range 0 to 35V

TI Quad Channel Squib Driver



- 40V, TI BiCMOS Process. 0.35µm, quad channel airbag squib driver.

Failure Mode Effect Analysis (FMEA)
Pin FMEA (PFMEA) and Design FMEA (DFMEA)

- Introducing PFMEA and DFMEA
- Introduction to Current Sensing

Pin FMEA Example

- FMEA,Automotive IC designs go hand in hand.
- SOC pin fault Analysis @ PCB/system level is the key for design specifications.
- Occurrence and detection of faults are important.

  Occurrence = 7 (chances of shorts during PCB manufacturing level is high)

  Detection =1 (chances of detection of shorts are very high).

Pin FMEA Example- VDD5 Regulator

Pin Number	Pin Name	Potential Fault Mode	Potential Effect of Failure	Fault Cause	Occurrence	Detection
			SOC Level	(During Design & Manufacturing Levels)		
1	VDD5	Pin Open	Output of the regulator IC is open.	Open Bondwire	7	1
		Short to GND	Too high current flowing through the output stage. High power dissipation.	Bondwire/Wire short to Ground line	7	1
		Short to Vbat	Too high reverse current flowing through the output stage. High power dissipation	Bondwire/Wire short to a high voltage line	7	1
		Short to GND (Neighboring pin)	Too high current flowing through the output stage. High power dissipation.	Bondwire/Wire short to neigbouring line	7	1

Current Sensing,limitation/regulation is the key to address faults.

Pin FMEA to Design FMEA- Design Approach

#1 Pin FMEA → VDD5 regulator power dissipation during short to ground (high Iload) is a high risk.

→ #2 Design Measure : Current Limitation

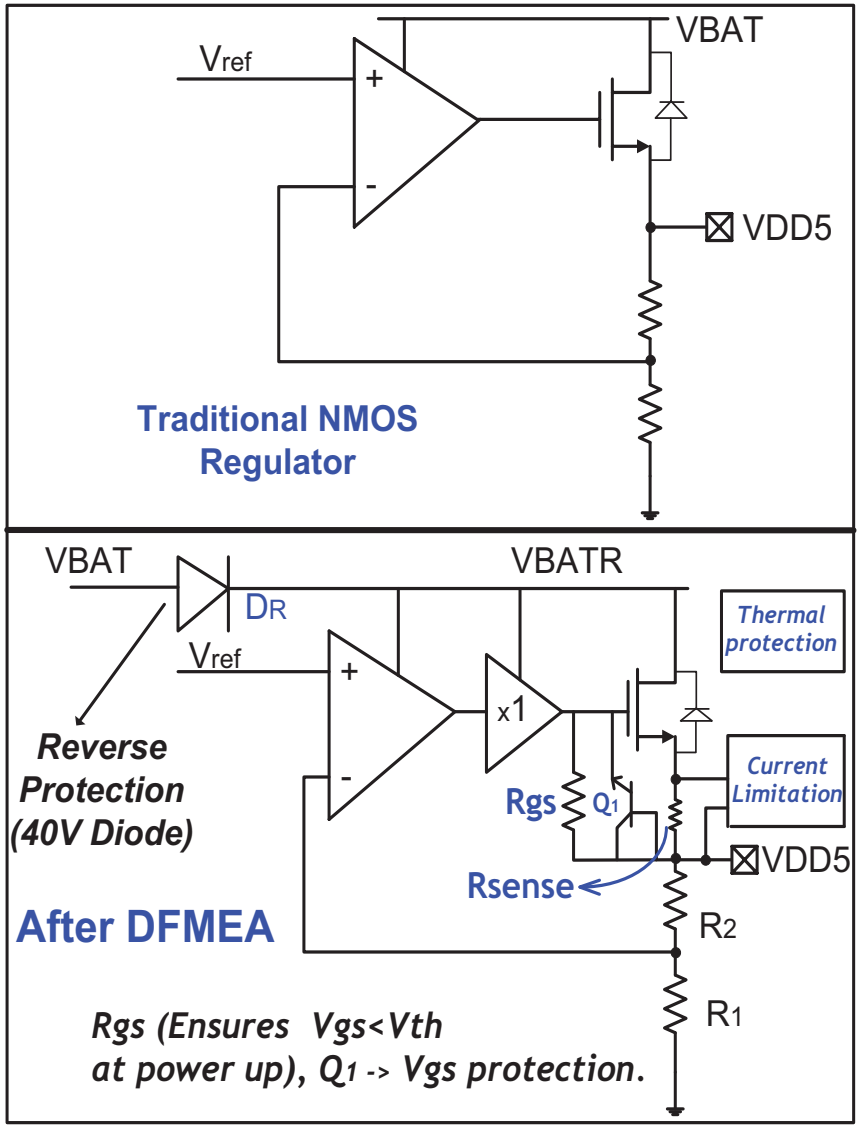
→ #3 Risk Mitigation :
If #2 fails (latent defect)
→ Back up protection ?
= Over Current Detection (Ioc)

→ #4 Iload > Ioc →
Turn OFF VDD5

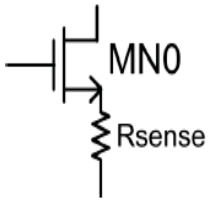
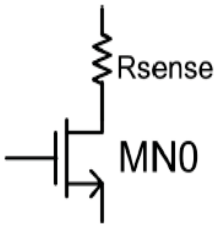
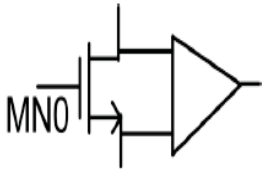
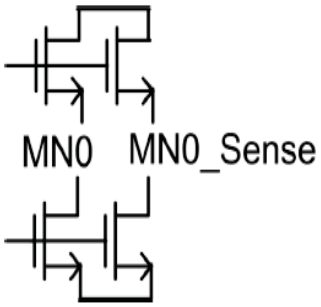
→ #5 Iload < Ioc =>
#4 fails. No Turn OFF (High Risk) !
→ Thermal Protection

DFMEA :
SYSTEMATIC DESIGN APPROACH TO MITIGATE DESIGN FAILURES

<u>Designs need Over Current and Thermal Protection along with Vgs, Vds protection</u>

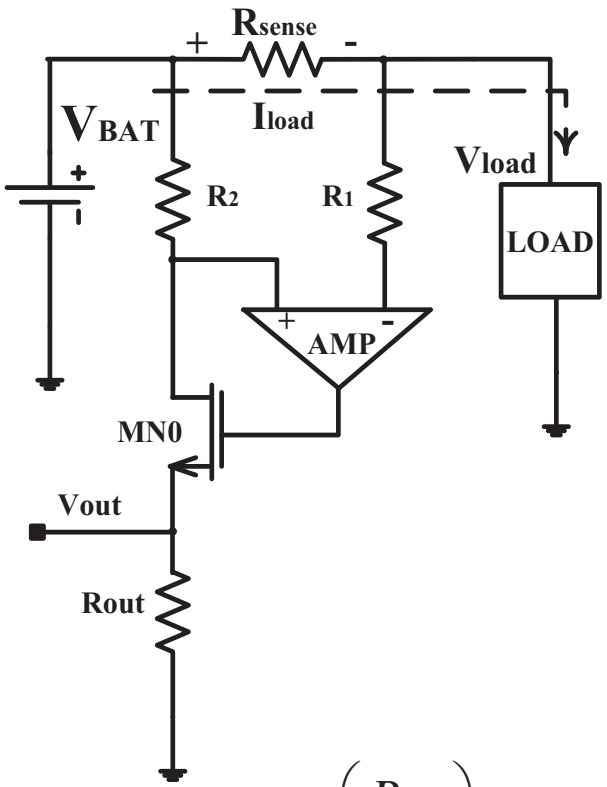


Current Sensing Techniques

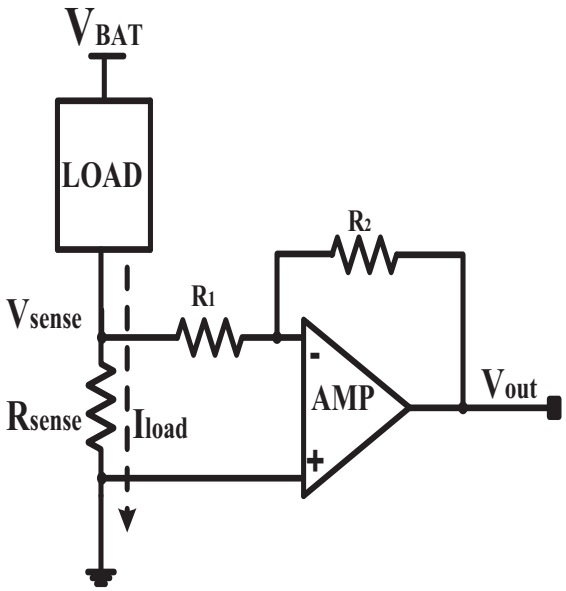
Topology	Method	Description	Advantages	Disadvantages
	Sense Resistor Source Side	Poly resistor in series with the switch	Accurate. Regulation loop stability is easier as the architecture is similar to a source follower type.	Sensitive to Substrate Currents. Limited to less than 300mA.
	Sense Resistor Drain Side	Poly resistor in series with the switch	Accurate and insensitive to substrate currents	Stabilizing the loop is not straight forward as the power stage is a gain stage.
	Power switch Ron	R_{ds_on} of the switch	Higher current limits can be achieved	Inaccurate
	Sense-FET	Scaled version of powerFET for current sensing (drain or source tied together)	Higher current limits can be achieved	Threshold voltage Mismatch between powerFET and senseFET

Current Sensing Fundamentals

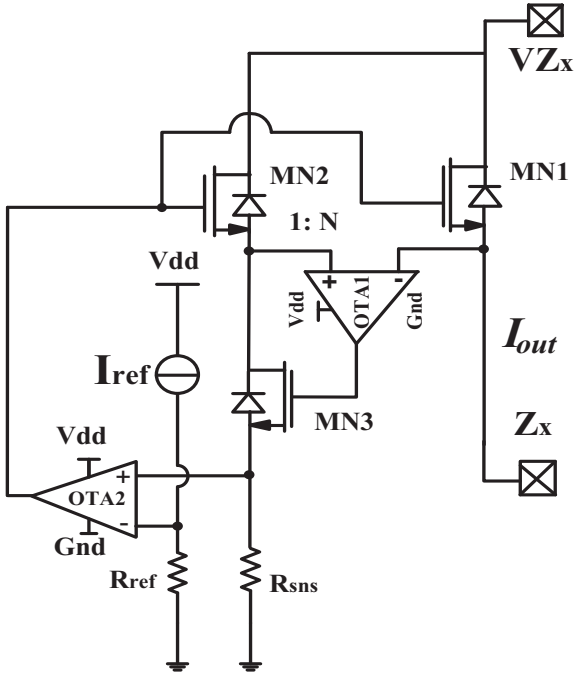
Sense the current (shunt resistor based or senseFET based).
Limit the V_{BE} or V_{GS} of the Transistor to limit the current.



$$V_{out} = I_{load} R_{sense} \left(\frac{R_{out}}{R_2} \right)$$



$$V_{out} = -\left(\frac{I_{load} R_{sense}}{R_1} \right) R_2$$

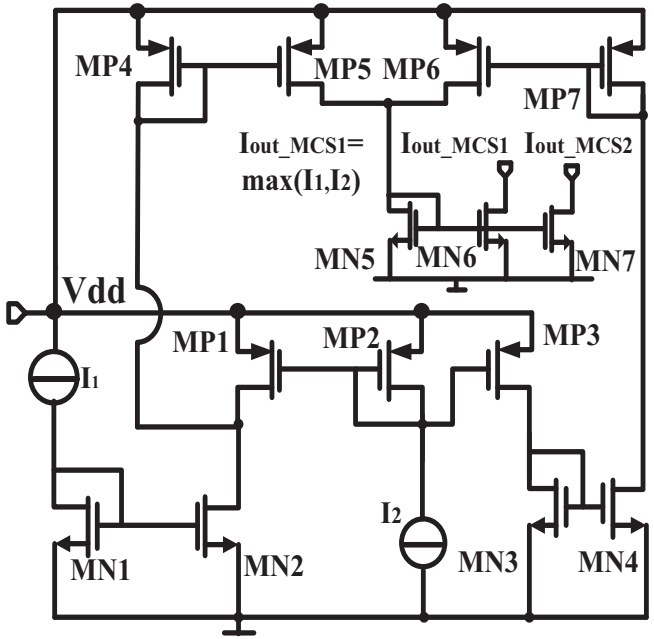


$$\left(\frac{I_{out}}{N} \right) R_{sns} = I_{ref} R_{ref}$$

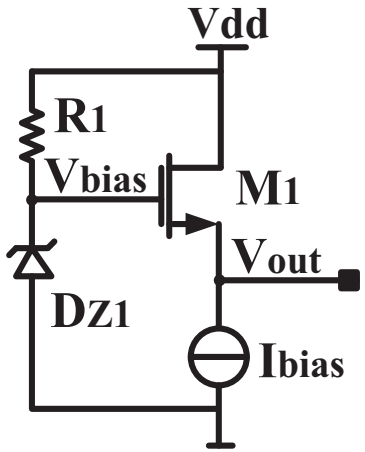
$$\Rightarrow I_{out} = \frac{I_{ref} R_{ref} N}{R_{sns}}$$

Circuits Commonly Used

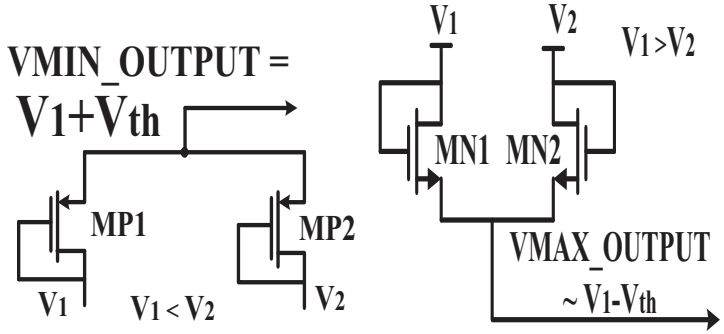
Maximum Current Selector

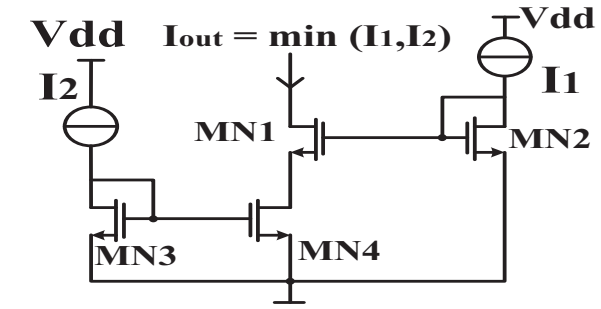


Voltage Limiter

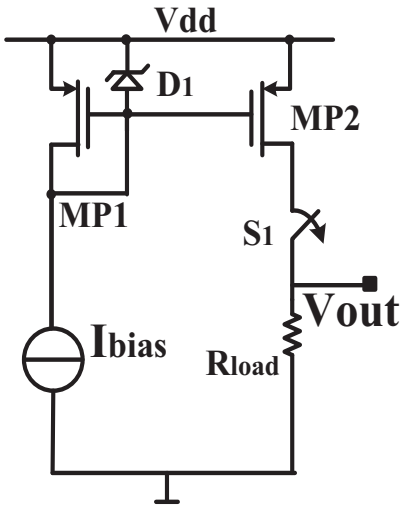


Minimum, Maximum Voltage Selectors

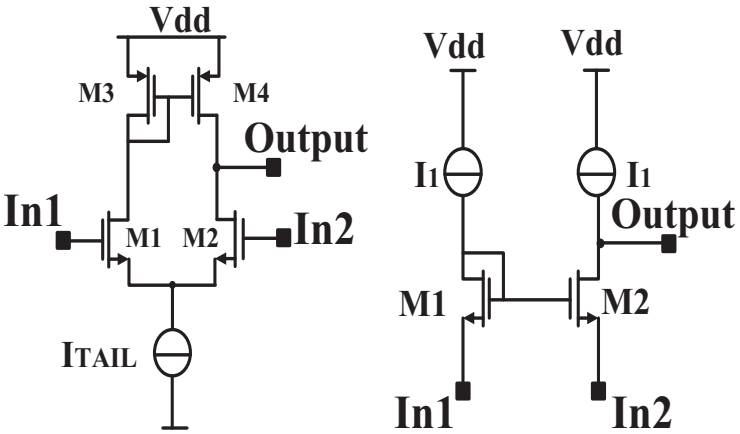




Minimum Current Selector



Current Limiter

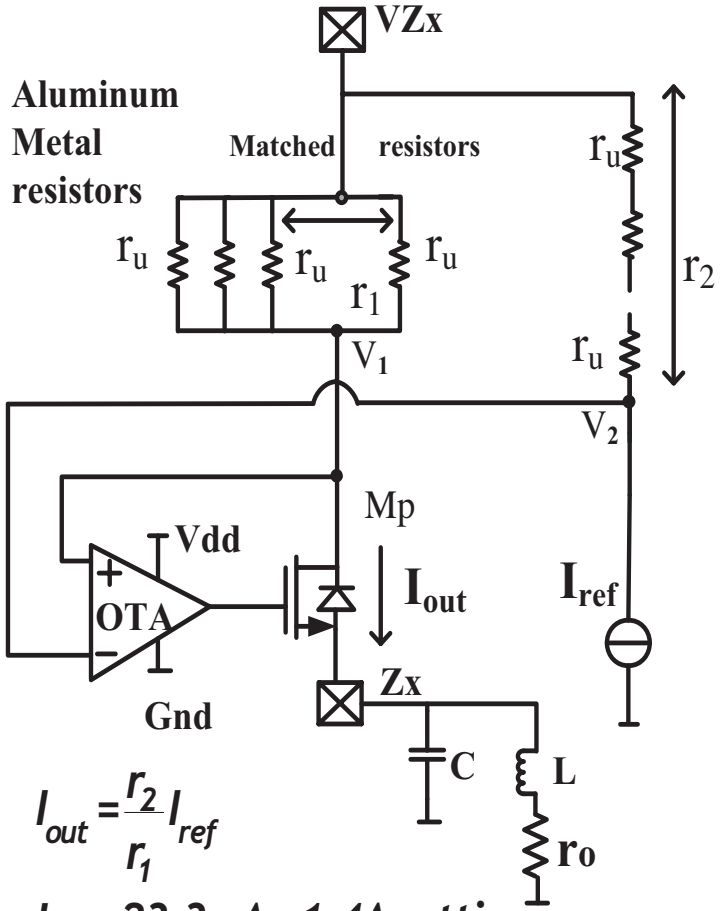


Voltage & Current Differential Stages

High Side (HS) Current Sensing - Metal Resistor

- HS Current Regulation Concept
- FLOTHERM Simulations
- Isothermal Plots
- HS Layout Strategy
- Free-Wheeling Path
- Self Heating

HS Current Regulation Loop Concept



$$I_{out} = \frac{r_2}{r_1} I_{ref}$$

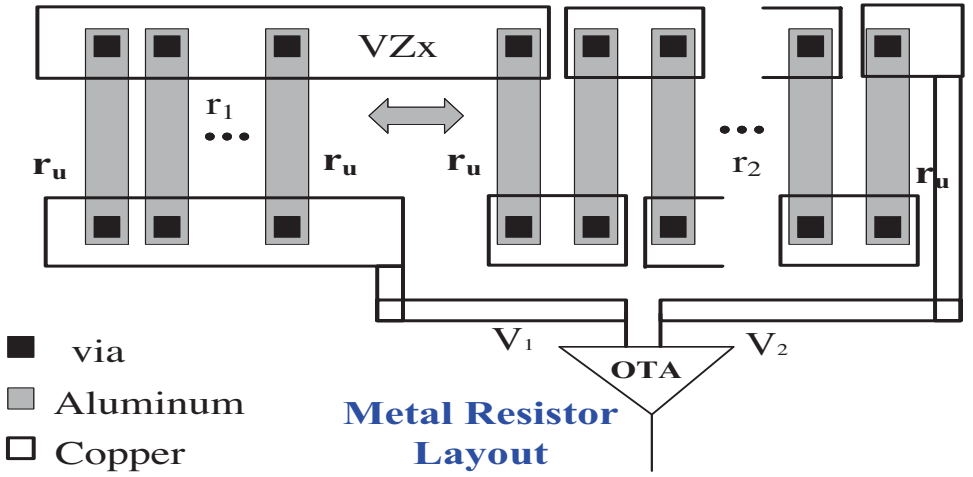
I_{ref} ~ 23.3mA → 1.4A setting

I_{ref} ~ 33.3mA → 2.0A setting

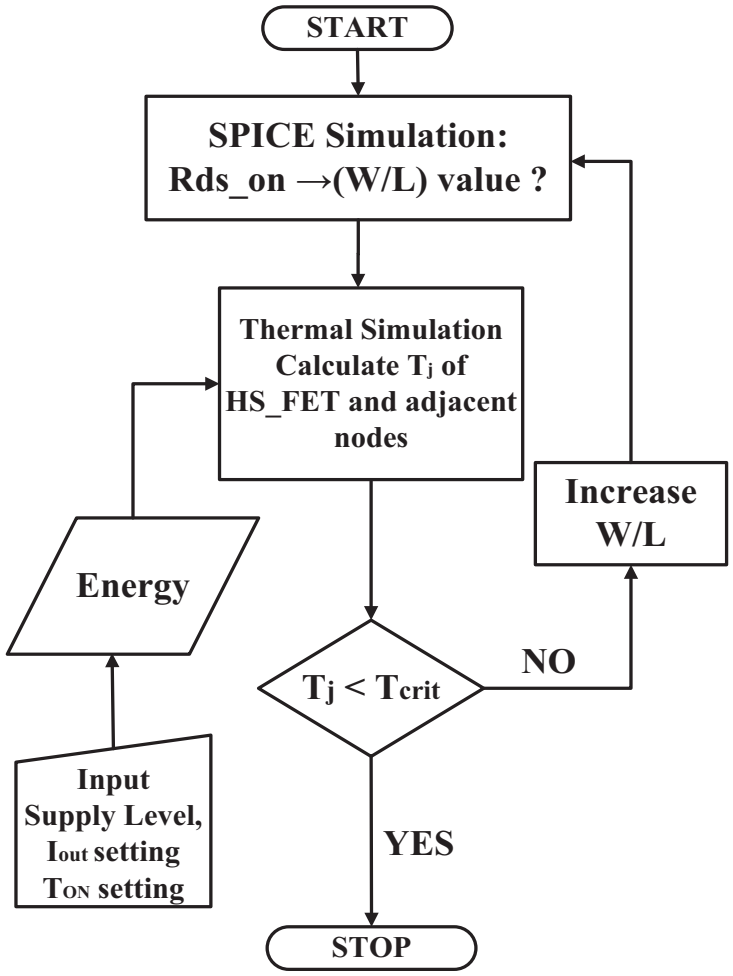
[Easwaran et al US 8,093,925B2]

- Power Dissipation across Mp

  [VZx- (Iout.r_0)]* Iout. (VZx=38V)
- r_0= R_squib + Rds_on_LS ~1.8Ω… 2Ω.
- 2A Case : ~64W to 68W for 0.75ms (48mJ energy)
- 1.4A case: ~49W for 2.1ms (98mJ energy).

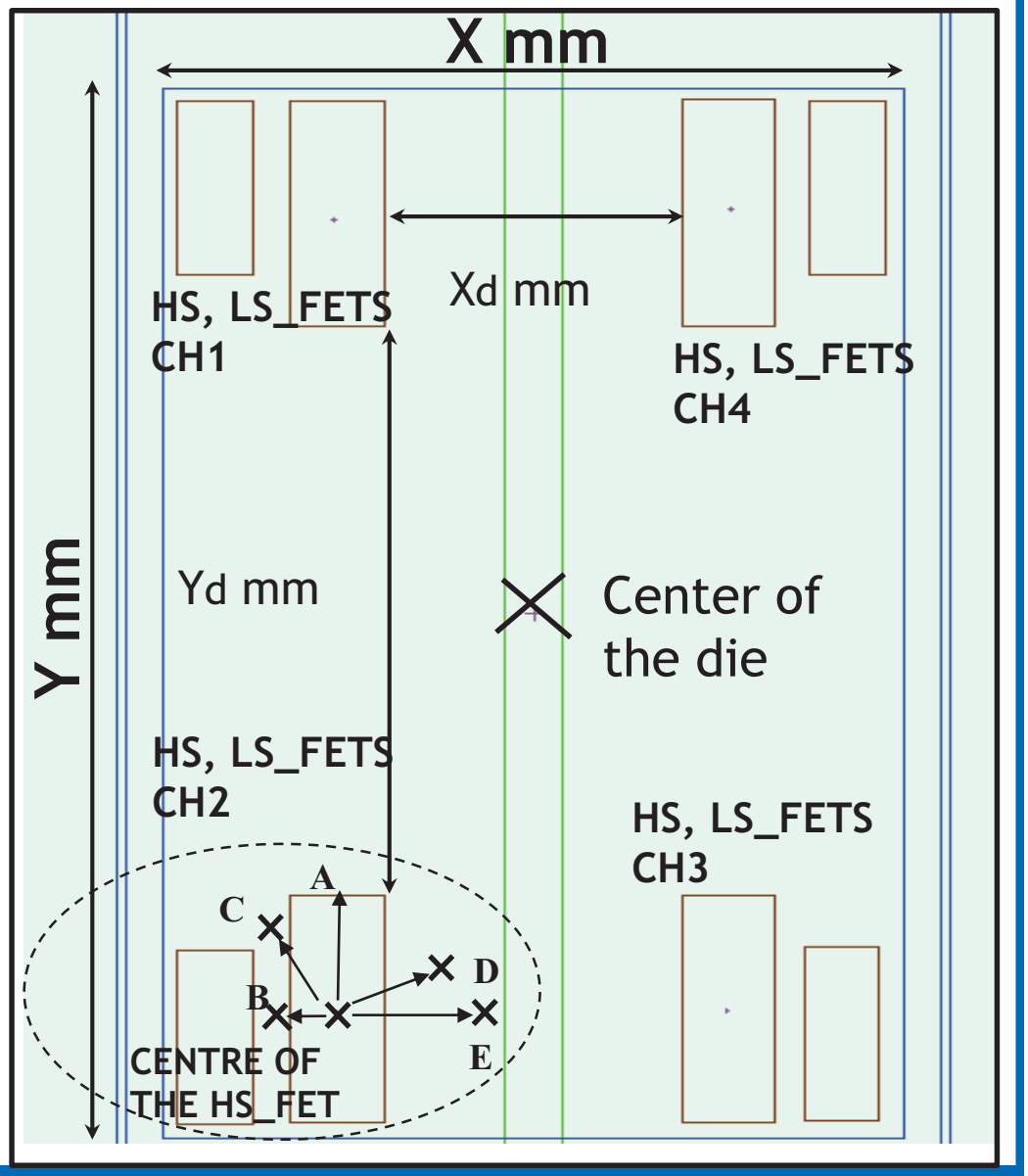


FLOTHERM Simulation [HS_FET Temperature rise]

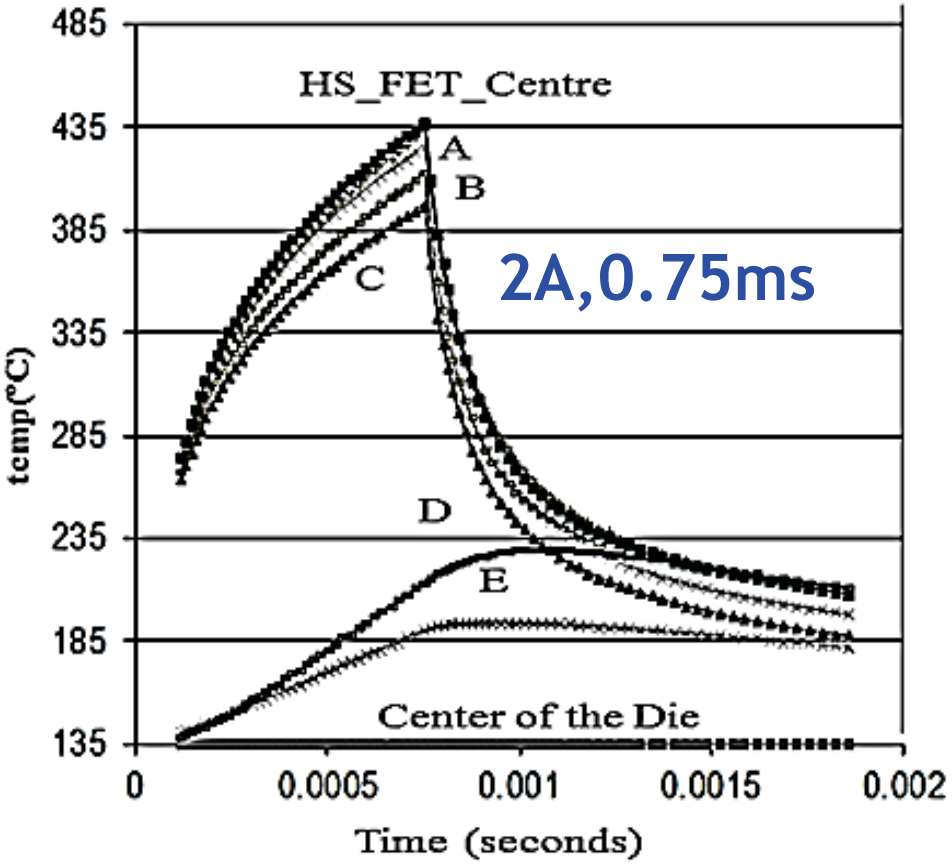


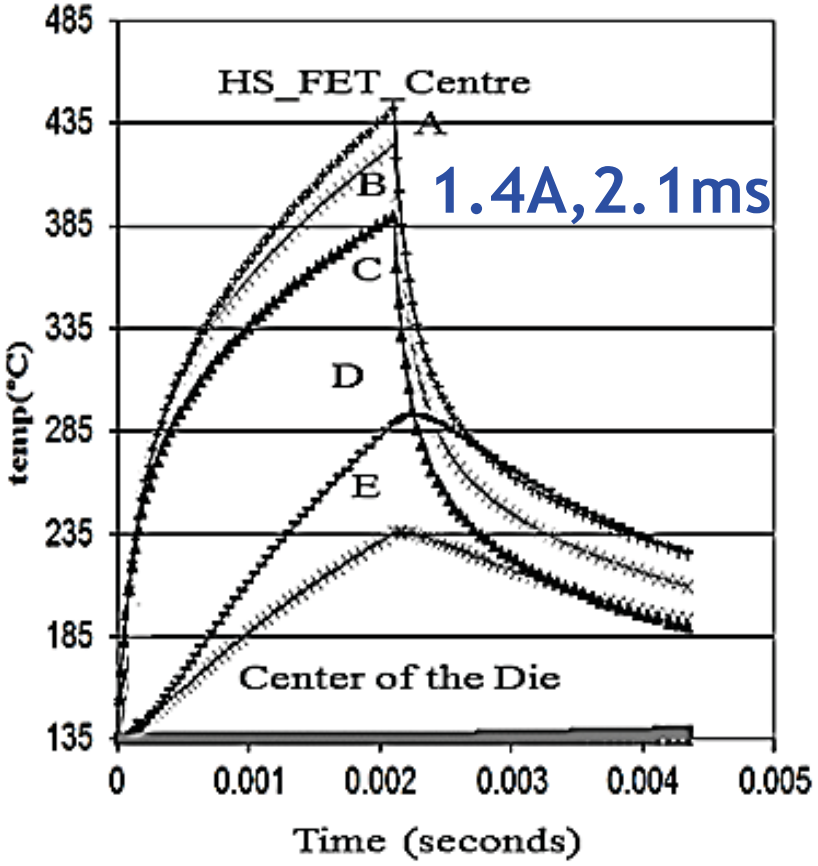
Case Study: Quad channel Airbag Squib Driver.

All 4 channels activated simultaneously



Temperature rise around HS_FET Gate Driver

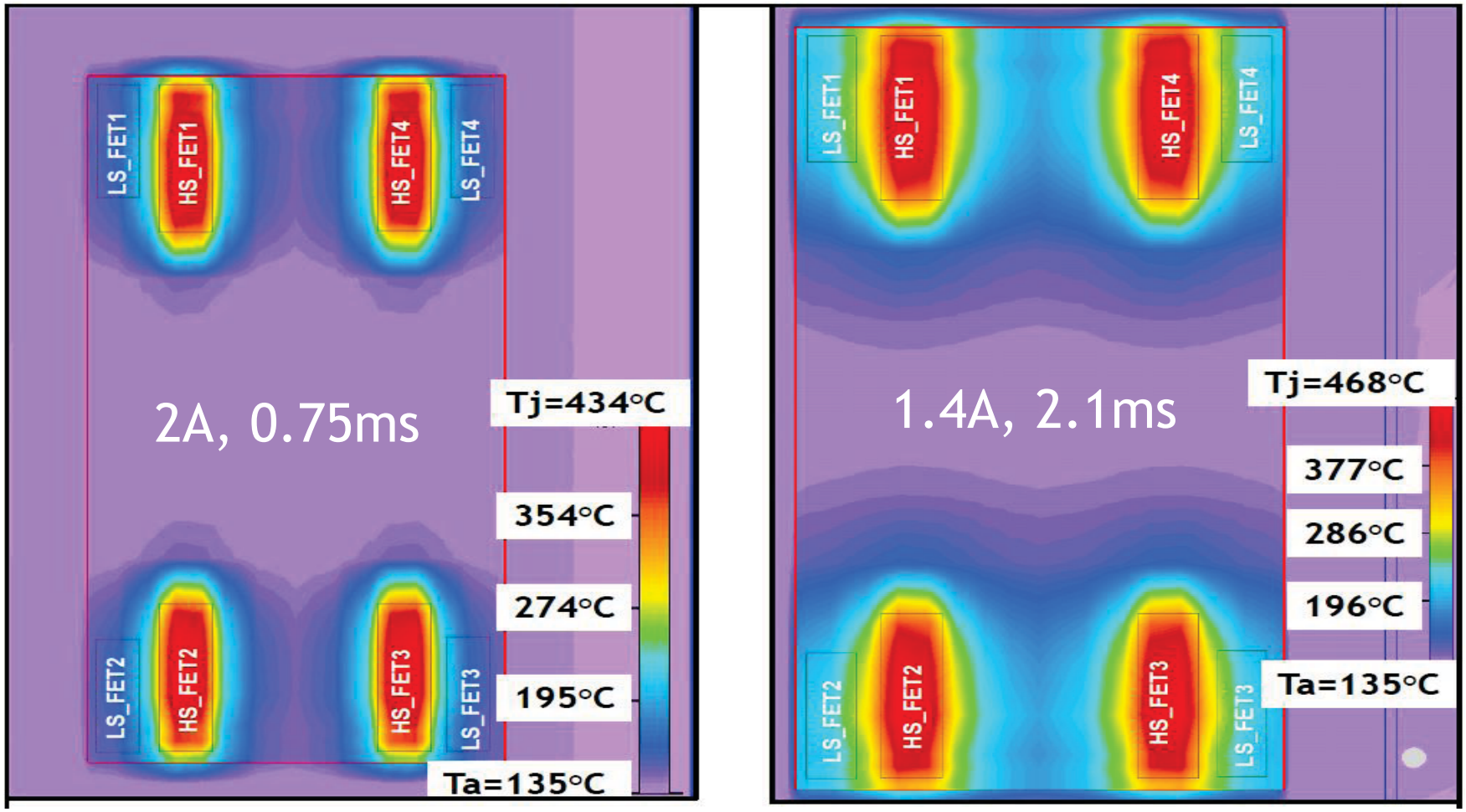




Ambient Temperature = Ta = 135°C.

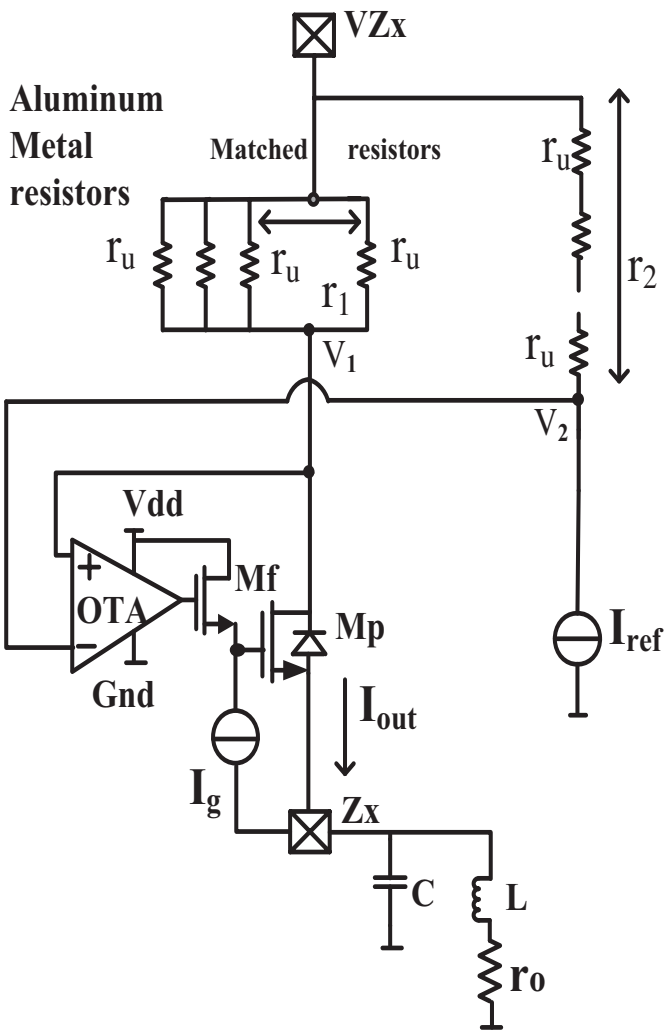
Deployment event : Junction temperature rise (Tj) monitored at the center and gate driver locations of the HS_FET.

Isothermal Plots



- Tj (Junction temperature of the HS_FET reaches ~ 460°C.
- No SPICE model for temperatures > 200°C

HS_FET Current Regulation, Layout Strategy

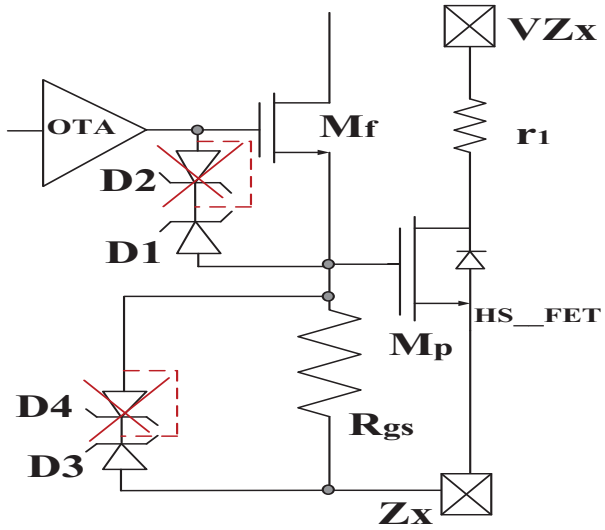


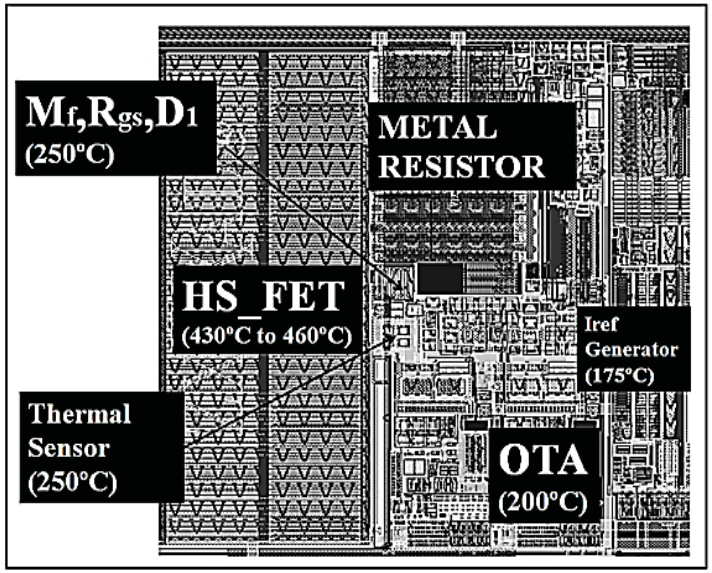
Layout Strategy

Centre of HS_FET is 460°C.

- OTA, I_{ref} generator to be placed where T_j<200°C. (Simulatable !)
- M_f and I_g is a source follower.
- Size M_f such that it can drive $2I_g$ => Place M_f and current source I_g in the area where T_j is ~200°C to 300°C.
- Works even if we can simulate the whole circuit only till 200°C.

HS_FET Current Regulation and DFMEA





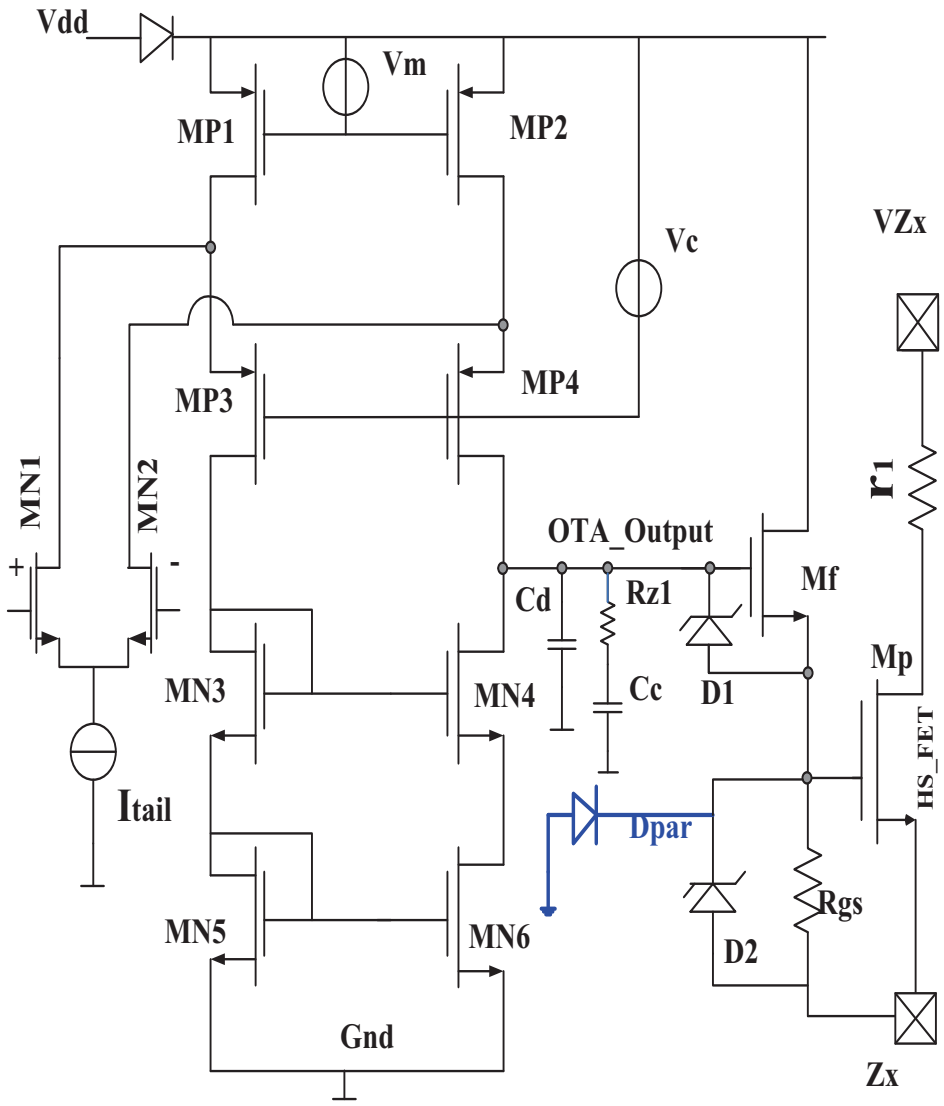
- Mf drives Rgs instead of Ig. Rgs ensures Vgs <Vth for Mp at power up. Mp not turned ON inadvertently.
- *Source follower with resistive load better than current source load.*

- Mf and Mp need Vgs protection. At 300°C, any forward leakage of D2 will reduce OTA's output impedance.

⇒ Avoid forward diodes D2 and D4 to mitigate risk based on DFMEA.

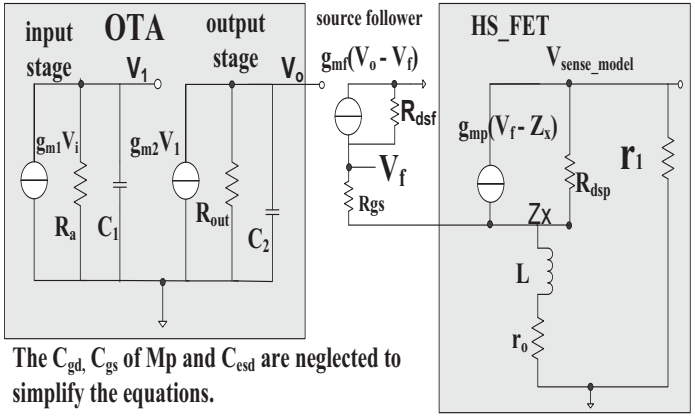
⇒ Off state leakage @ 5V is traded off. " µA" leakage still better than "nA".

Internal Free Wheeling Path



- When the HS Driver turns OFF, the free wheeling current will still flow through the HS_FET.
- This is feasible since the gate of the HS_FET is clamped to -0.7V due to Dpar (N-diffusion connected at the gate)
- Eliminates external Schottky diodes.

Small Signal Analysis, HS_FET with OTA



The C_{gd}, C_{gs} of Mp and C_{esd} are neglected to simplify the equations.

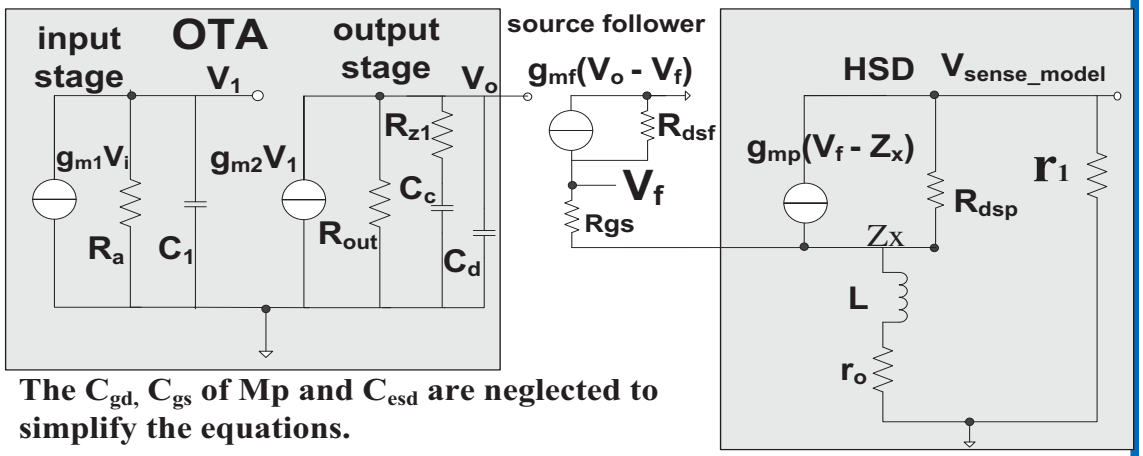
$$\left(\frac{g_{mp}}{1+g_{mp}r_o}\right)\sim r_o \quad if \quad g_{mp}r_o \geq 1$$

$$H(s)\sim \frac{g_{m1}R_a g_{m2}R_{out}r_1}{r_o\left[\left(1+sR_{out}C_2\right)\left(1+s\frac{L}{r_o}\right)\right]}$$

$$f_{p1}=\frac{1}{2\pi R_{out}C_2};\quad f_{p2}=\frac{r_o}{2\pi L};$$

$$f_\tau \approx \frac{1}{2\pi}\sqrt{\frac{g_{m1}R_a g_{m2}r_1}{LC_2}};$$

Before Compensation



The C_{gd}, C_{gs} of Mp and C_{esd} are neglected to simplify the equations.

$$H(s)=\frac{g_{m1}R_a g_{m2}R_{out}\left(\frac{g_{mp}}{1+g_{mp}r_o}\right)r_1\left(1+sR_{z1}C_c\right)}{\left[1+sR_{out}C_c+s^2\left(LR_{out}C_c\left(\frac{g_{mp}}{1+g_{mp}r_o}\right)\right)\right]}$$

When $r_o > 1\Omega$, $\frac{g_{mp}}{1+g_{mp}r_o}\sim r_o$

$$H(s)=\frac{g_{m1}R_a g_{m2}R_{out}r_1\left(1+sR_{z1}C_c\right)}{r_o\left[1+sR_{out}C_c+s^2\left(\frac{LR_{out}C_c}{r_o}\right)\right]}$$

$$f_{p1}=\frac{1}{2\pi R_{out}C_c}$$

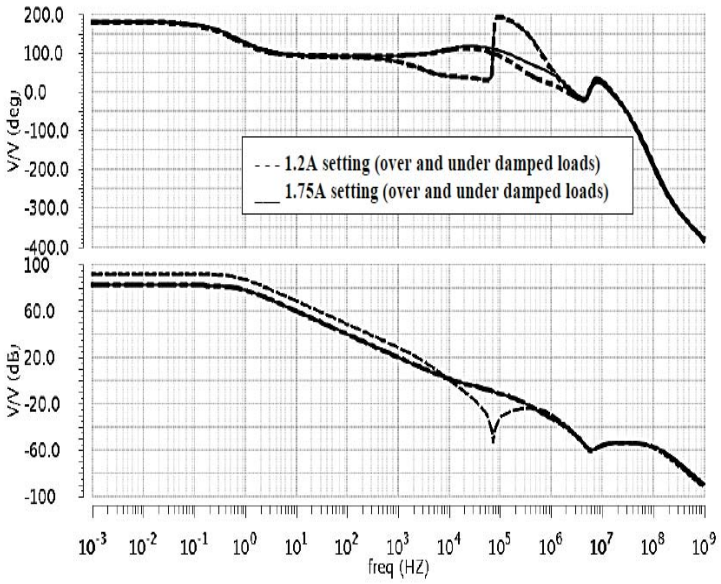
$$f_{p2}=\frac{r_o}{2\pi L}$$

$$f_{z1}=\frac{1}{2\pi R_{z1}C_c}$$

$$f_\tau=\frac{g_{m1}R_a g_{m2}r_1}{2\pi r_o C_c}$$

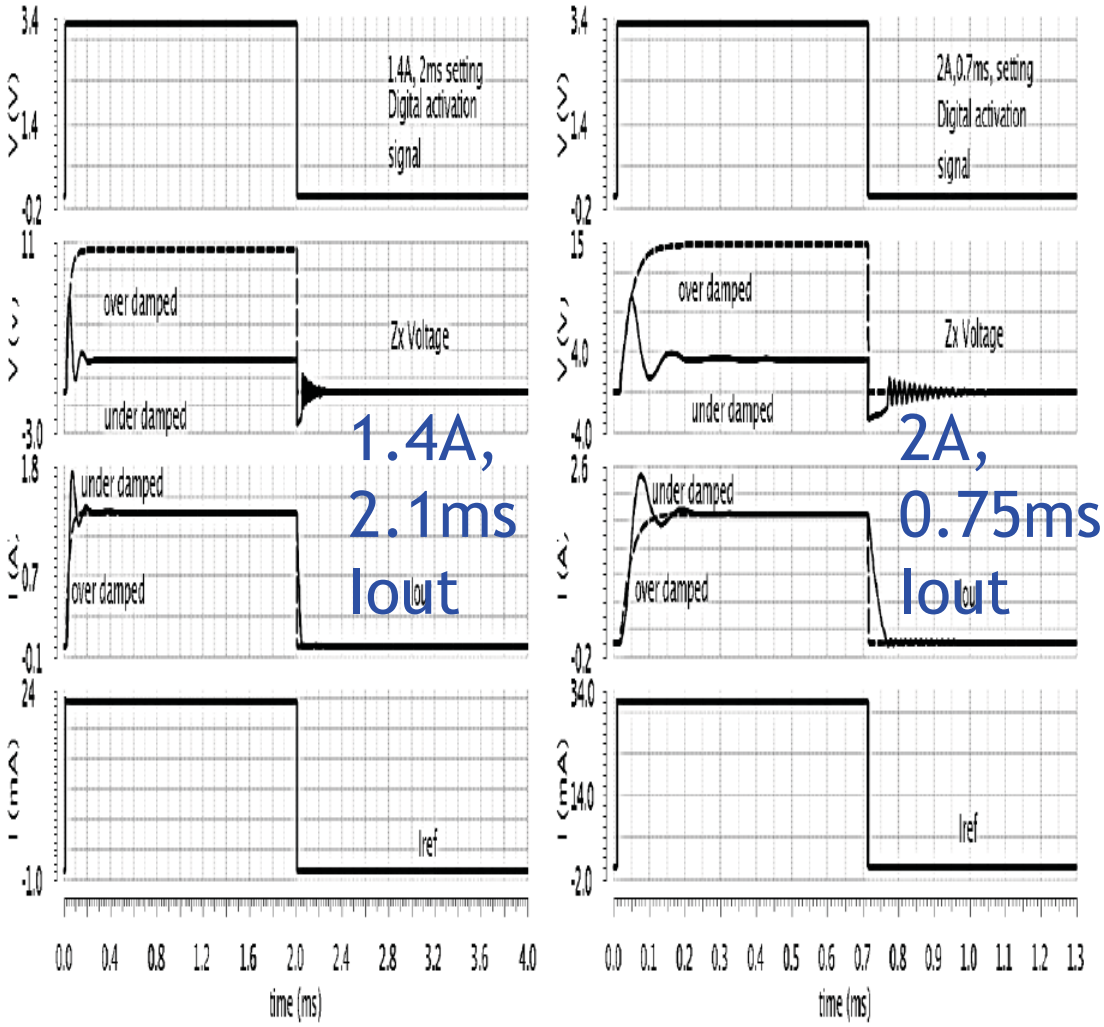
After traditional Compensation

Stability- Simulation Results HS_FET



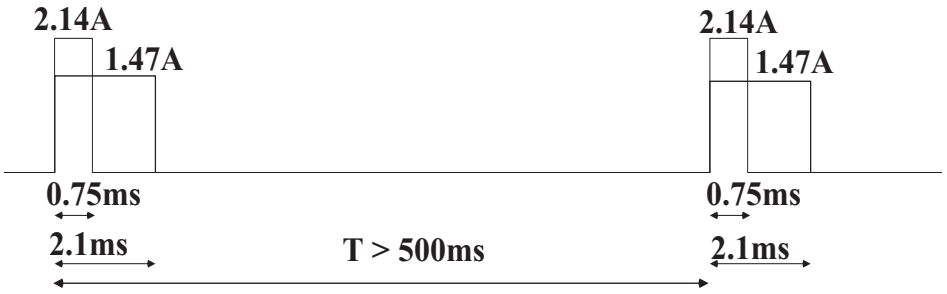
Bode Plot

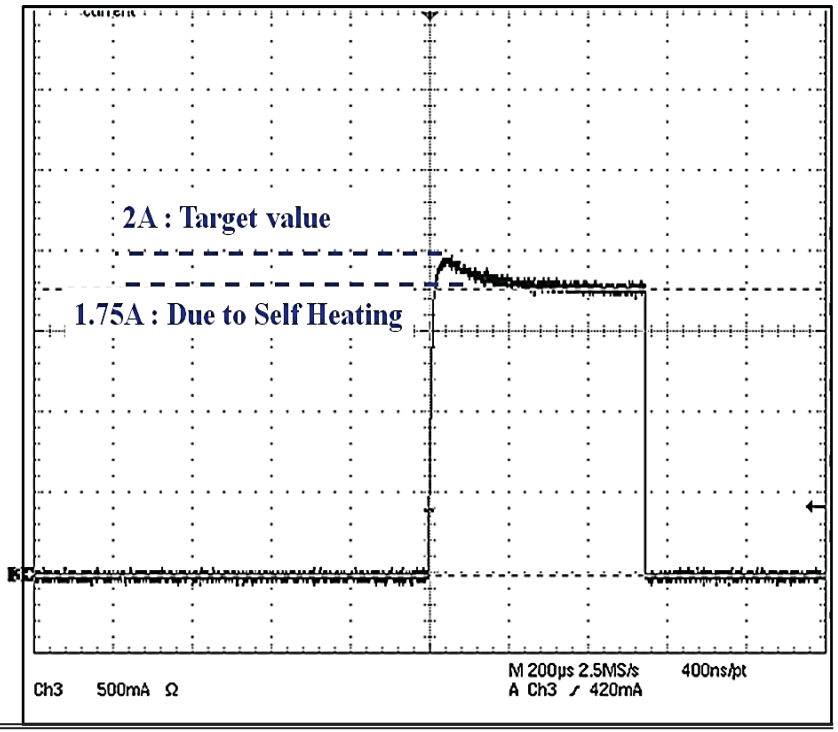
Over damped (1µH, 8Ω)
Under damped (100µH, 1Ω)



Transient simulations

Metal Resistor Self Heating

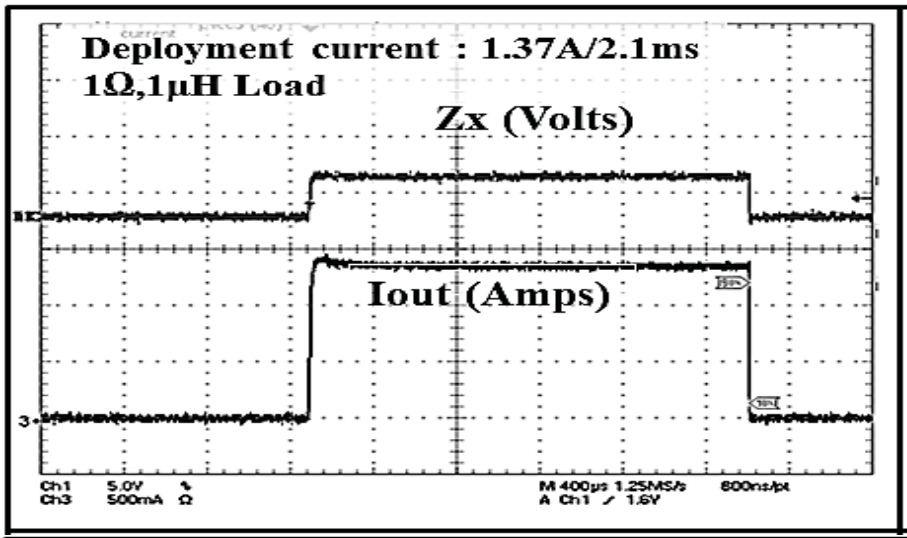


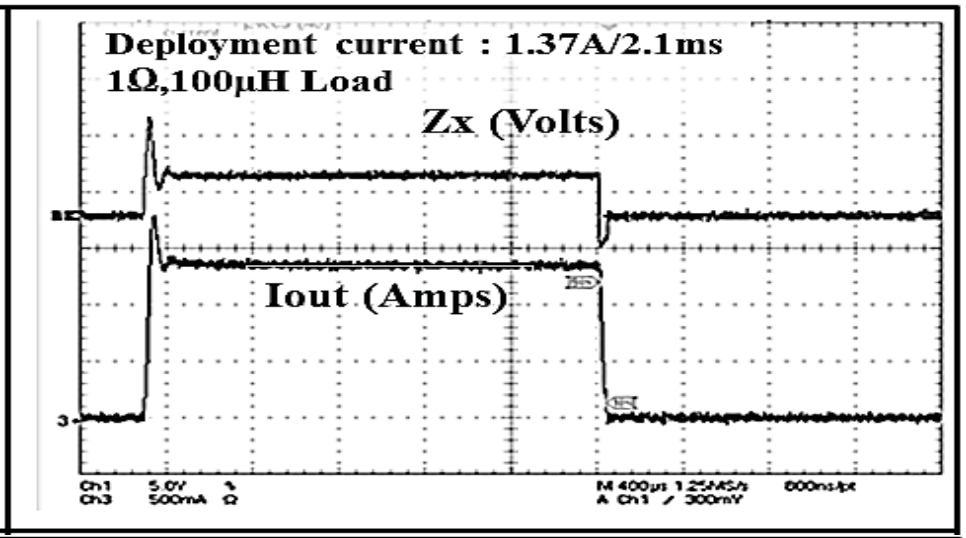


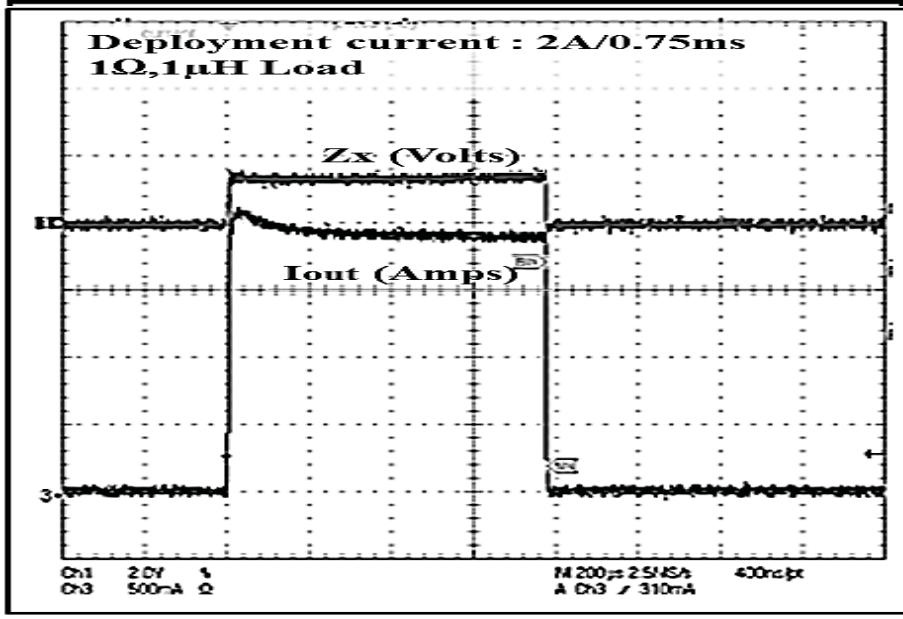
- Metal width -> current density between J_{PEAK} and J_{RMS}. Choose 25mA/µm.
- Self heating can be compensated by increasing Iref.

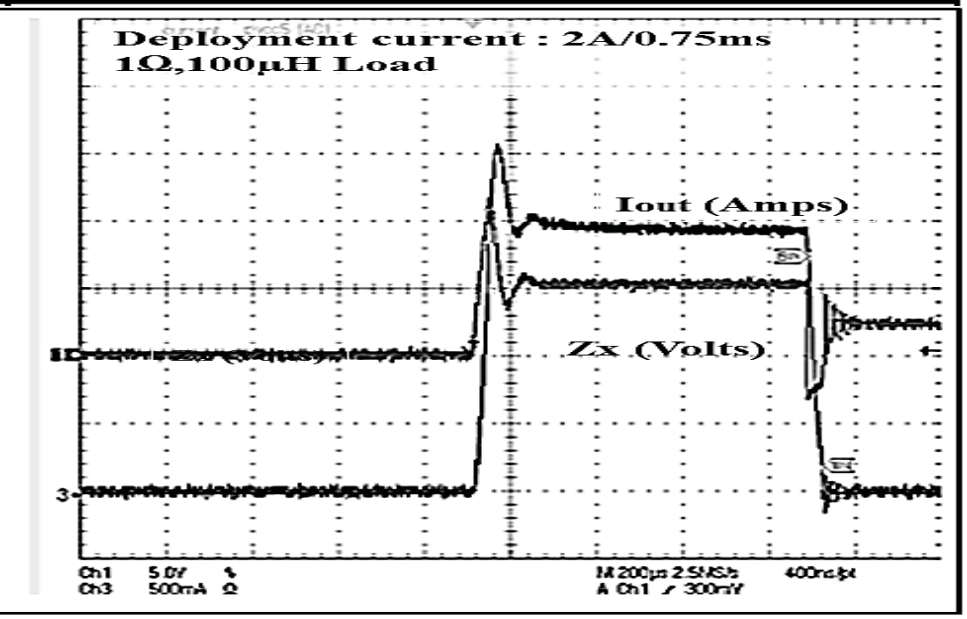
Types of Current Density	Notation	Thumb Rule mA/µm	Application
PEAK	J_{PEAK}	50	ESD Currents
RMS	J_{RMS}	10	PWM Currents
DC	J_{DC}	1	DC Currents

Measurements : HS_FET Current Regulation





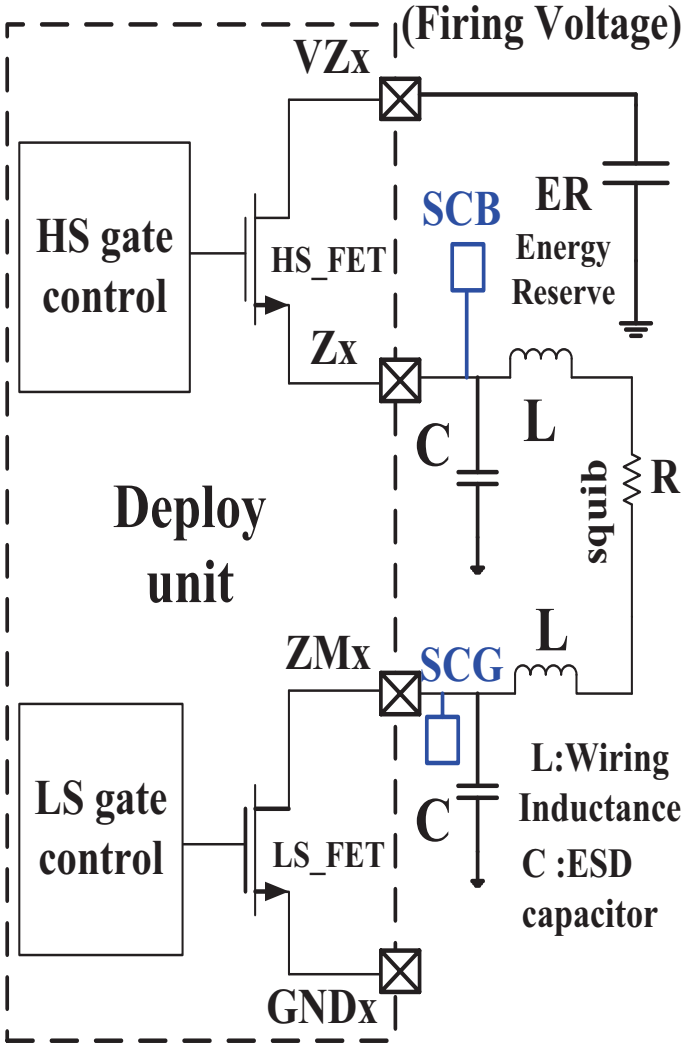




Short to Ground, Battery Conditions

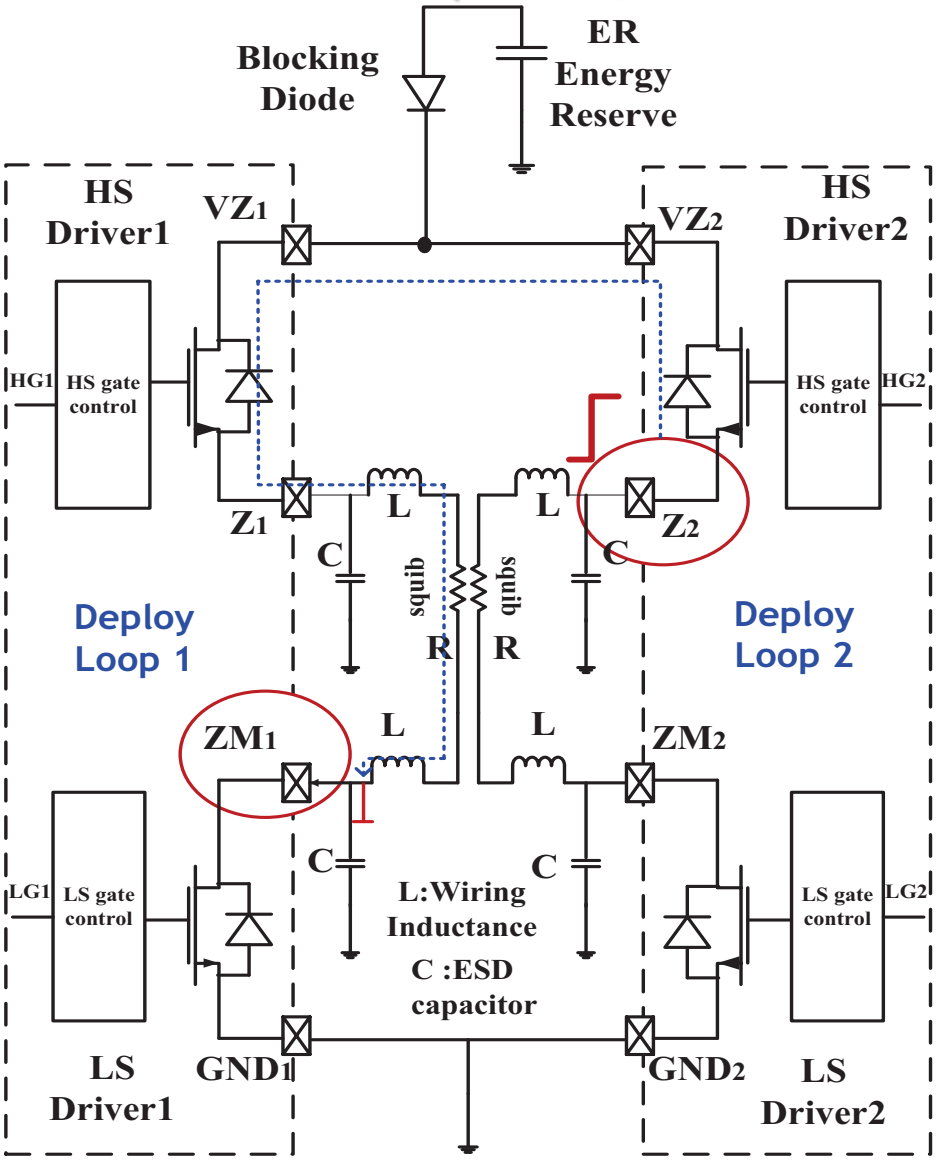
- Short to Ground (SCG), Short to Battery (SCB)
- CrossLink
- Energy Level – Unpowered State
- Active Discharge Circuit
- Dynamic SCG and circuit improvements

HS_FET Current Regulation, SCG,SCB Faults



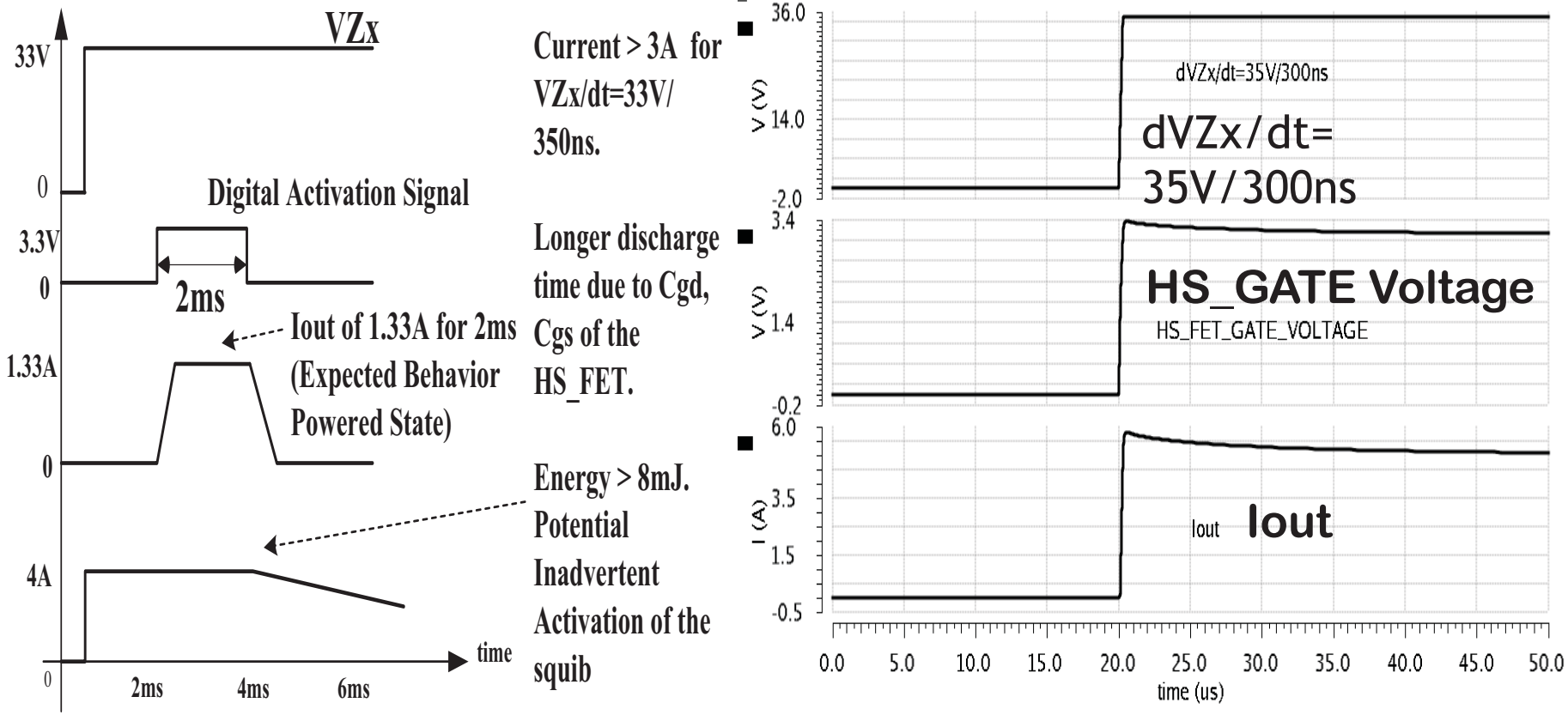
- Probability of single faults (Short Circuit to Ground (SCG) or Battery (SCB)) is very high. Circuits have to be designed to tolerate this.
- Simultaneous faults on same channel (SCB and SCG) has low probability.
- *SCG on the output of Driver 1 and SCB on the other Driver is highly probable.*

Cross Link (SCB, SCG on individual channels)



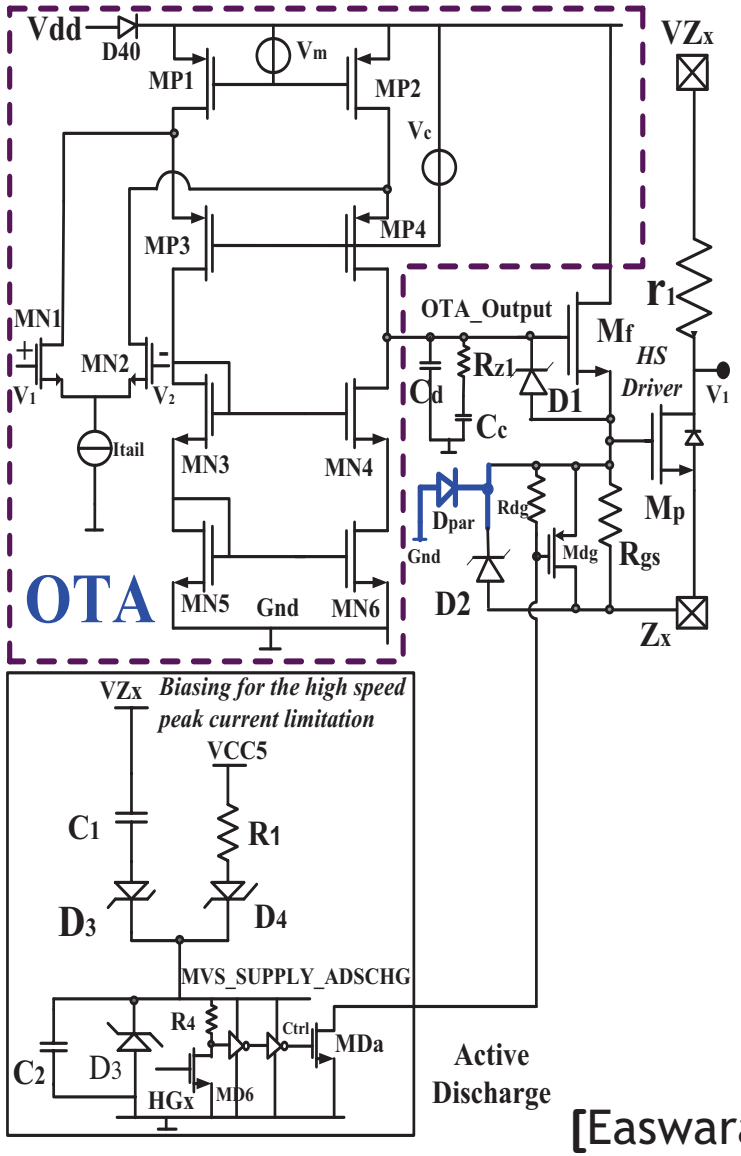
- Z2 -> SCB & ZM1 -> SCG is a High probability event.
- Dynamic SCB on Z2 with ZM1 at ground is critical for the Deploy loop 1.
- *Energy level > 8mJ on Squib_CH1 due to spike on Z2 (VZ1,VZ2) is not allowed.*

Energy Level Violation - Unpowered state SCB

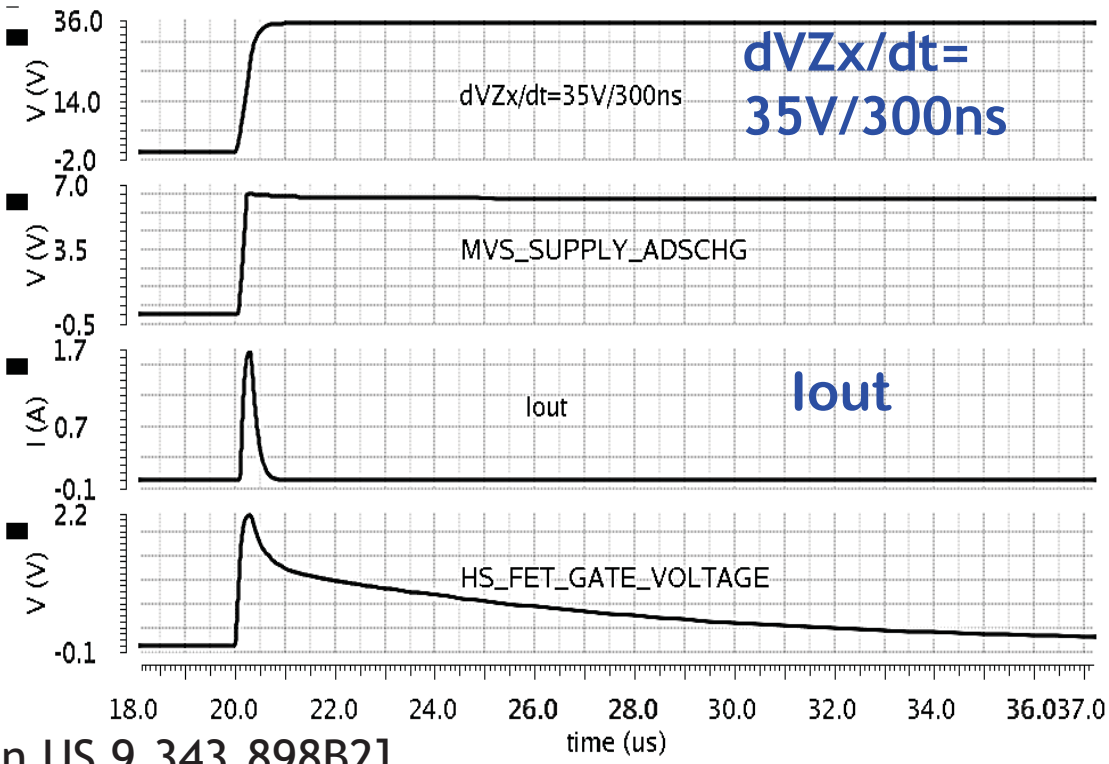


Passive discharge : R_{gs} resistor ensures gate is discharged (Vgs~0V). Fast transients need active discharge to quickly discharge the gate to meet 5A,4µs spec.

Active Discharge in Unpowered State



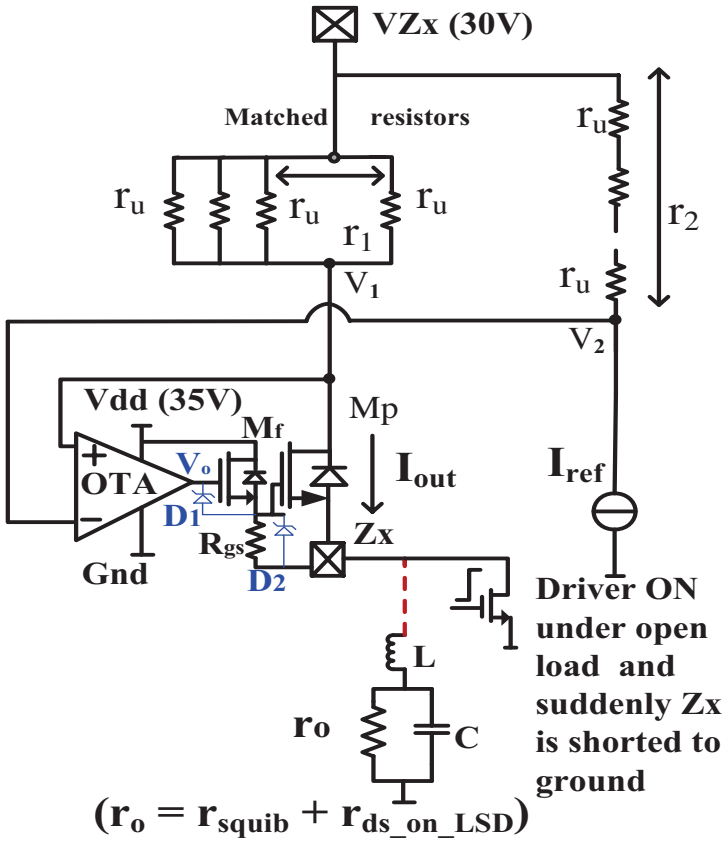
- Passive discharge is Rgs resistor that keeps the Gate-source junction at 0V without turning ON the powerFET.
- For very fast transients, active discharge speeds up the discharge.

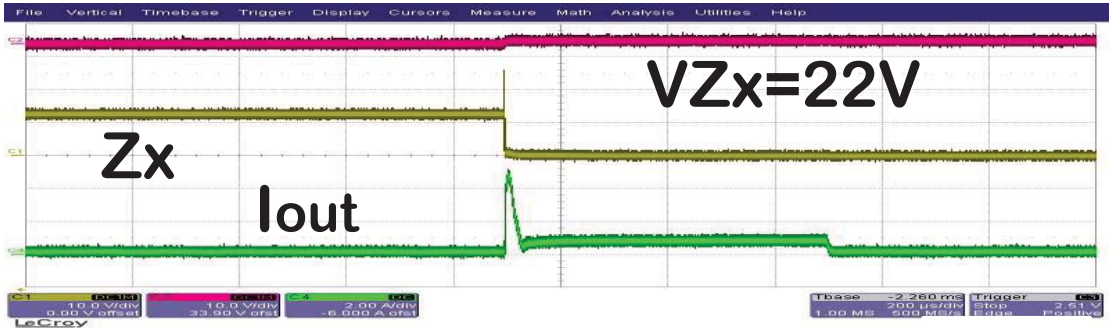


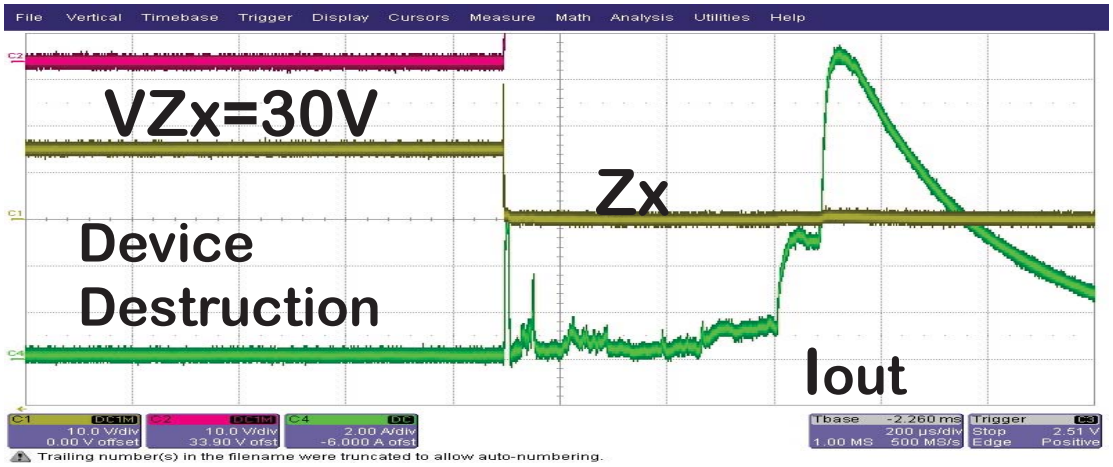
[Easwaran US 9,343,898B2]

HS_FET Current Regulation, SCG Scenario

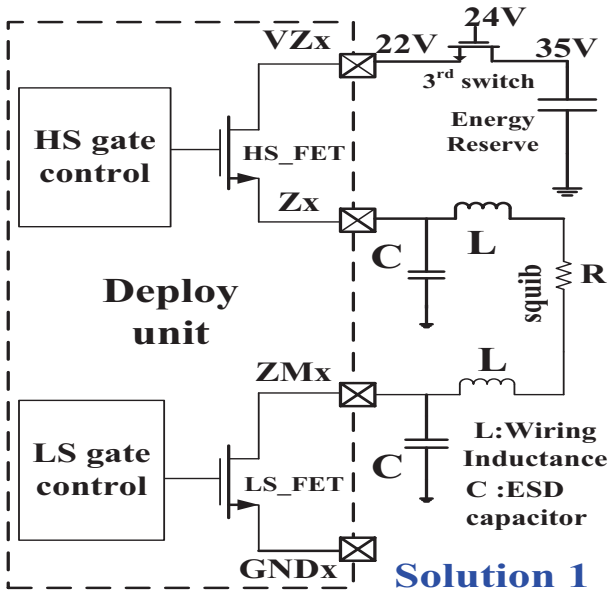
A dynamic SCG during deployment -> Open to Short test. VZx=22V, 6A,peak current. @ 30V VZx > 10A peak current is too high ? How to mitigate risk ?





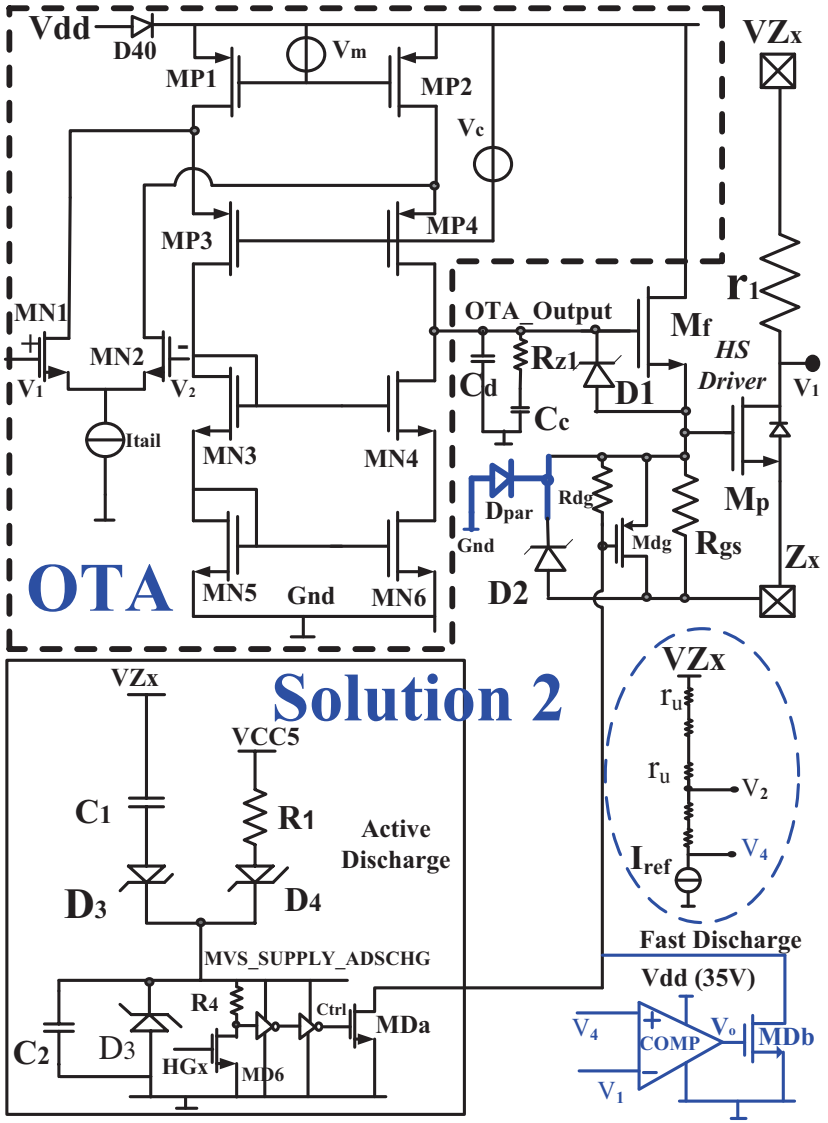


HS_FET Current Regulation, SCG Risk Mitigation



DFMEA showed high risk under open to short tests. (High peak currents)

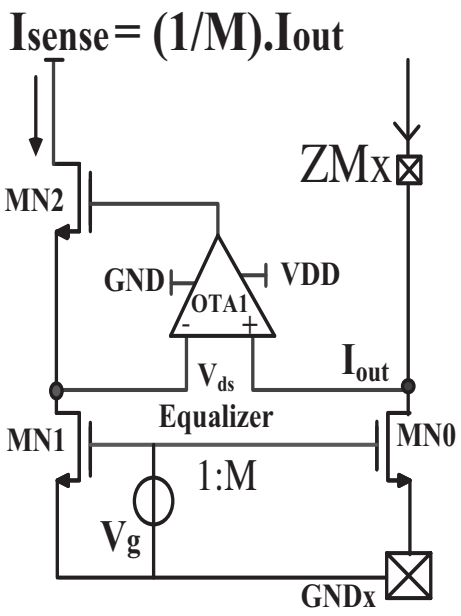
- Peak current reduced in 2 ways.
- Solution 1 : 3rd Switch, VZx=22V.
- Solution 2 : Add fast Discharge Circuit. V4 generated from same r2 resistor string.

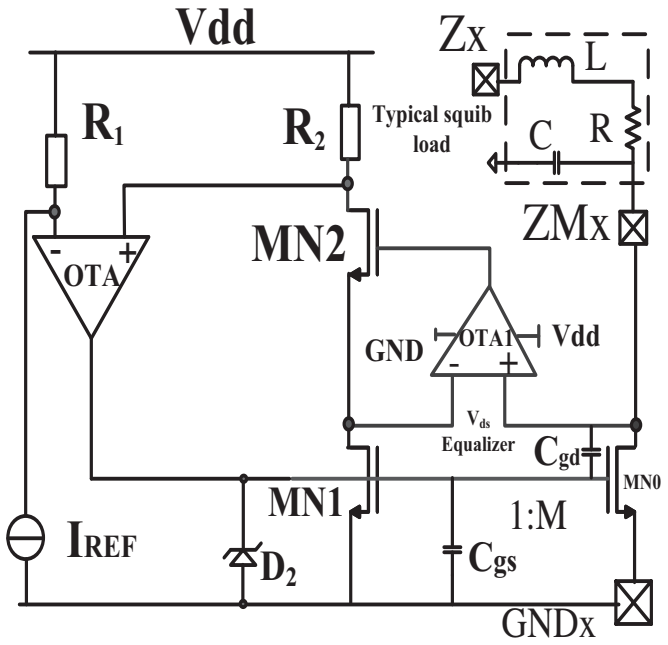


Low Side (LS) Driver and Current Sensing

- LS Current Regulation
- Passive and Active Discharge

LS_FET Current Regulation





$$H(s) \sim -\frac{\frac{g_{mp}}{g_{dp}}\left[1+\left(\frac{sL}{R}-\frac{sC_a}{g_{mp}}\right)\right]}{\left[1+\frac{sL}{R}+s^2\frac{LC_a}{g_{dp}}\right]}$$

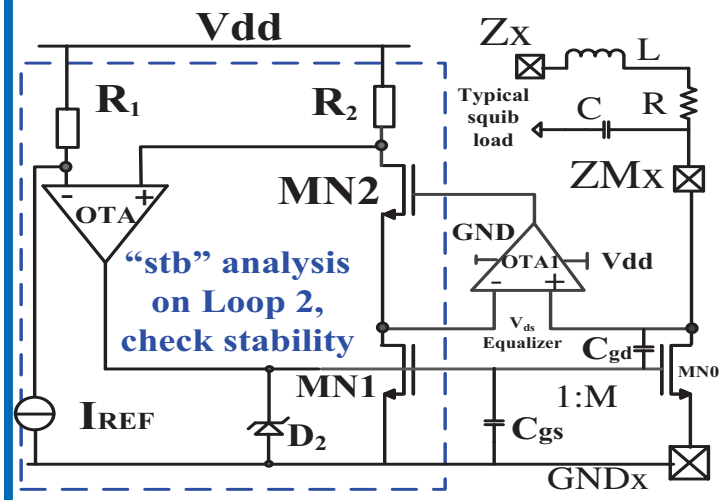
$$I_{limit} \approx \left(\frac{R_1}{R_2}\right) M I_{ref}$$

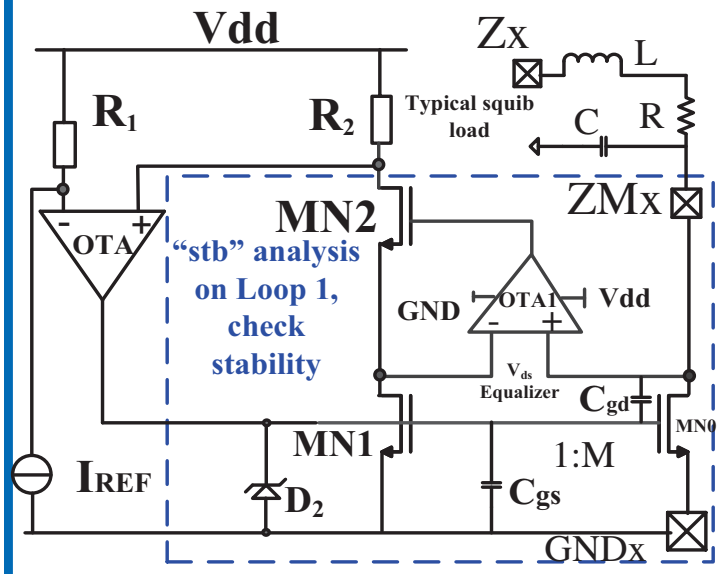
$$\Rightarrow I_{limit} \approx \left(\frac{312\ K\Omega}{225\ \Omega}\right)(64)(34\mu A) \sim 3A$$

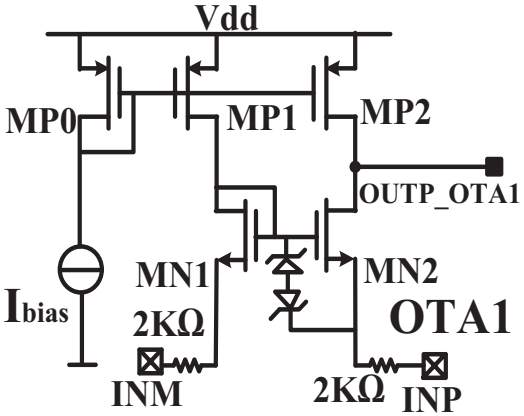
- LS_FET needs current limit of 3A when Zx has a SCB.
- A senseFET based current sensing and limiting/regulating circuit is needed. 2nd order transfer function H(s) from the gate to drain of MN0 (g_{mp}, g_{dp}, $C_{gd}=C_{gs}=C_a$) for L-C loads.
- 2 OTAs involved. OTA needs higher gain than OTA1.

  End Result -> Stabilize the loop with Cg,eff of MN0.

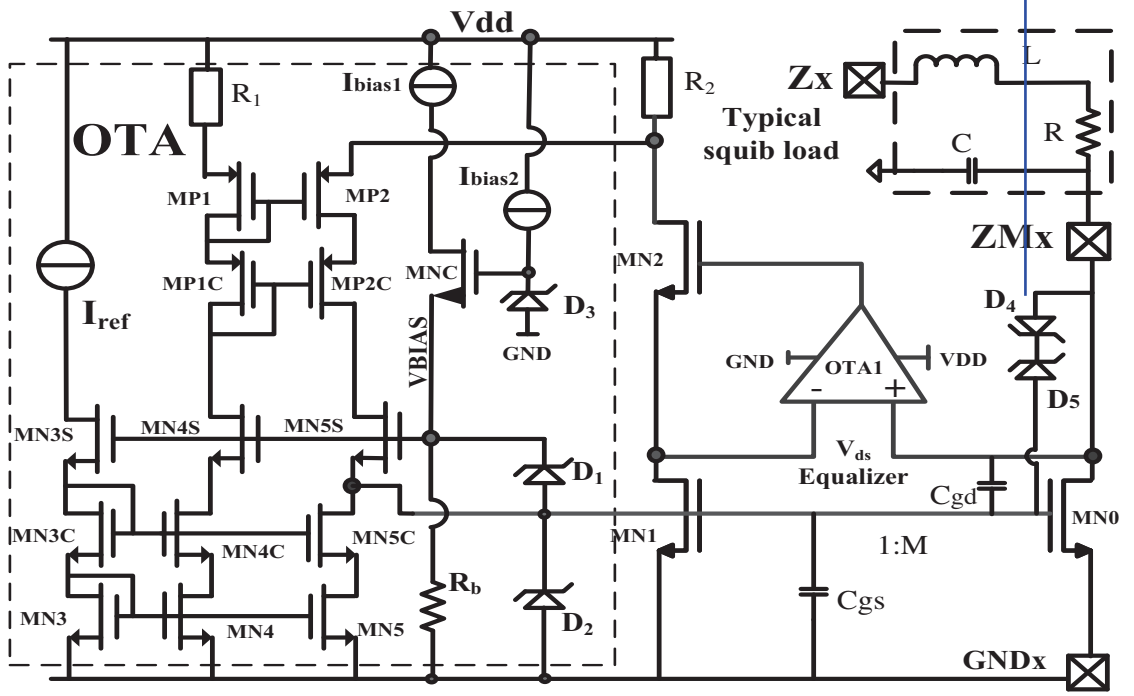
LS_FET SCB Stability Analysis



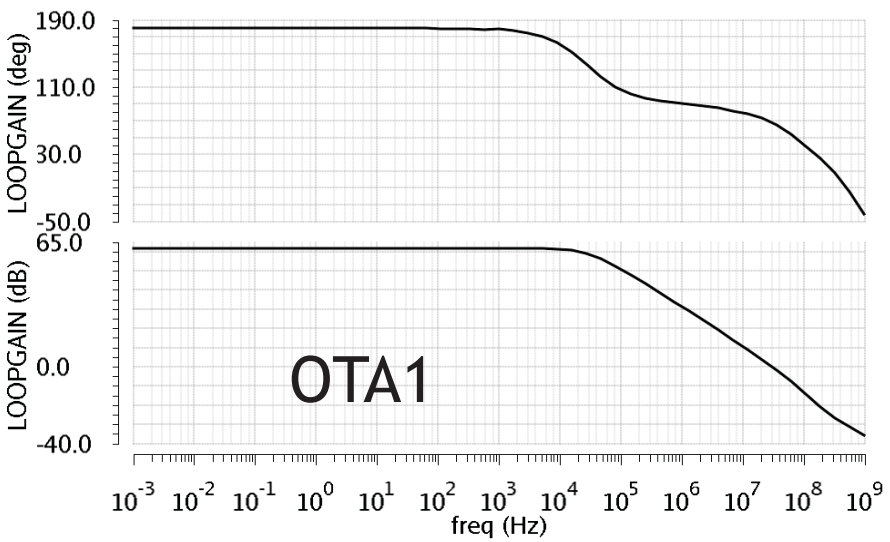


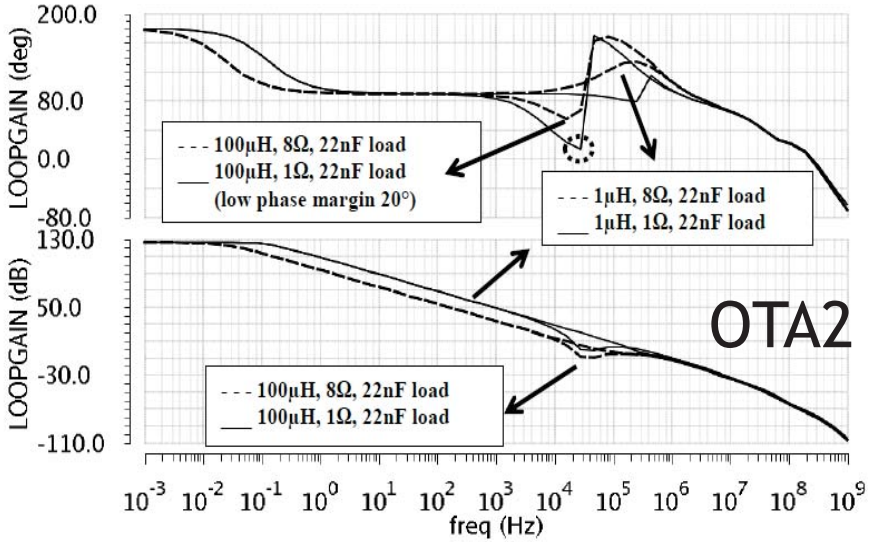


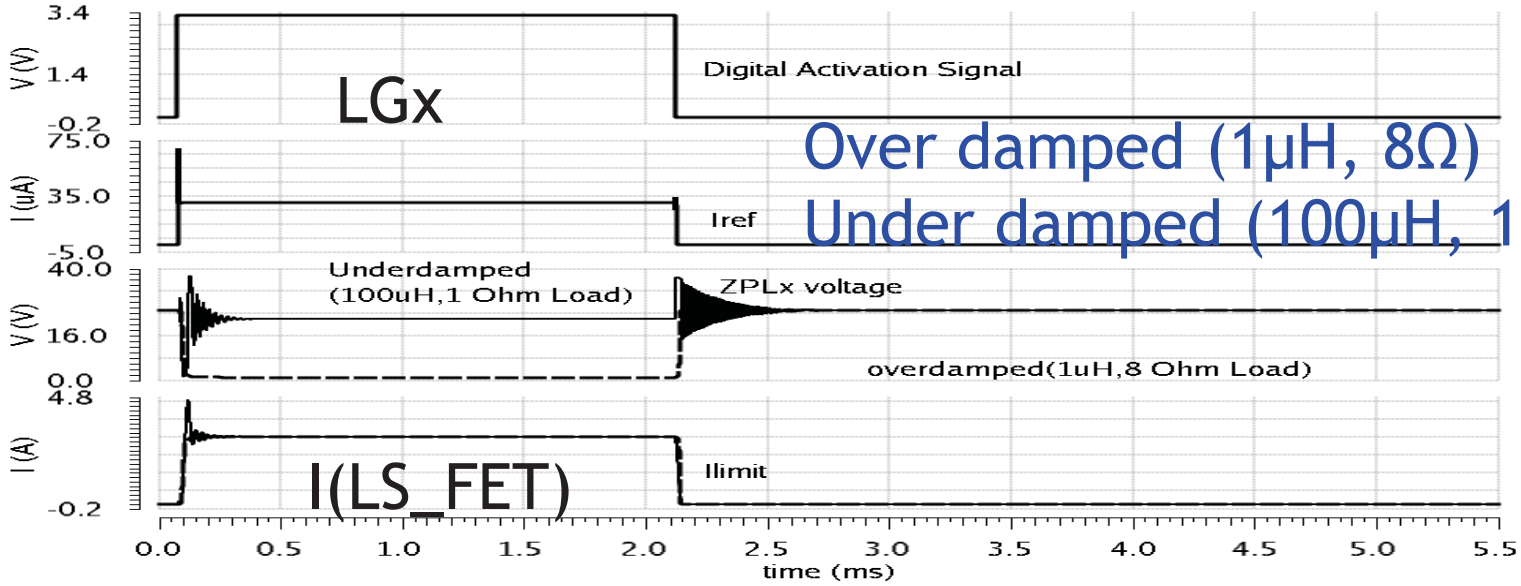
D4,D5 for Free-wheeling



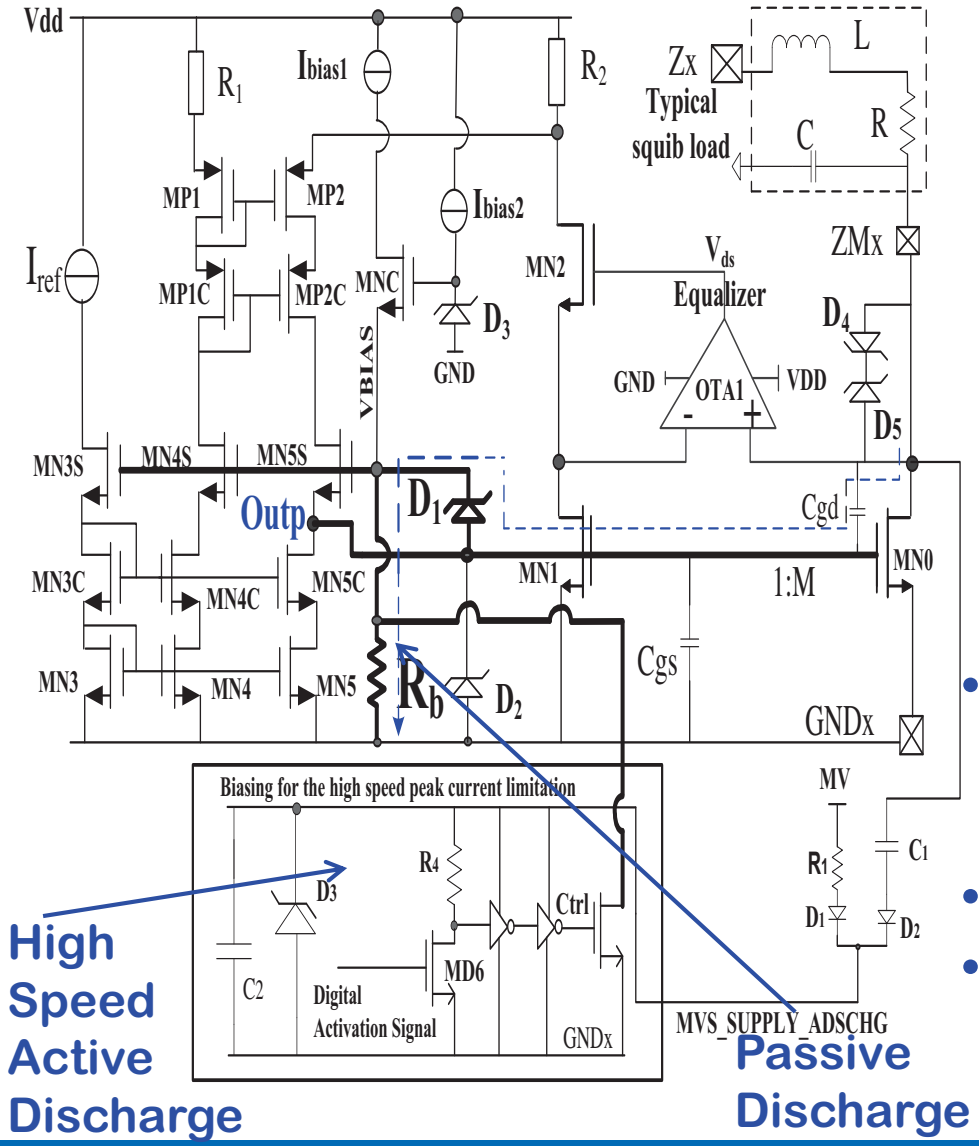
LS_FET Current Regulation, Simulation Results

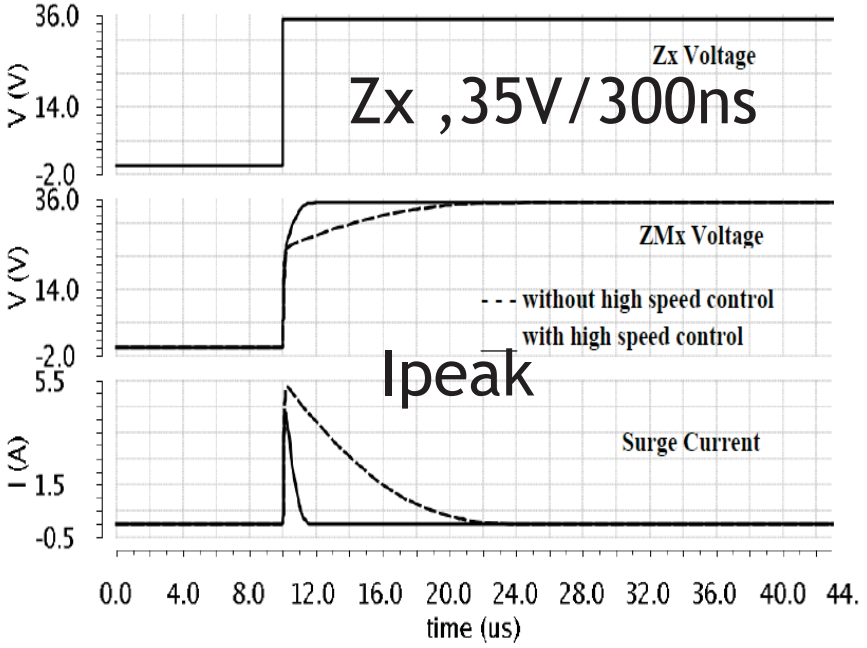






LS_FET Passive Discharge Concept

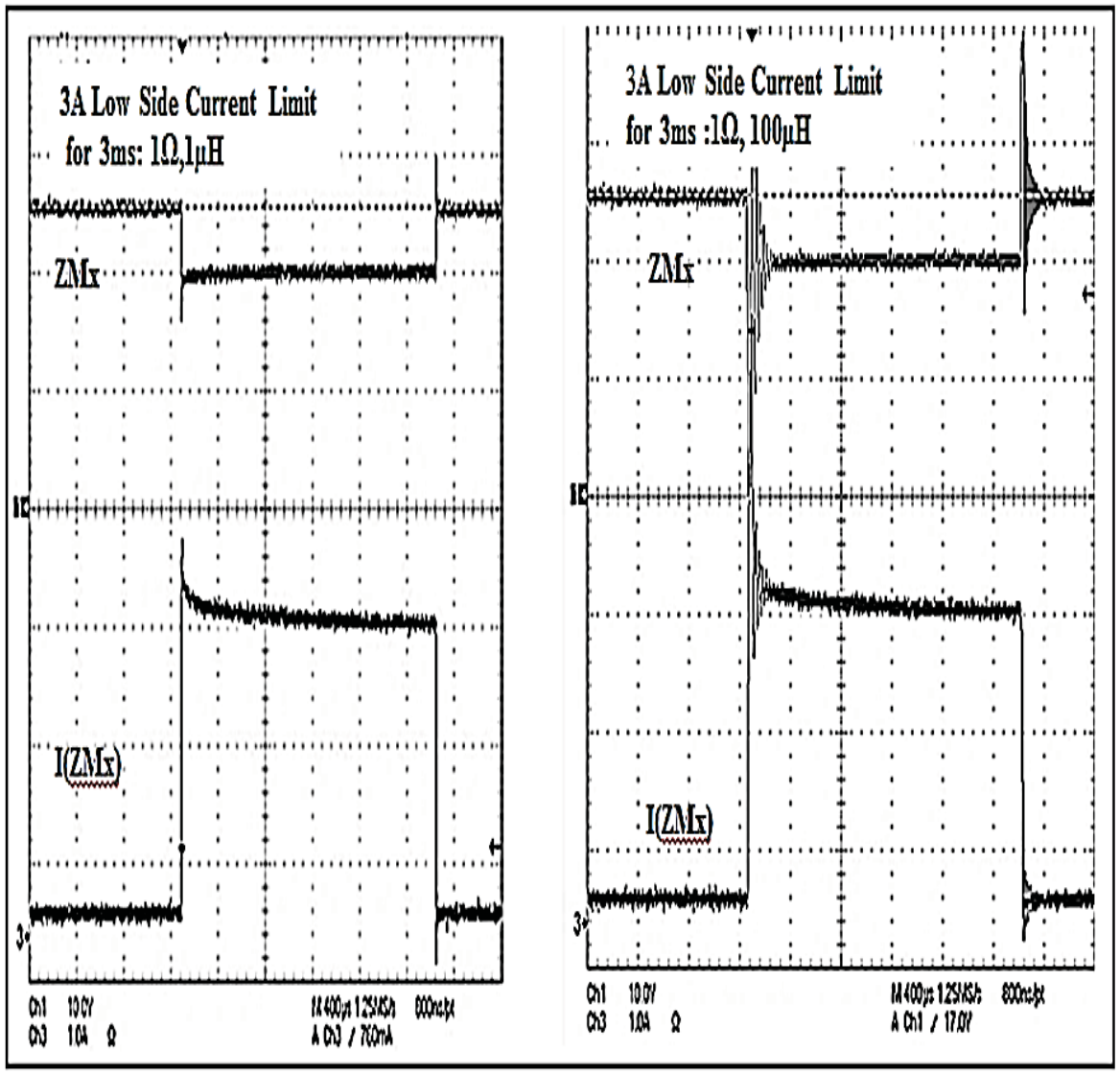


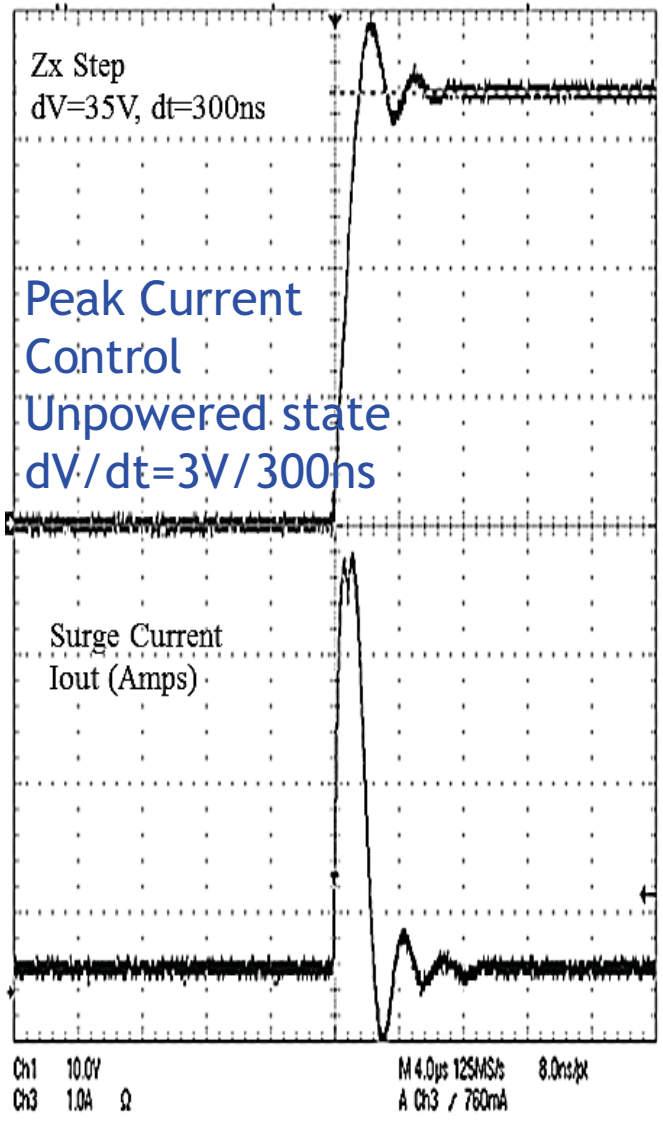


- Resistor at gate of MN0 not an option for passive discharge ("Outp" impedance is lowered).
- Rb at MN5 gate is the solution.
- Active Discharge speeds this up further.

[Easwaran US 8,553,388B2]

Measurements : LS_FET Current Regulation

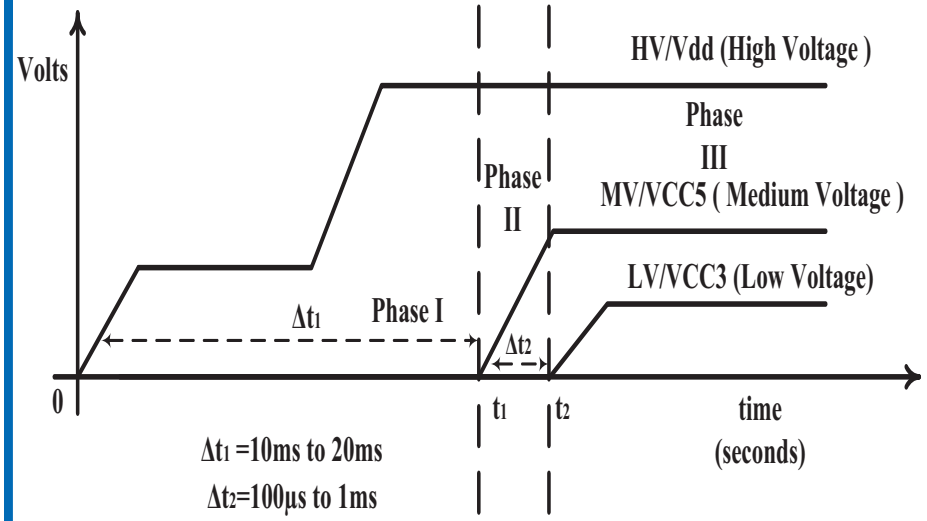




Biasing Schemes

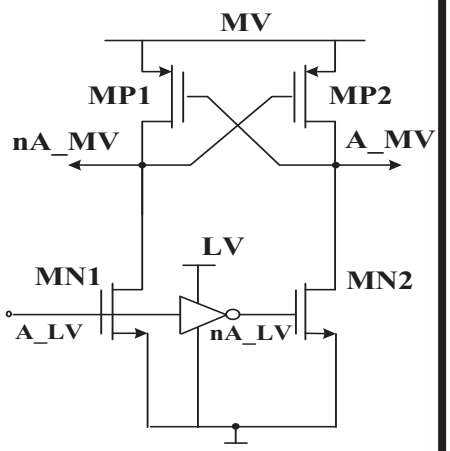
- Multiple Supply Voltage Designs
- Cross Coupled Level Shifters
- Maximum Current and Voltage Selectors

Multiple Supply Voltage Design Challenge

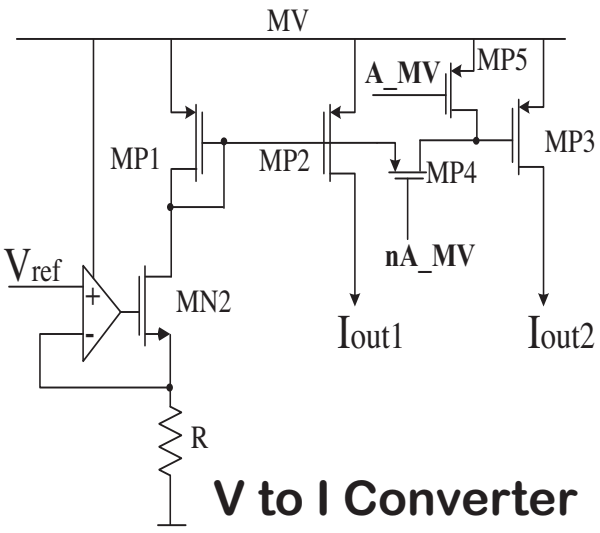


Phase I, Phase II : LV rail is not available.

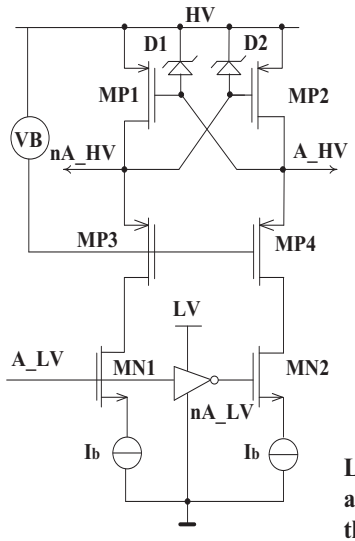
- nA_MV and A_MV can be either 0 or MV => This can activate or deactivated circuits inadvertently.
- V to I Converters can produce 0 current by turning OFF MP1 or avoid MP3 activation making Iout2=0
- A_HV if @ HV-12V, will turn OFF MP6 inadvertently.



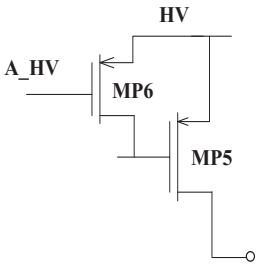
LV to MV Level Shifter



V to I Converter

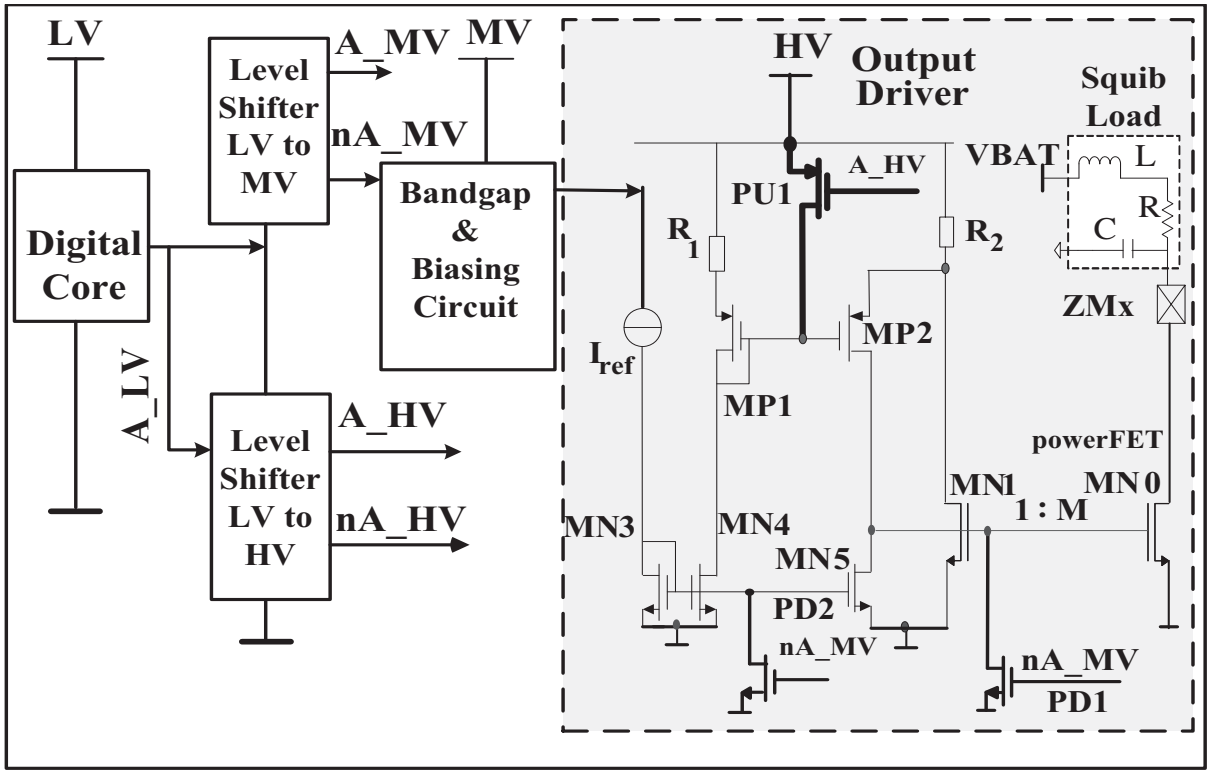


LV to HV Level Shifter



LV → HV Level shifter controlling the activation and the deactivation of MP5 through MP6

Levelshifters with voltage and current selectors



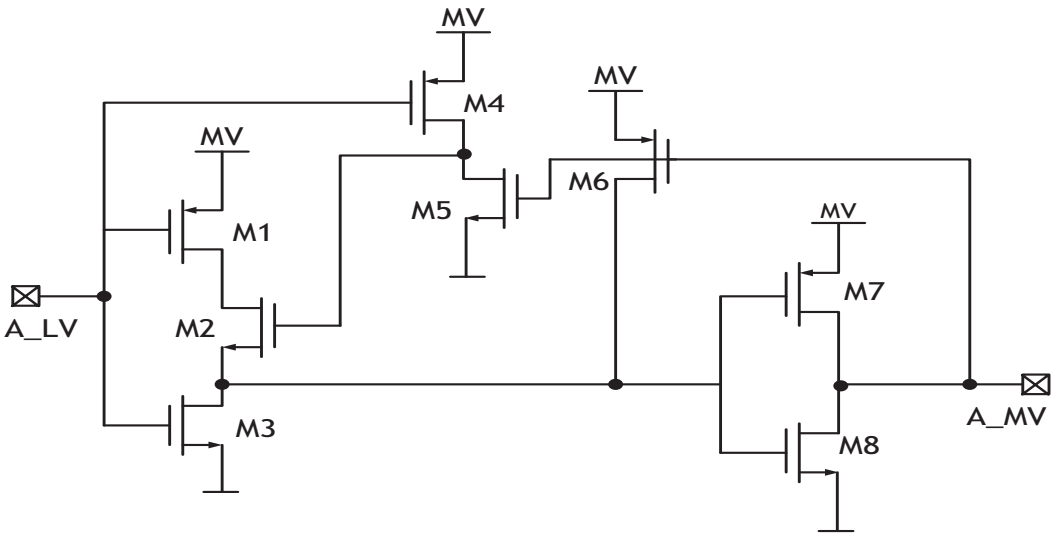
If HV,MV are present (LV=0V), possibly,
A_HV ~ HV
nA_MV ~ 0V
MN3, MN4 gates can float to ~ Vgs~Vth when Iref is not well defined.

⇒MP1, MP2 turned ON, MN1, MN0 gates can be higher than Vth.

⇒Inadvertent activation/ current flow from VBAT and squib can be deployed.

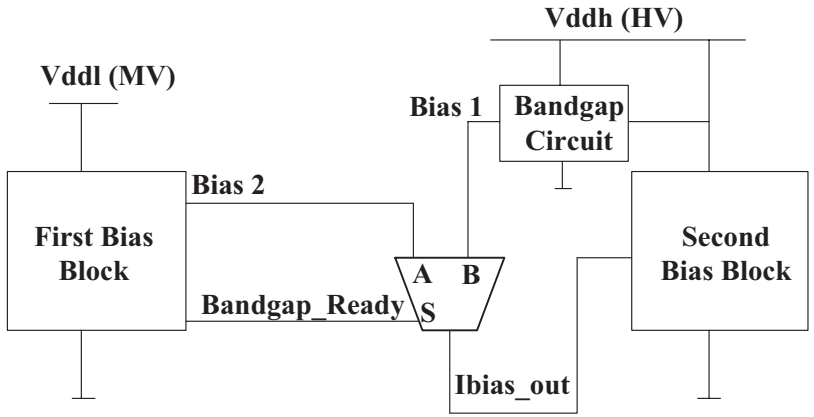
⇒ Proper pull up/down is essential.

Prior Art

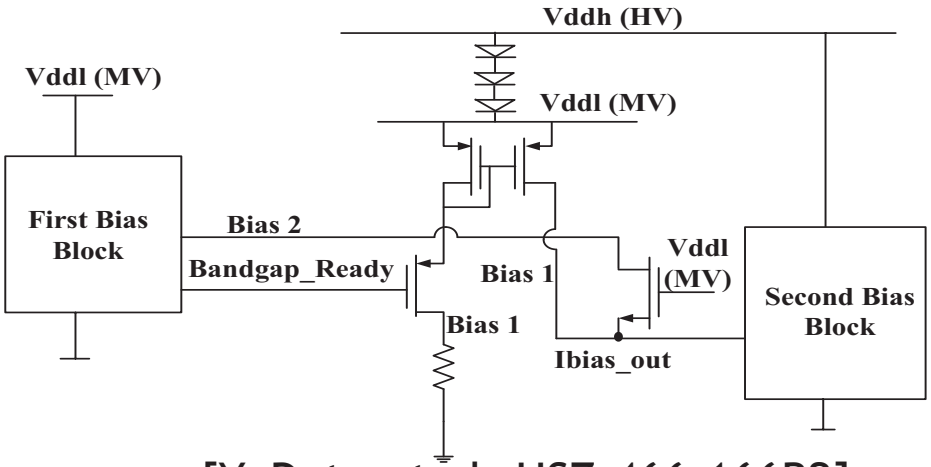


LV Rail Independent level shifters.
[M.H.Kim US7,683,667B2]

LV Rail Independent bias current generation



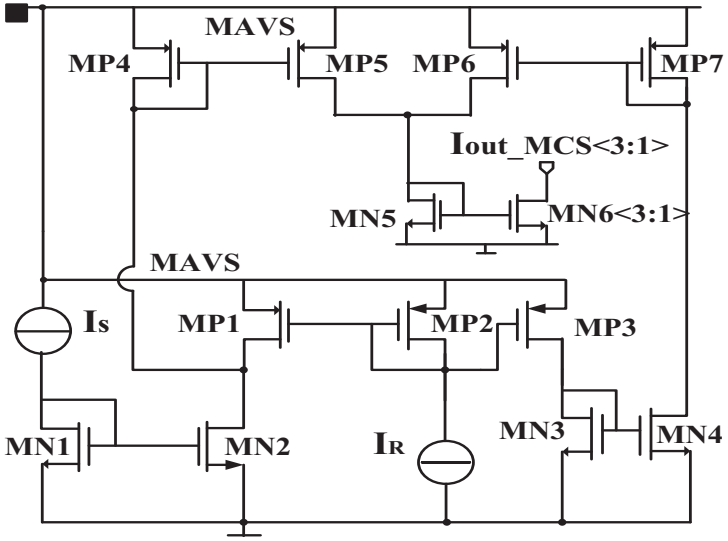
[C.Y. Chen US 7,391,595B2]



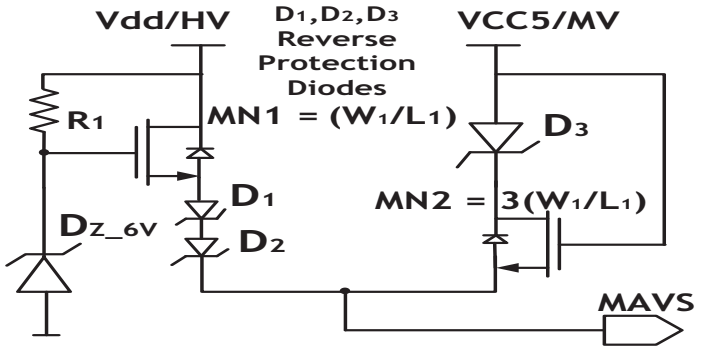
[Y. Date et al, US7,466,166B2]

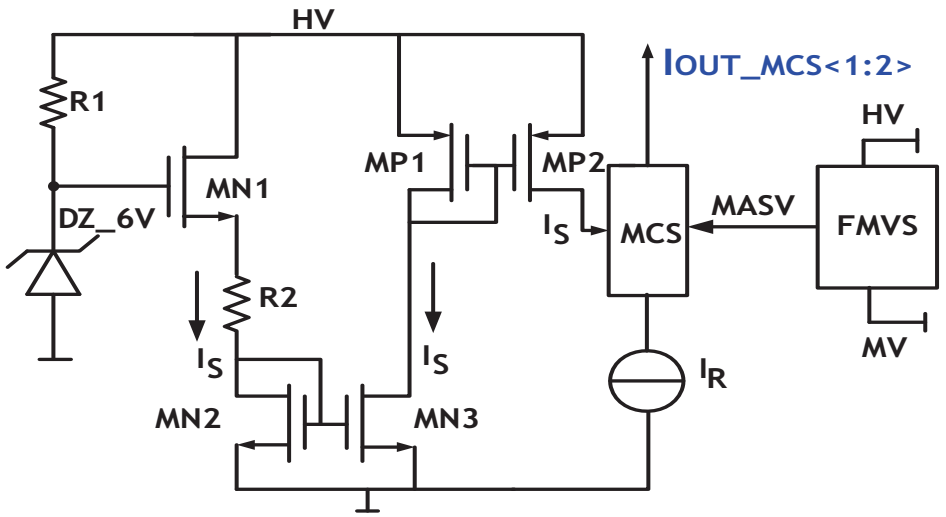
Levelshifters with voltage and current selectors

Max.Current Selector (MCS)

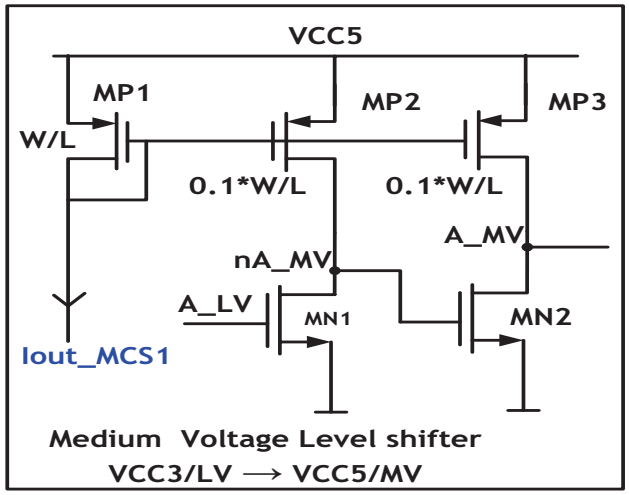


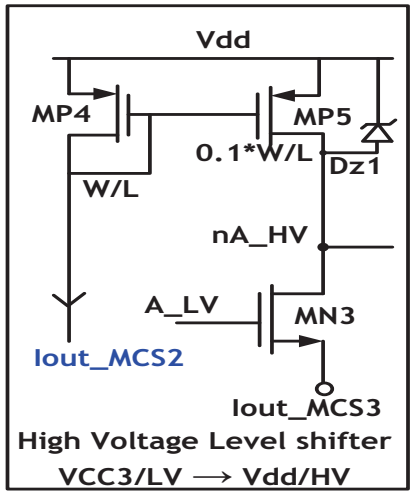
Fault Mode Voltage Selector (FMVS)





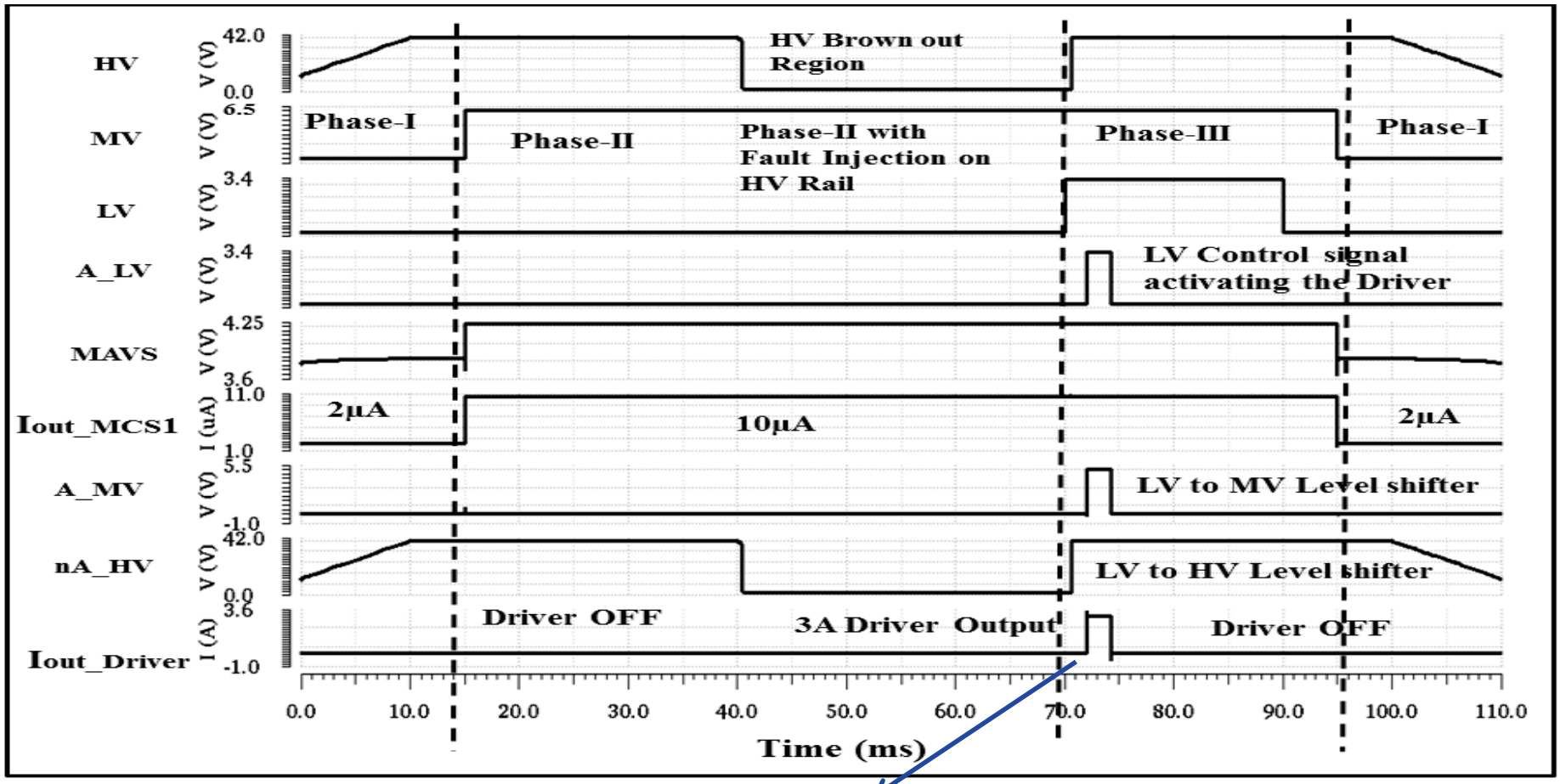
Logical "OR" of Currents and Voltages





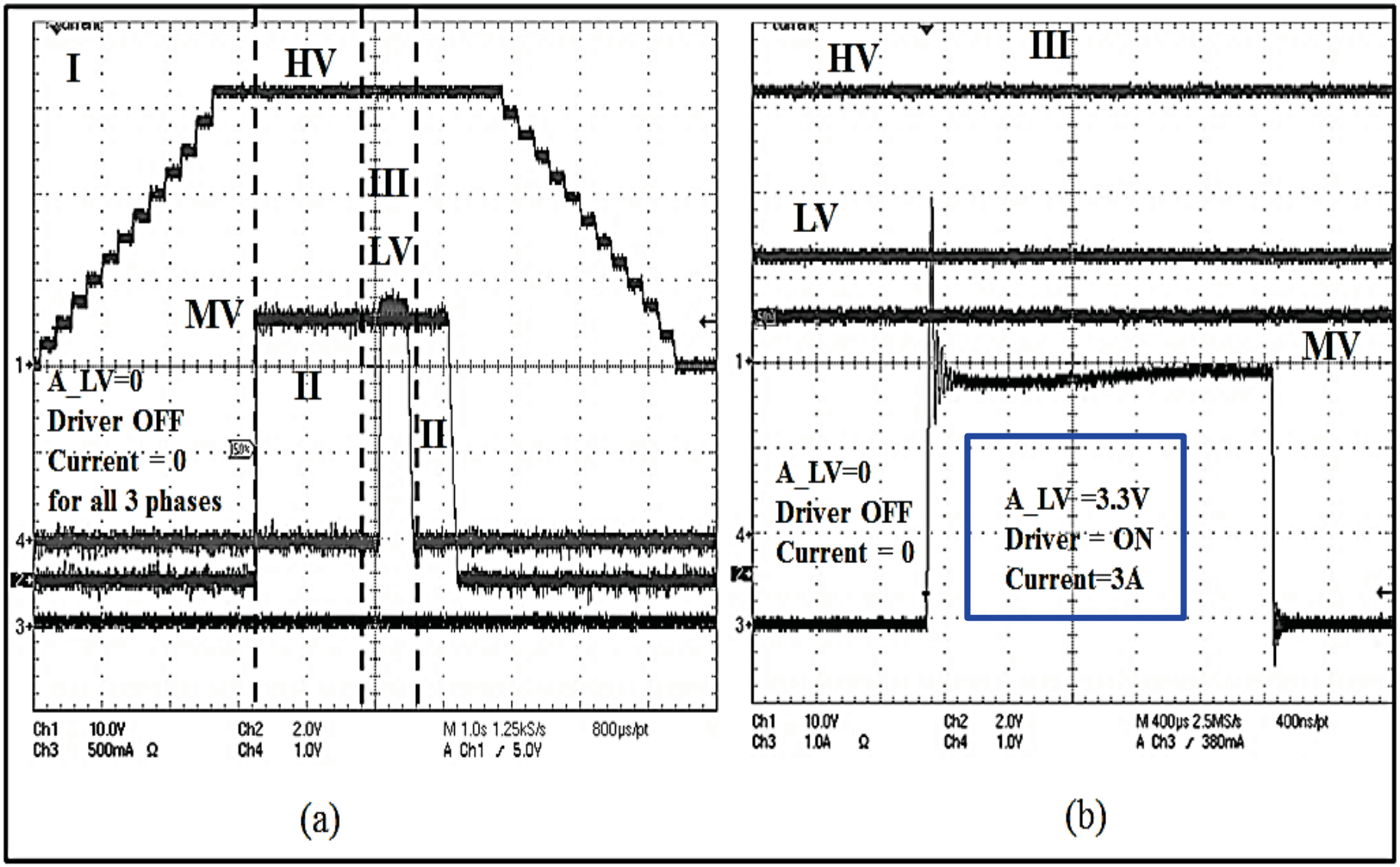
[Easwaran et al US 7,888,993B2]

Simulation Methodology



- Driver is active only when A_LV toggles to 3.3V .
- Driver Regulates current to 3A when A_LV is high. Otherwise its output is 0A.

Measurement Results - Power Up, LS_FET Test



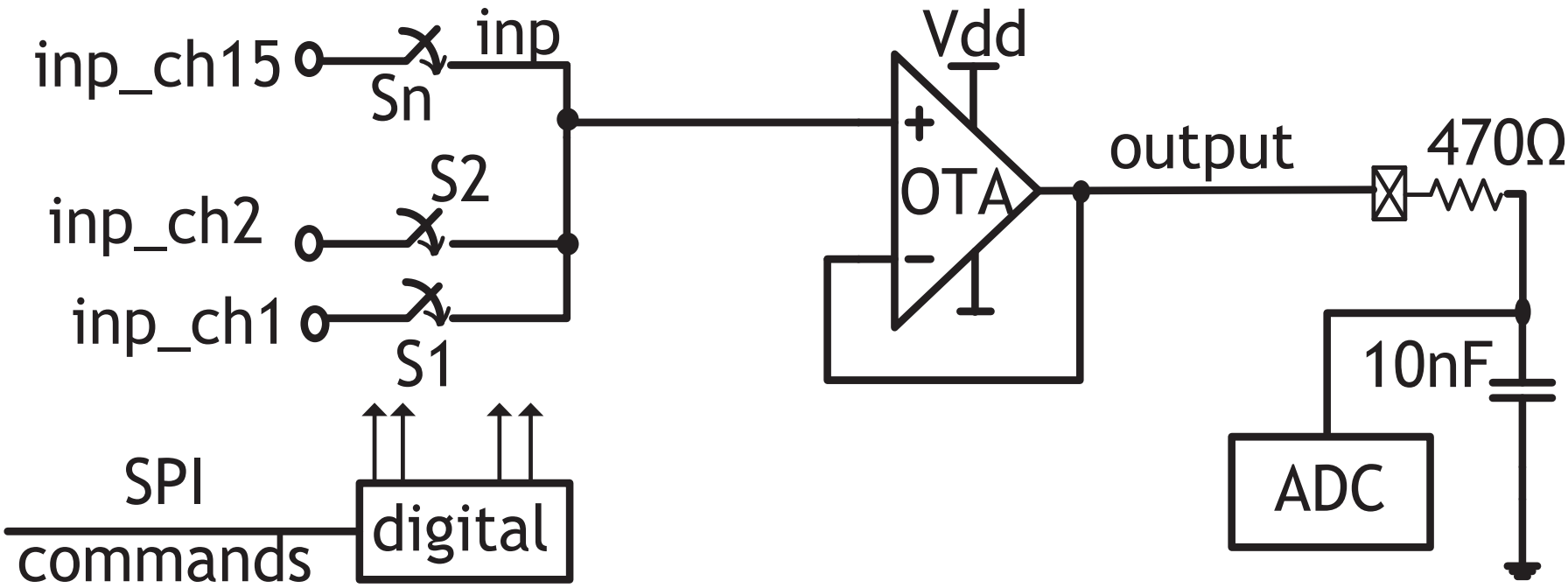
Diagnostics

- Diagnostic Scheme
- High Voltage Switches
- Parasitic NPNs – Mitigation
- HS, LS FET Diagnostics
- Output voltage clamping

Goals

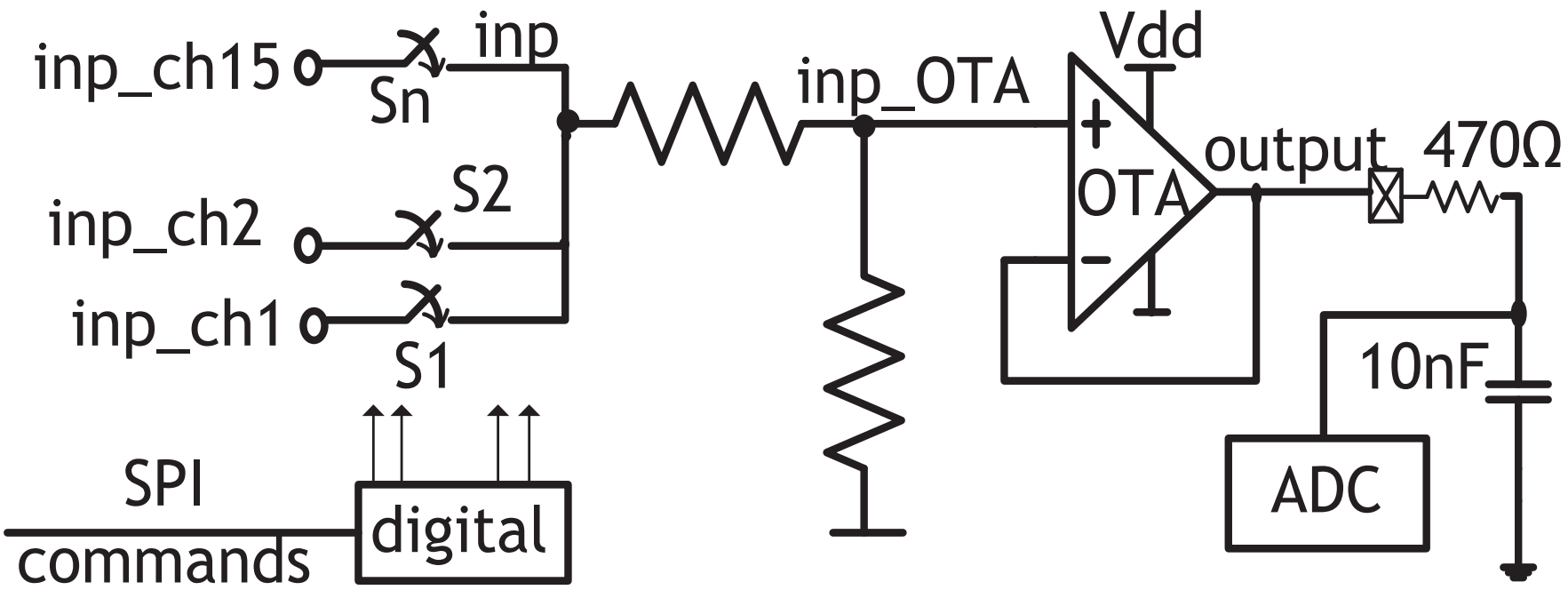
- Voltage, leakage, impedance measurements, checks on powerFETs are critical.
- Scaled version of high voltage inputs is measured through Analog output (AMX_OUT) or converted to a digital value through ADC.
- HS and LS_FETs are turned ON for 1-2ms duration. Load ~10mA to 30mA and checked for leakage flags.

Diagnostic Scheme (Airbag Squib Driver)



- inp_chx (x=1..15) can range from 100mV to 15V.
- Output should be limited to 5.4V to protect the ADC against over voltage conditions.

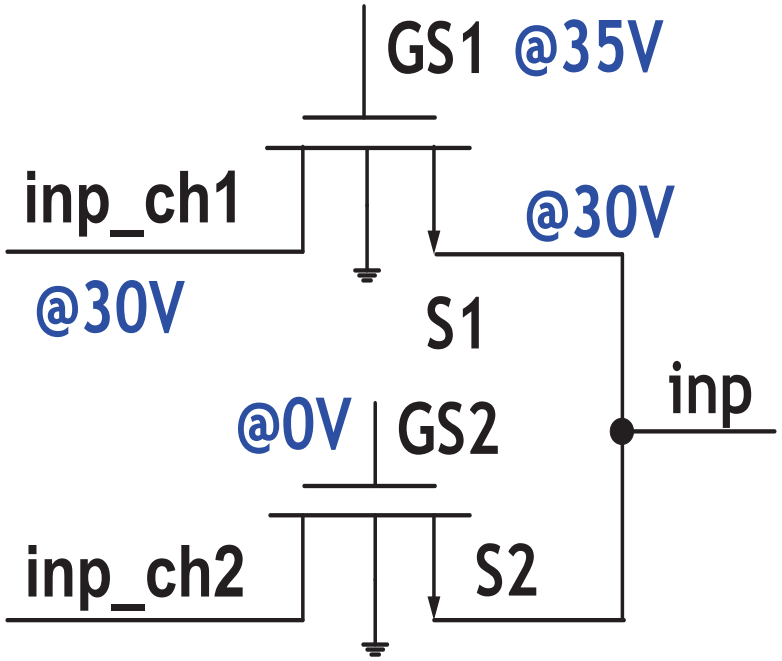
Scaled Down Voltage Measurements



- inp_chx (x=1..15) can range from 100mV to 15V.
- Output should be limited to 5.4V (+/-0.1V) to protect the ADC against over voltage conditions.

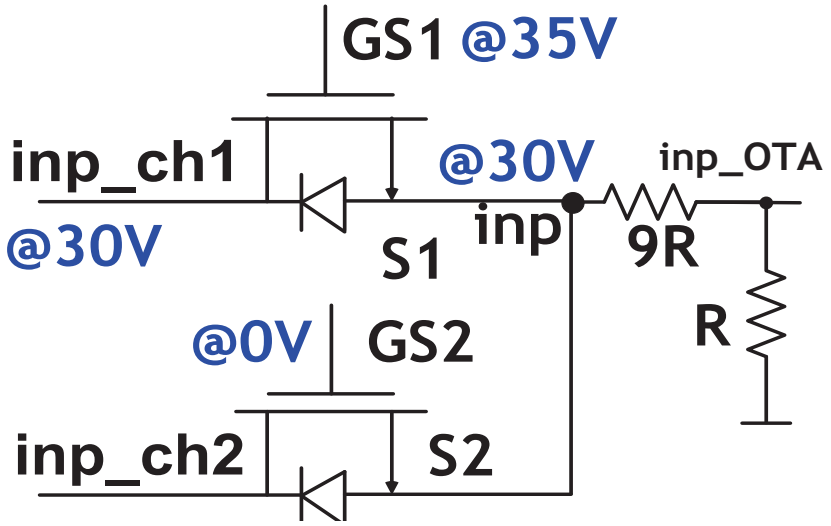
Switches

- One switch is active. Rest are in OFF state.
- All Switches should be protected (No Vgs, Vds, Vsb violation).

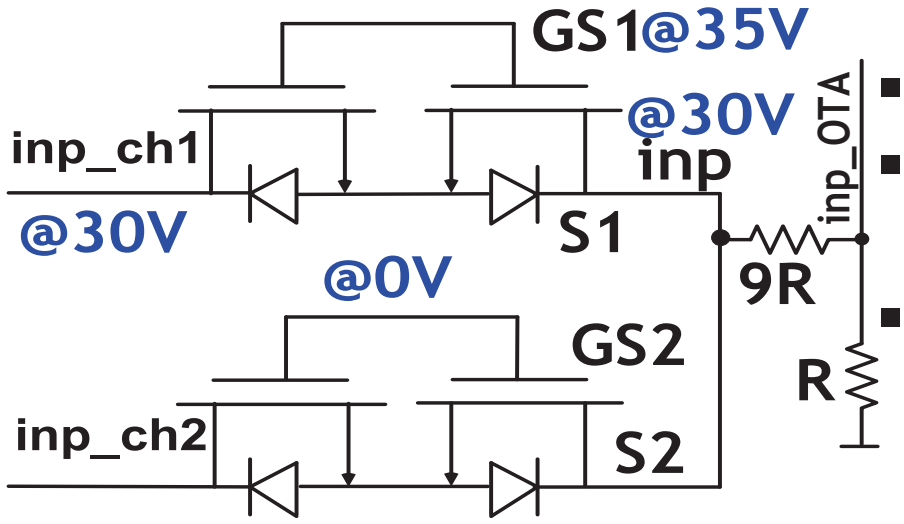


- Vgs,Vds of S1 is within its max. ratings. Vsb of S1 is violated (30V vs 13.2V or 5.5V allowed).
- Protect Vsb for S1 by tie-ing s-b together (layout impact due to isolation from substrate).
- Vgs and Vsb of S2 are violated. Vsb protected by tie-ing s-b together but Vgs fix needs another approach.

LDMOS Based Switches

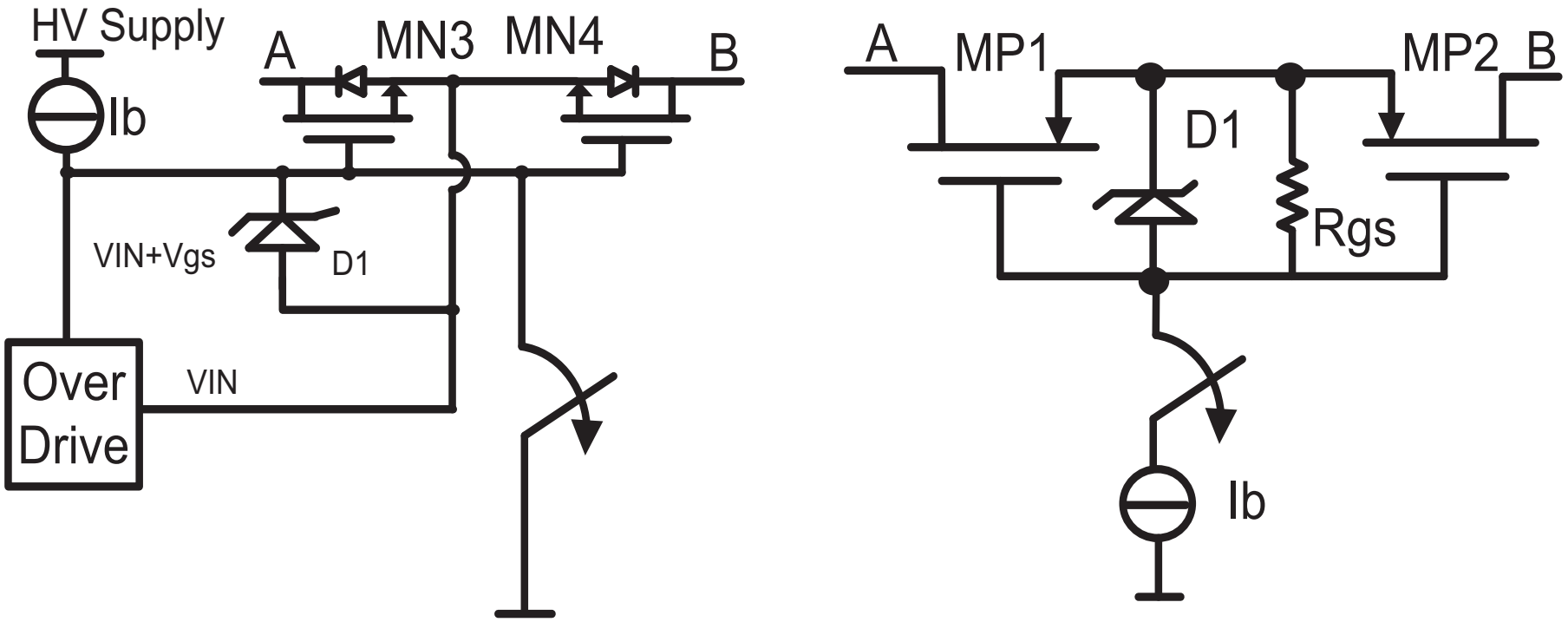


- Vgs,Vds of S1 is within its max. ratings. Vsb is not an issue for LDMOS.
- Vgs of S2 is impacted. Body diode of S2 is forward biased if inp > inp_ch2.
- Reliability Concern.



- Fix back to back LDMOS FETs.
- G-S junctions are not directly exposed.
- G-D junctions withstand high voltage levels. Area impact high.

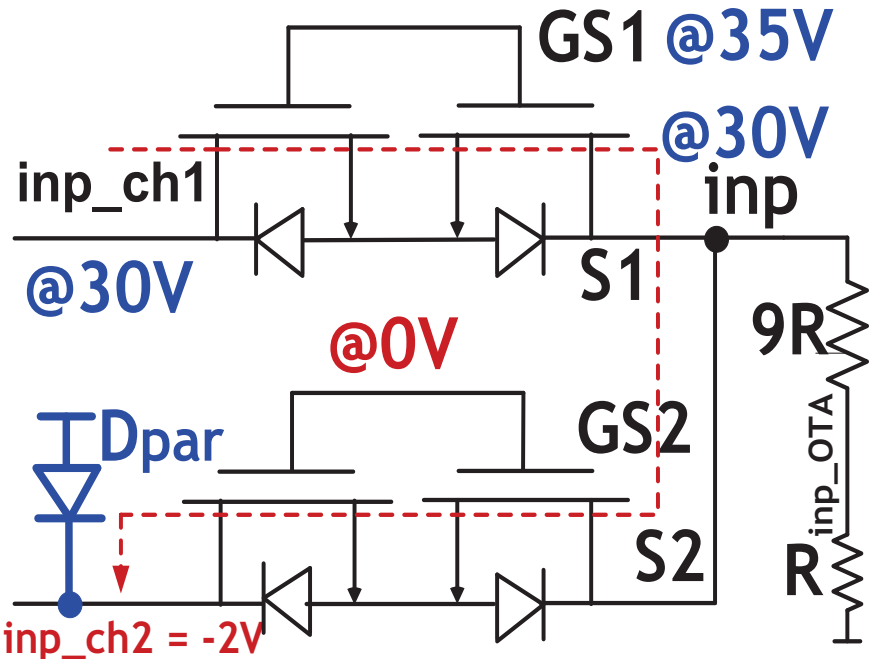
High Voltage Switch Architecture

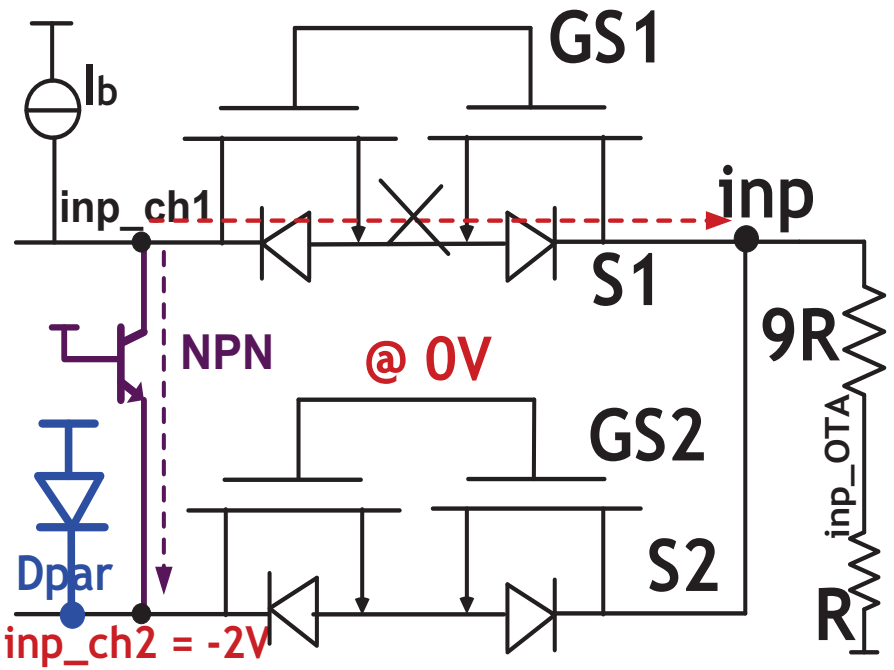


- NMOS and PMOS HV Switches with their adaptive gate bias and protection

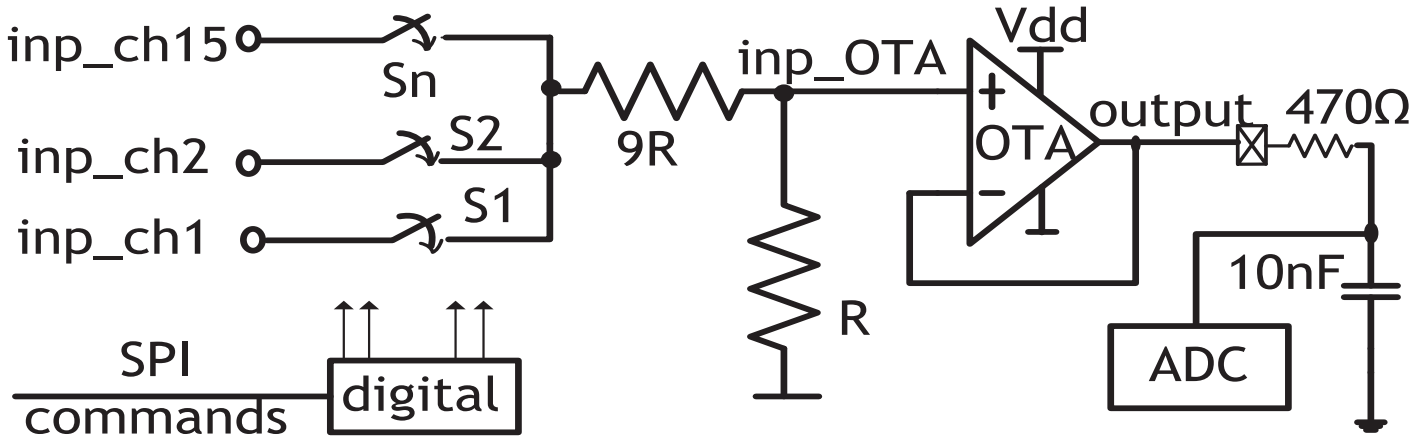
LDMOS Based Switches

- When inp_ch2 is below ground level (-2V), issues arise !
- Dpar (P-N junction from substrate to drain) is forward biased. [Clamped @-0.7V for current load. Too high current when forced to -2V].
- GS2 turns ON =>cross talk between inp_ch1 and inp_ch2. Potential NPN path will also exist and I_b never gets to “inp”.



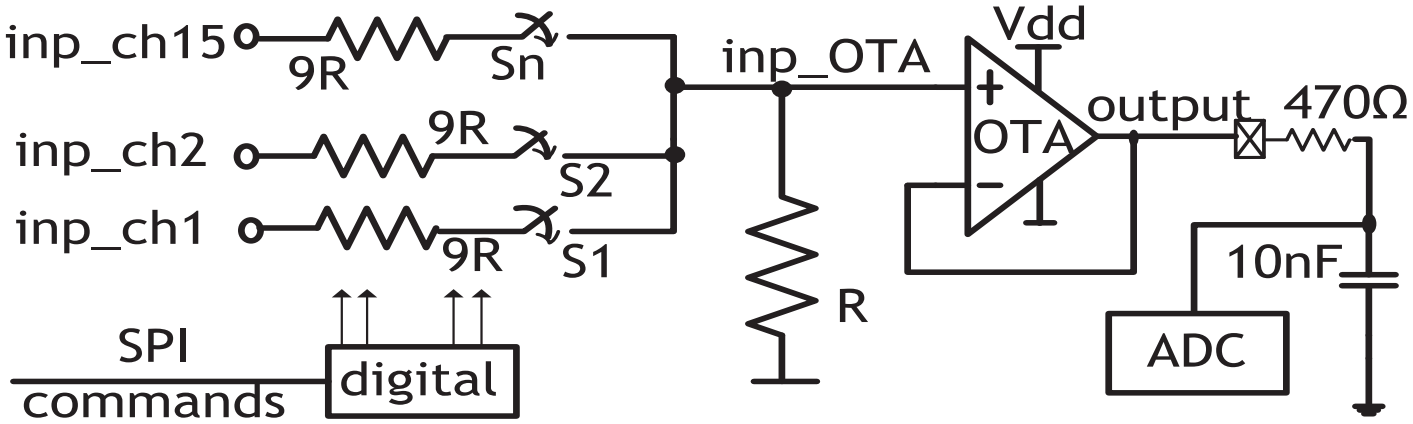


Design Improvements

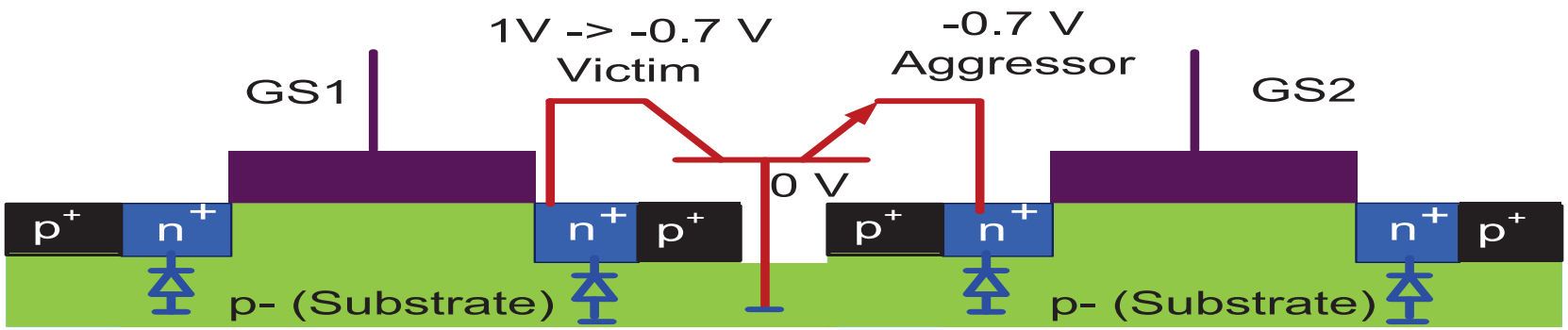


Intended design and robust design. If a signal is taken negative, then resistors limit the current.

No impact to functionality 9R >> Rds_on of Sn

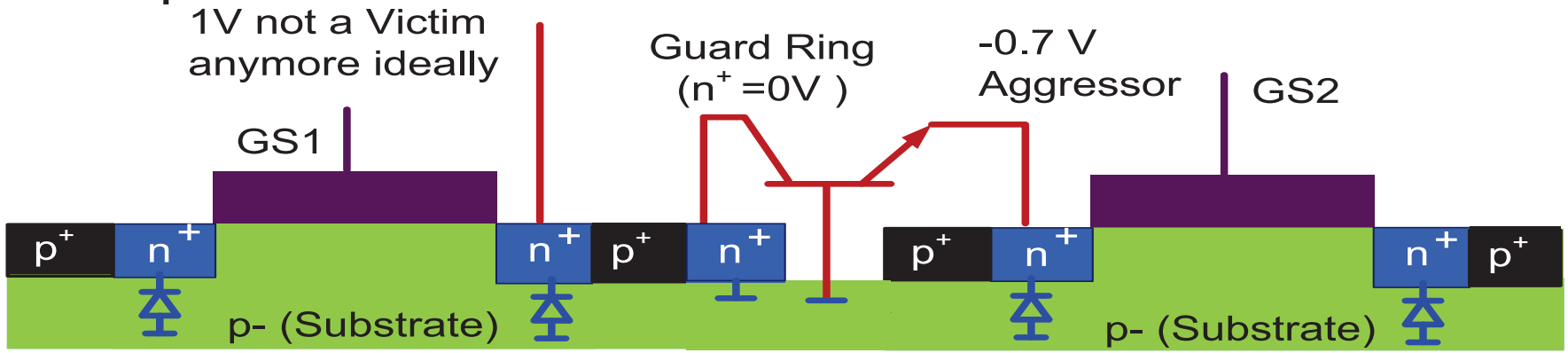


Layout Challenges and Improvements



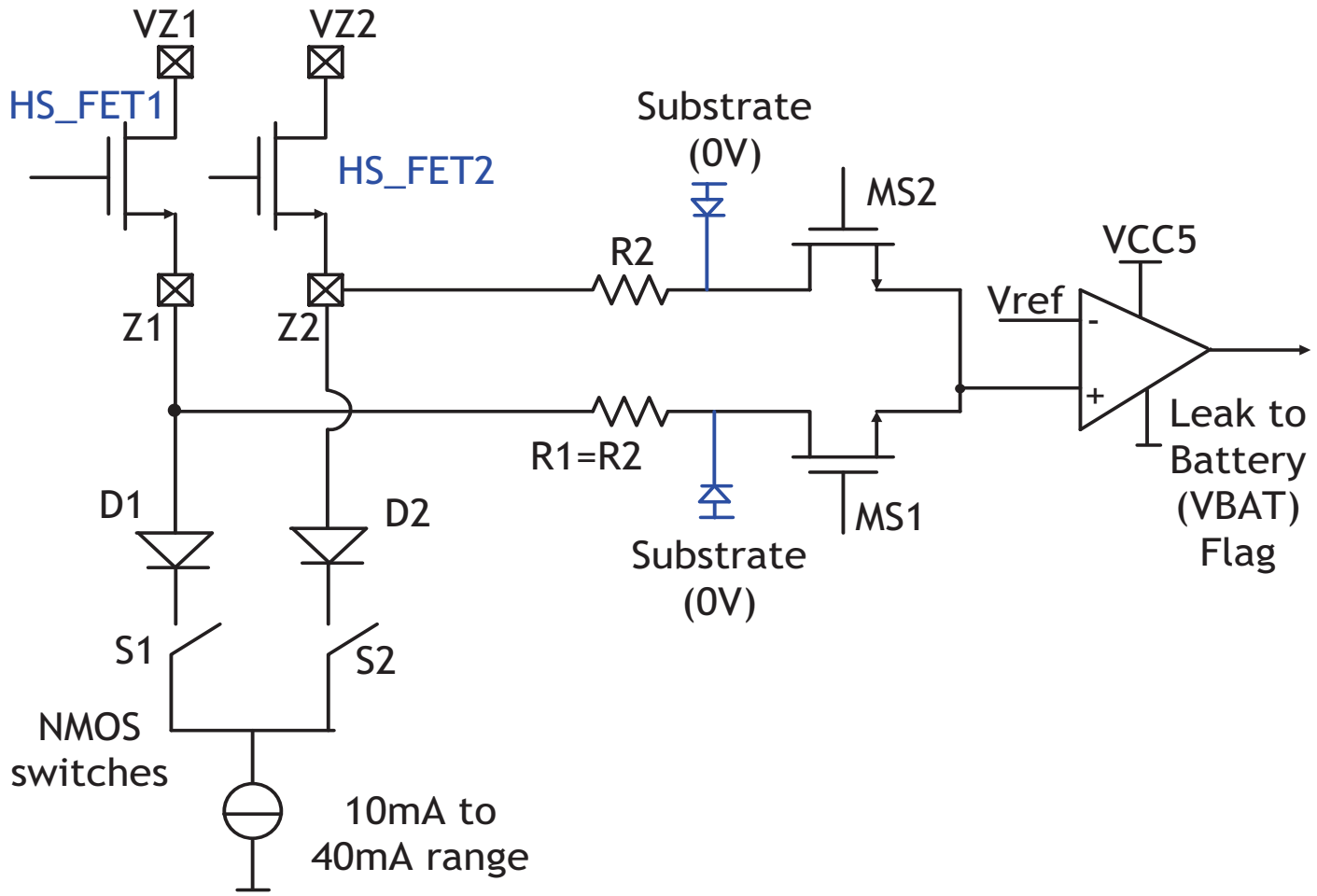
NPN action is dependent on the spacing between the two n+ regions. Lesser separation => higher NPN action.

- Larger separation is not area effective.
- Guard rings typically help to avoid potential NPN. Alternative is Deep trench.



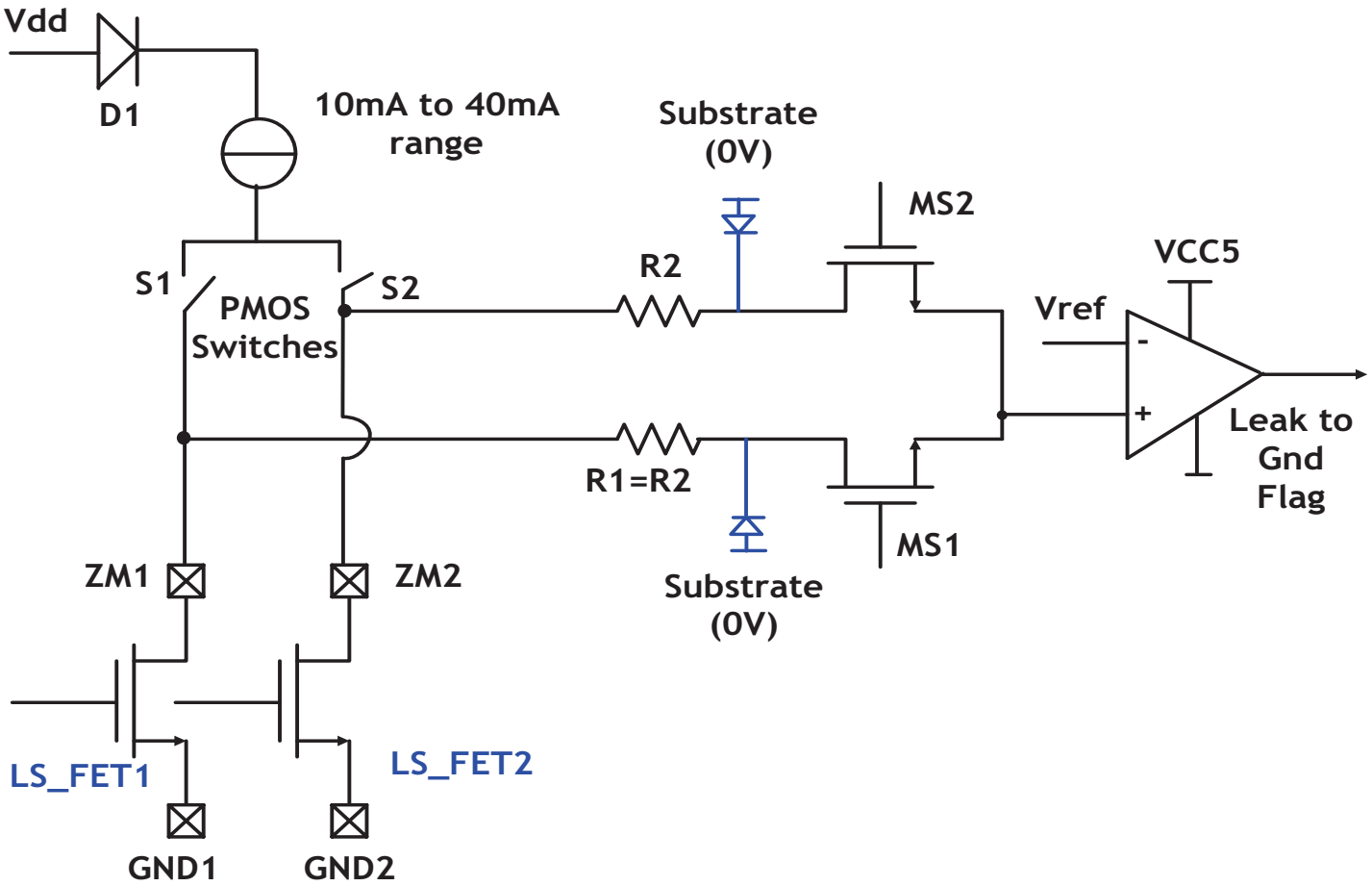
HS_FET Test

HS_FET is turned ON in diagnostic mode.
1-2ms duration, 10 to 40mA current range. Check for leak to battery.

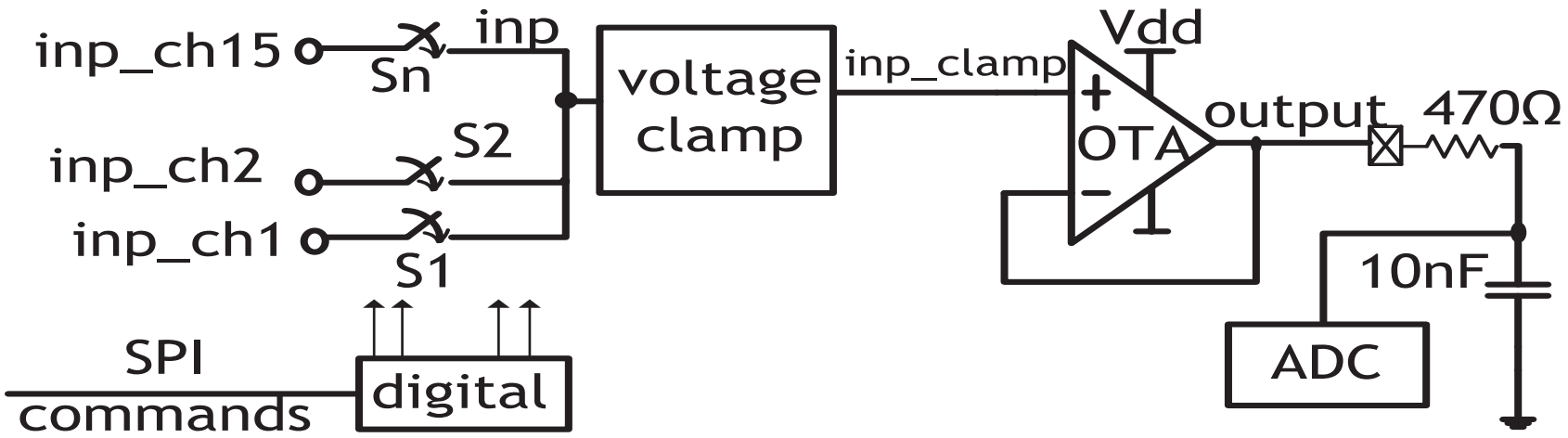


LS_FET Test

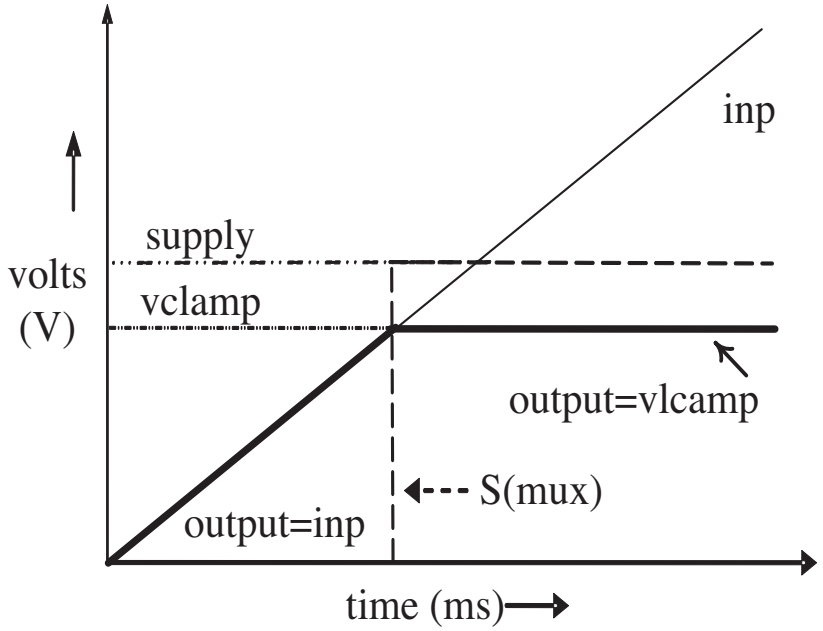
HS_FET is turned ON in diagnostic mode.
1-2ms duration, 10 to 40mA current range. Check for leak to Ground.



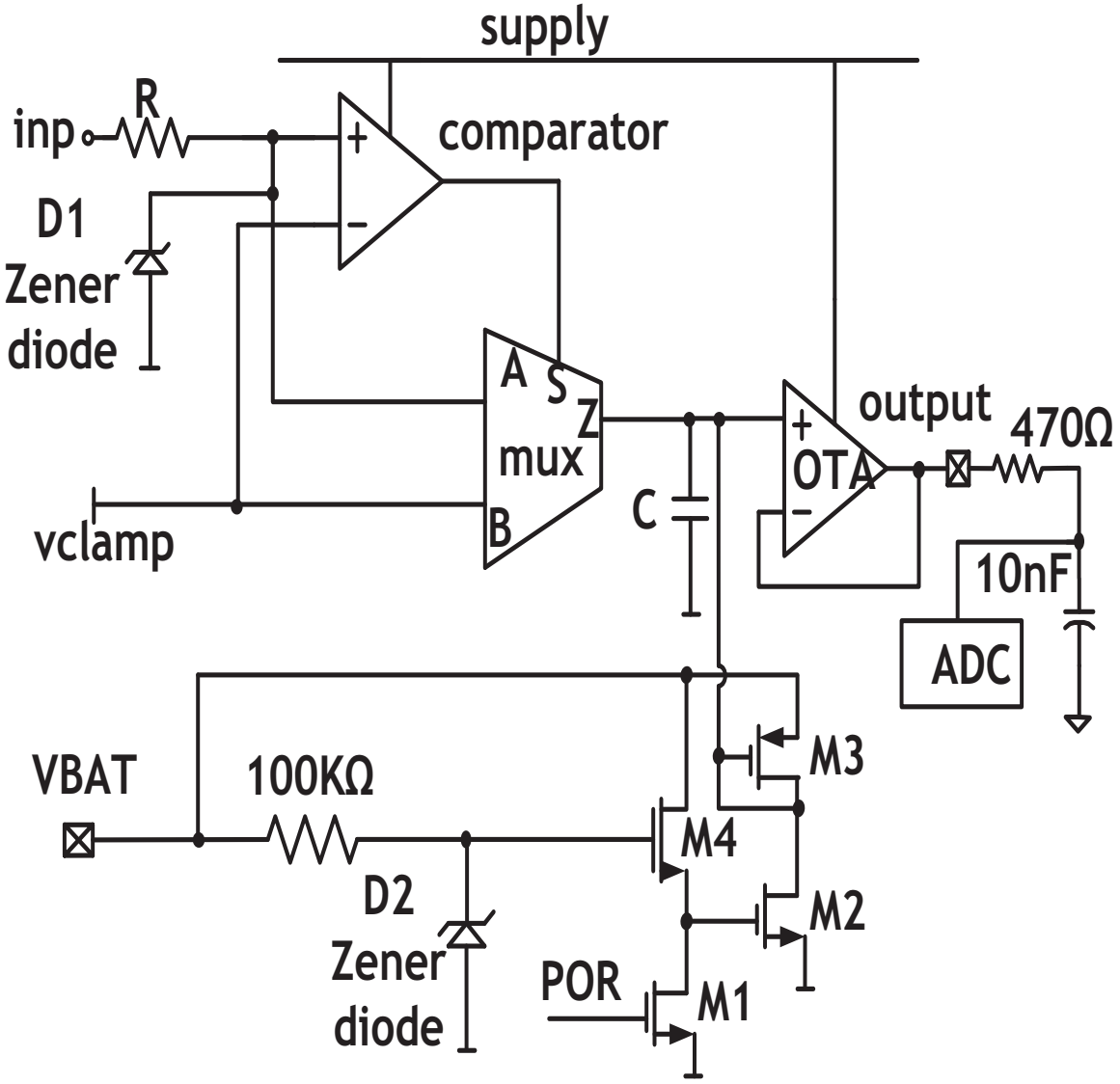
AMX_OUT Output voltage Clamping



- Output should be limited to 5.4V (+/-0.1V) to protect the ADC against over voltage conditions. So clamp the input of the comparator.

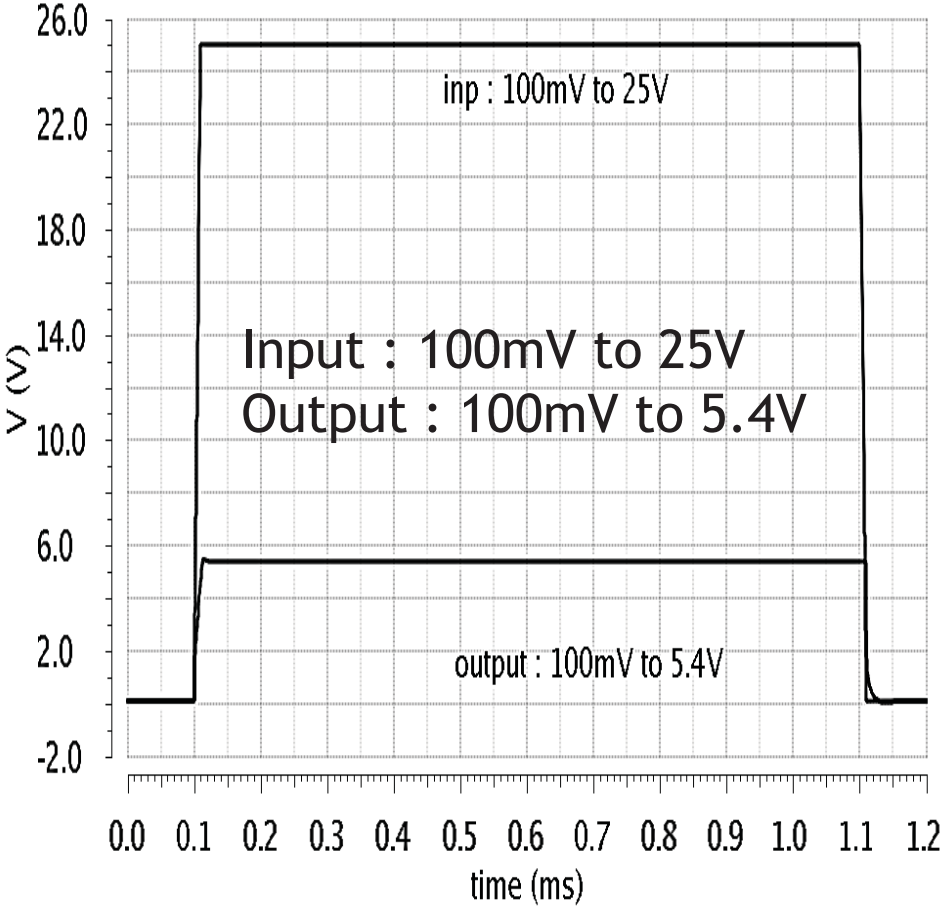


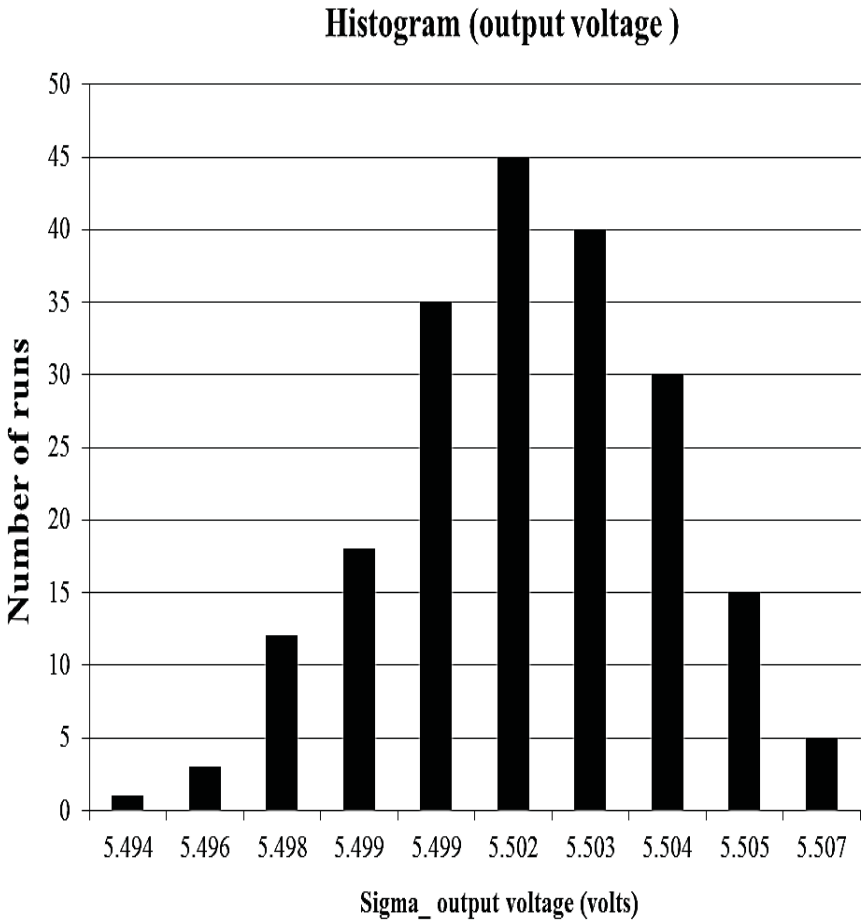
AMX_OUT Output voltage Clamping



- Zener diode based clamping is not precise. Too much Process, temp spread.
- MUX the input to the OTA based on the input. Precise approach.

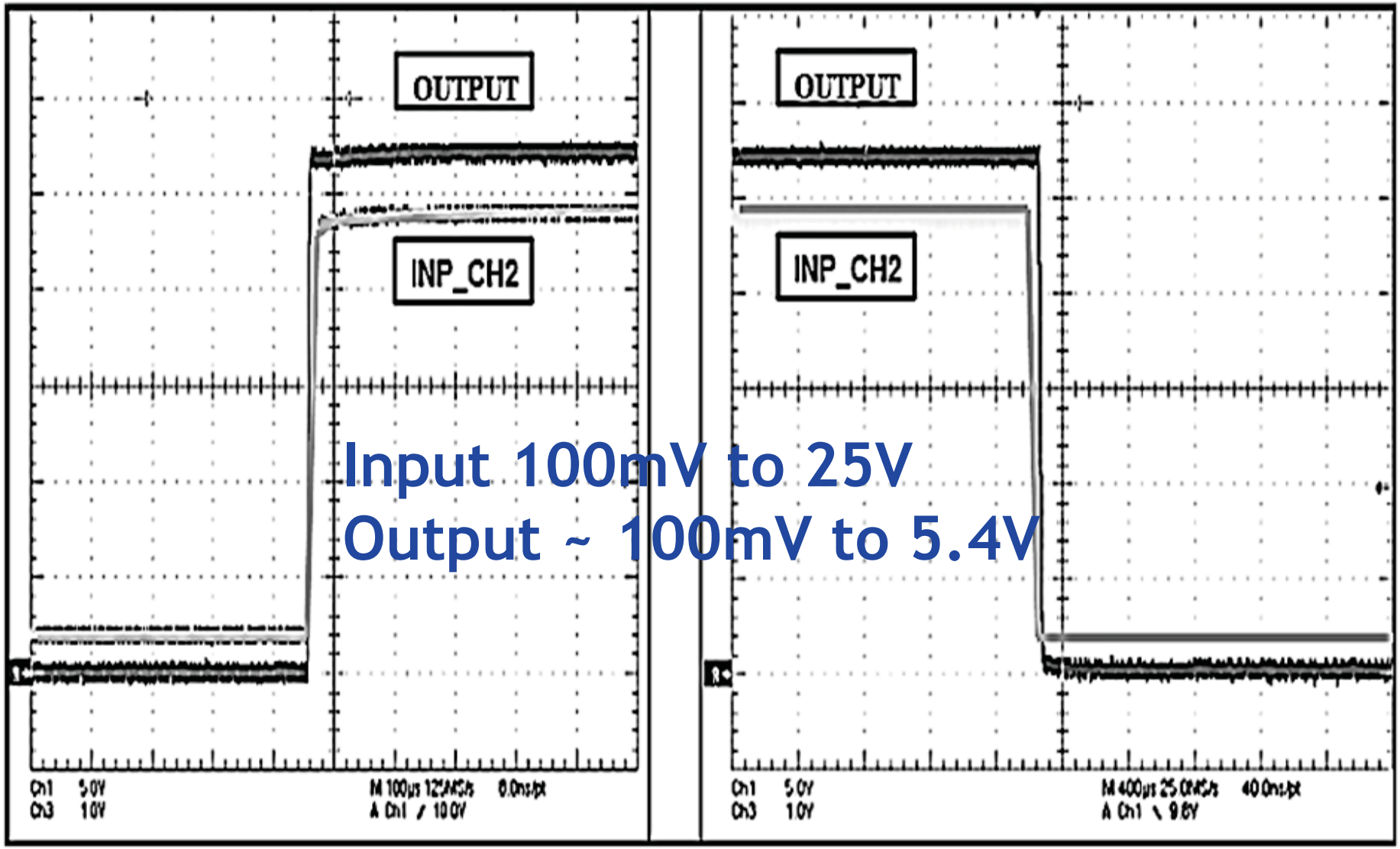
AMX_OUT Output voltage Clamping





- Output voltage limited during any power up scenario
- Precise output voltage limitation due to precise input voltage limitation

Measurement Results - AMX_OUT



Additional Requirements

- Automotive IC Design overhead
- Conducted Emission
- Portable Design
- References – Current Limited Voltage Source

Automotive IC Design Overhead

Concept/Topologies in Conventional (Consumer) and Automotive designs are not way different.

Faults, protection strategies, fast transients, unpowered state requirements lead to new topologies/additional circuits.

- 40V compliance is mandatory on several High Voltage pins.
- ESD -> Device level , system level (powered, unpowered state) requirements have to be met for Automotive designs.
- Passing DPI (Direct Power Injection), BCI (Bulk Current Injection), Mobile Transmitter tests add an additional overhead to Automotive designs .

ESD Requirements_SDU_Example

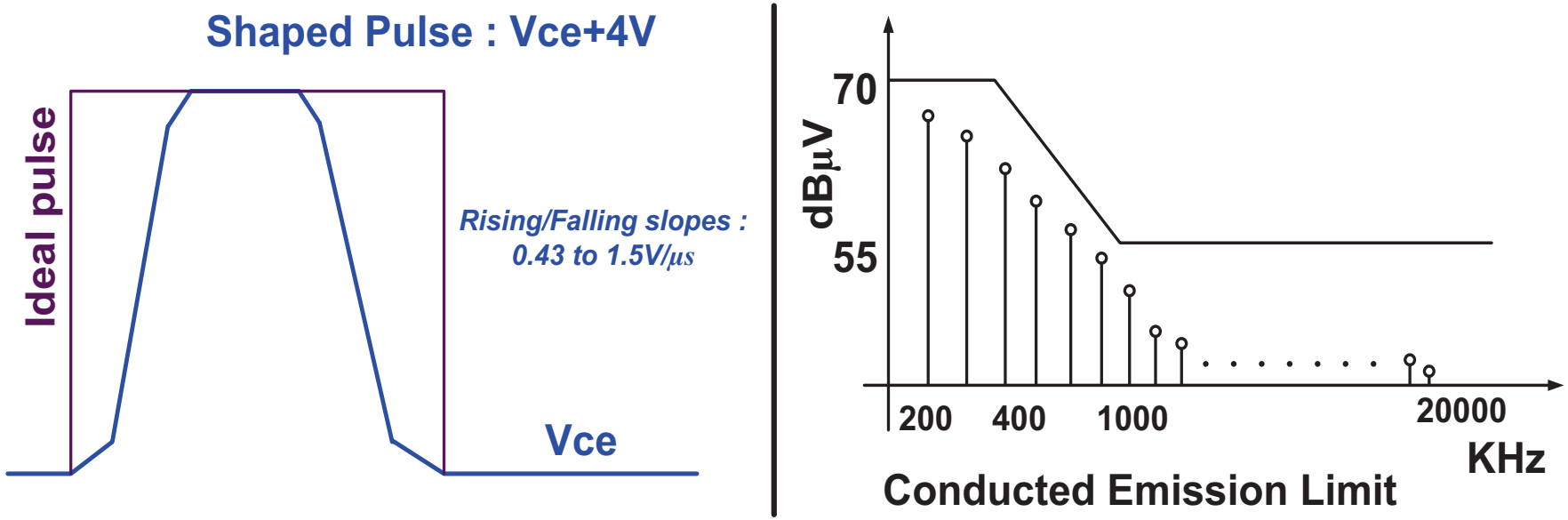
Traditional ICs: HBM : +/- 1KV, CDM : +/-500V -> JEDEC, IC Level.

Automotive ICs, AEC Q-100

- Max ESD Levels HBM : +/-2KV, CDM : +/-500V, +/-750V Corner Pins
- Max ESD Levels Unpowered, Powered ESD : For Zx, ZMx (squib lines), +/-8KV (with min.external protection (only capacitors))
- +/-25KV (with external protection (capacitors + Zener diodes).
- Pass Criteria : No destruction of ASIC. Part can't reset (powered state)

Conducted Emission Levels

- Shaped pulse reduces EMI (Electro Magnetic Interference).
- Sharp pulse edges have higher harmonics and can interfere with sensor data, audio band.
- Sharp pulses generate supply & ground noise due to Parasitic Inductance that can affect the whole IC performance. So it is important to shape the pulse => No Fast Switching !!



Portable Design

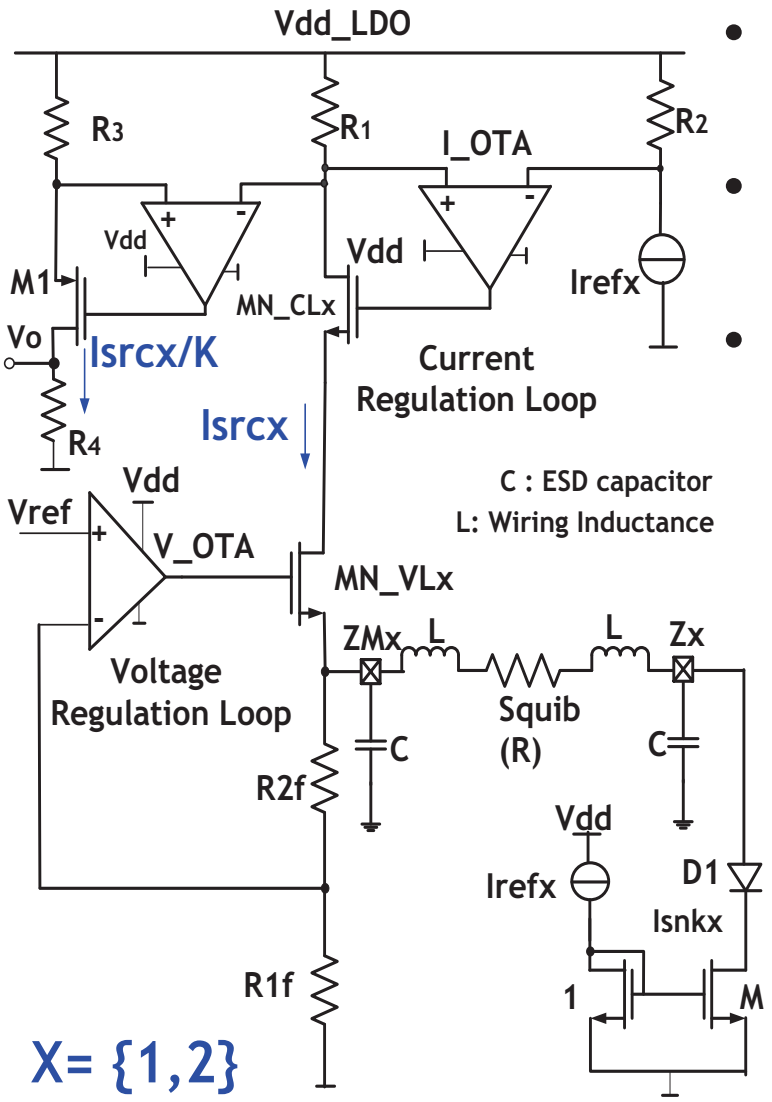
- Design change from one BiCMOS node to another BiCMOS technology node involves first to check for Vgs protection.
  - 40V device in two different technology nodes, Vds is still 40V but $V_{gs,max}$ can be 13.2V vs 5V.
  - Ensure that the Zener diodes reverse break down used for 5.5V gate oxide protection, is 5V.
- PowerFET W/L critical for R_{ds_on} and thermal SOA.
- Transfer function H(s) will be unchanged. => If Cox increased by a factor of 2 in new technology, W/L can be shrunk by 2, for same gm.
- Similar tricks for parameters like Rout.

$$H(s) = \frac{g_{m1} R_a g_{m2} R_{out} r_1 \left(1 + sR_{z1} C_c\right)}{r_o \left[1 + sR_{out} C_c + s^2 \left(\frac{LR_{out} C_c}{r_o}\right)\right]}$$

$$where\ g_{m1} = \sqrt{2I\mu . C_{ox} . \frac{W}{L}}$$

$$g_{m1\_new} = \sqrt{2I\mu . 2C_{ox} . \frac{W}{2L}} = g_{m1}$$

References - Current Limited Voltage Source



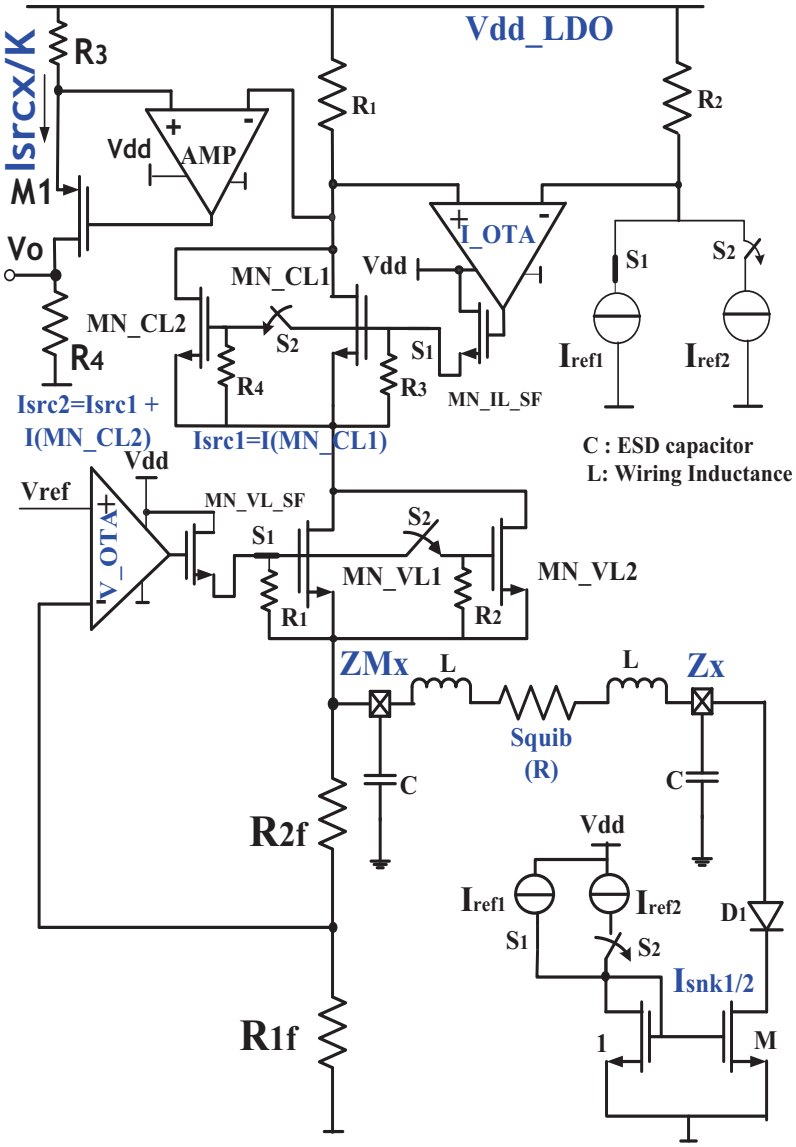
- Current Limited Voltage Source (CLVS) regulates voltage on ZMx pin.
- When ZMx is shorted to ground, I_OTA regulates/limits the current.
- Vo is the voltage equivalent of scaled version of Isrcx.

$$V_{ZMx} = \left(1 + \frac{R_{2f}}{R_{1f}}\right) V_{ref}$$

$$I_{srcx} = \left(\frac{R_2}{R_1}\right) I_{refx}$$

$$I_{scl} = \left(\frac{I_{srcx}}{k}\right) = \left(\frac{R_1}{R_3}\right) I_{srcx}$$

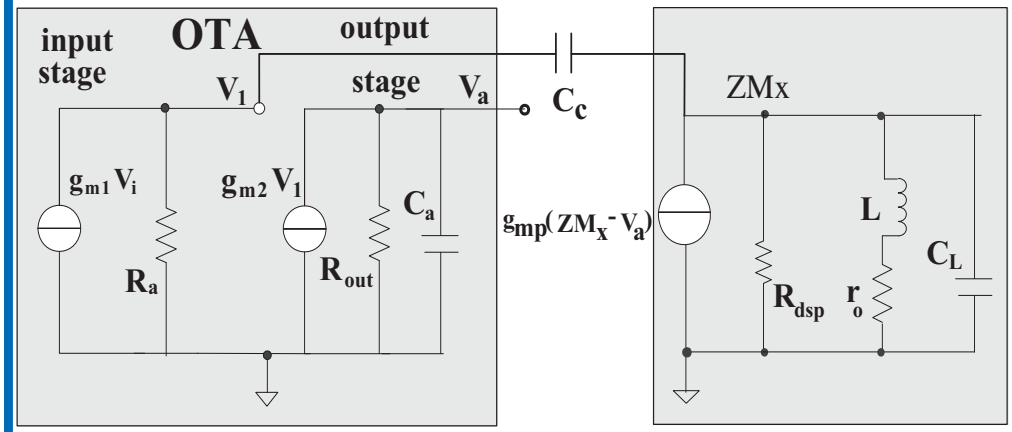
Implementation - Current Limited Voltage Source



- Diagnostics is always a two point measurement.
- Isrc1/2 > Isnk1/2 so that V_OTA regulates the voltage on ZMx.
- Vo, VZMx are measured through AMX_OUT. R4 is a known resistor.

- (Vo/R4) calculation => Isrcx/K is known.
- R1, R3 known by design=> K,Isrcx is known.
- => VZMx/Isrcx calculation provides leakage impedance on ZMx pin.

Small Signal Analysis : V_OTA Loop



$$H(s) \sim \frac{g_{m1}R_a g_{m2}R_{out}\left(1+s\frac{L}{r_o}\right)}{\left[1+sg_{m2}R_{out}C_c R_a + s^2\left(\frac{C_L C_a R_{out}}{g_{mp}}\right)\right]}$$

$$A_{dc\_2} = g_{m1}R_a g_{m2}R_{out} \quad ; f_{p1\_2} \sim \frac{1}{2\pi g_{m2}R_{out}C_c R_1};$$

$$f_{p2\_2} \sim \frac{g_{mp}g_{m2}R_1 C_c}{2\pi C_L C_a} \quad ; \quad f\tau\_2 = \frac{g_{m1}}{2\pi C_c}$$

For I_{snk2}, transconductance is

$$g_{mp\_snk2} = \sqrt{2I_{d\_snk2}\,\mu C_{ox}\frac{W}{L}}$$

$$\Rightarrow g_{mp\_snk1} = \sqrt{2I_{d\_snk1}\,\mu C_{ox}\frac{W}{L}} = \sqrt{2\frac{I_{d\_snk2}}{k}\,\mu C_{ox}\frac{W}{kL}} = \frac{1}{k}g_{mp\_snk2}$$

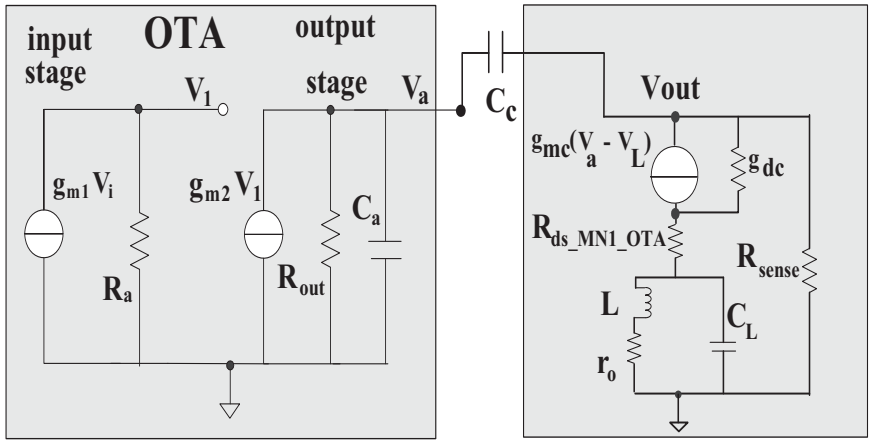
Poles, Zero, UGB for Isnk1 and Isnk2 are the same.

$$A_{dc\_1} = g_{m1}R_a g_{m2}R_{out} = A_{dc\_2}$$

$$f_{p1\_1} \sim \frac{1}{2\pi g_{m2}C_c R_{out}R_1} = f_{p1\_2} \quad ; \quad f_{p2\_1} \sim \frac{\left(\frac{1}{k}g_{mp\_snk2}\right)C_c g_{m2}R_1}{2\pi C_L\left(\frac{C_a}{k}\right)} = f_{p2\_2} \quad ; \quad f_{\tau\_1} = \frac{g_{m1}}{2\pi C_c} = f_{\tau\_2}$$

Small Signal Analysis : C_OTA Loop

$$H(s) \sim \frac{V_{out}}{V_i} = -\frac{g_{m1}R_a g_{m2}R_{out}G_{mc}R_{sense}\left(1-\frac{sC_c}{G_{mc}}\right)}{\left[1+sG_{mc}R_{sense}C_cR_{out}+s^2G_{mc}LC_cR_{out}\right]}$$



$$DC\ Gain\ A_{dc} = g_{m1}R_a g_{m2}R_{out}G_{mc}R_{sense} \quad where \quad G_{mc} = \frac{g_{mc}}{1+g_{mc}R_{ds\_on\_V\_MN1}} \sim \frac{1}{R_{ds\_on\_V\_MN1}}$$

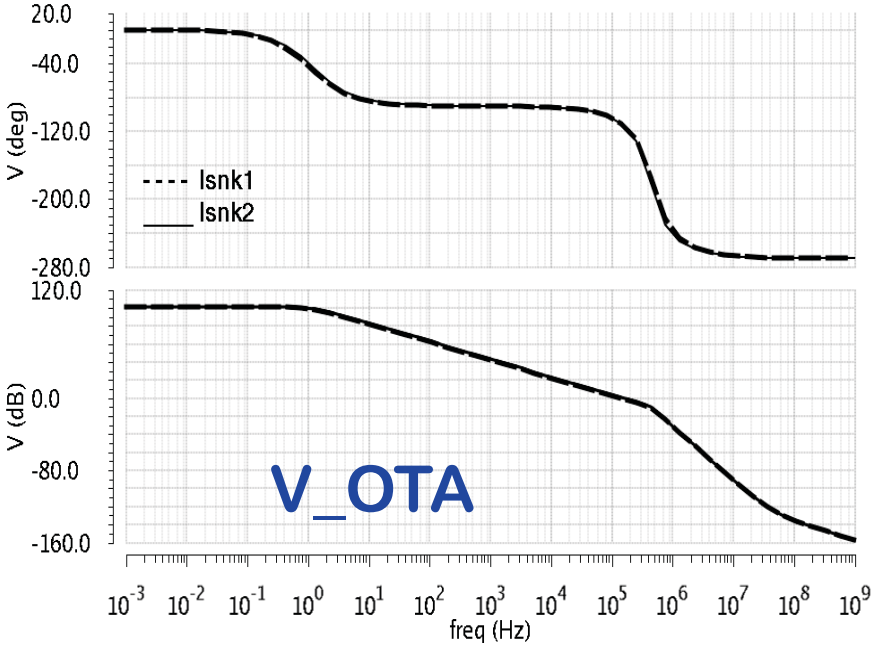
$$p_1 = \frac{1}{G_{mc}R_{sense}C_cR_{out}}$$

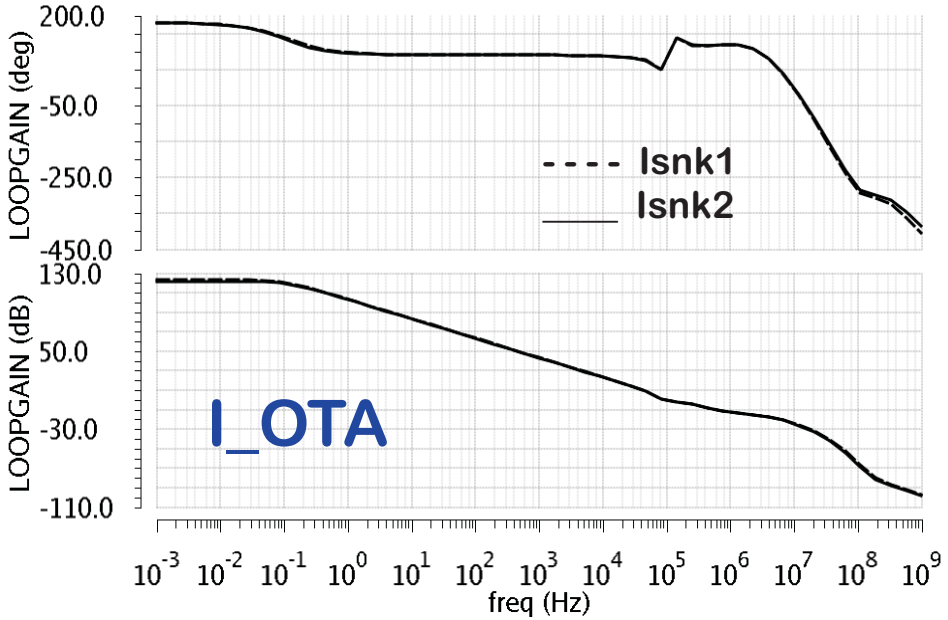
$$p_2 = \frac{G_{mc}R_{sense}C_cR_{out}}{G_{mc}LC_cR_{out}} = \frac{R_{sense}}{L}$$

$$z_1 = \frac{G_{mc}}{C_c}$$

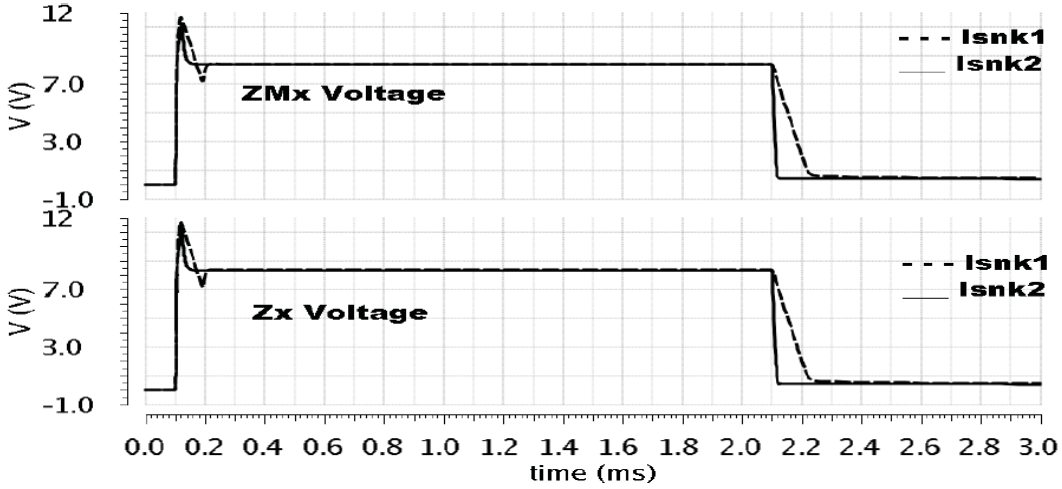
Current loop stability independent of Isrcx

Scalable Design for Predictable Behavior

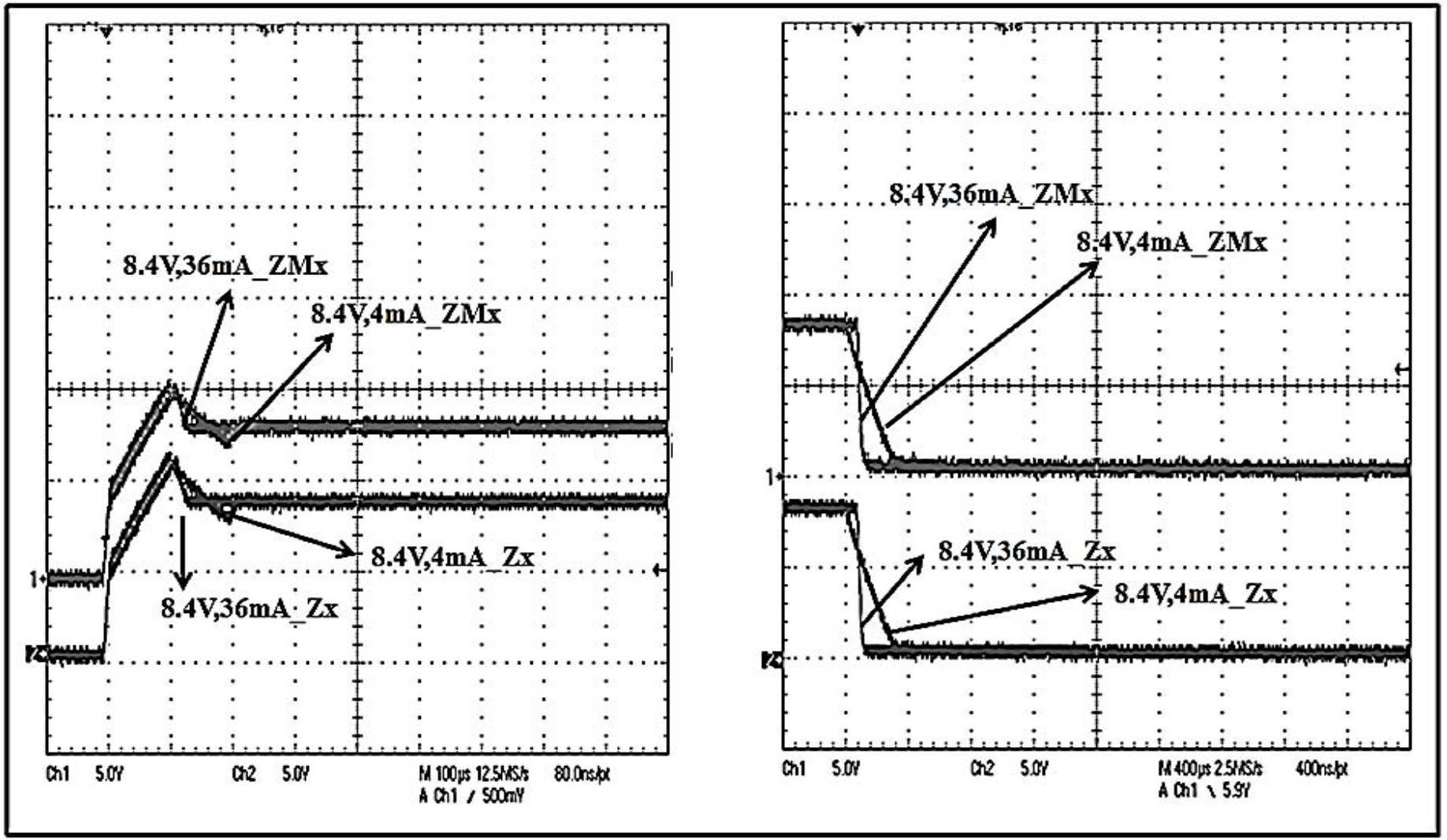




- Identical Poles and Zeroes for V_OTA and I_OTA.
- Transient response is similar as well.



Measurement Results -CLVS



Conclusion

- Automotive IC designs are not different from conventional (consumer/already well known) IC designs.
- Most of the Automotive ICs have to be 40V compliant. Some pins would have to tolerate negative voltages (-2V to -18V).
- Designs are portable from one technology to another. Circuits that are scalable have better predictable behavior.
- Additional circuits or modifications to conventional designs might be required to address fault conditions, powered and unpowered state, ESD, DPI requirements.(ESD and Immunity tests add additional burden to designers.)
- Level shifters have to be designed fail silent.
- Diagnostics, Cross link tests are critical and should be designed to avoid false warnings.
- Quality is a key factor in Automotive. 0 dppm is the expectation.

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Thankyou for your attention