AI Multi-Tenancy on Edge: Concurrent Deep Learning Model Executions and Dynamic Model Placements on Edge Devices

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Abstract—Many real-world applications are widely adopting the edge computing paradigm due to its low latency and better privacy protection. With notable success in AI and deep learning (DL), edge devices and AI accelerators play a crucial role in deploying DL inference services at the edge of the Internet. While prior works quantified various edge devices' efficiency, most studies focused on the performance of edge devices with single DL tasks. Therefore, there is an urgent need to investigate AI multi-tenancy on edge devices, required by many advanced DL applications for edge computing.

This work investigates two techniques – concurrent model executions and dynamic model placements – for AI multi-tenancy on edge devices. With image classification as an example scenario, we empirically evaluate AI multi-tenancy on various edge devices, AI accelerators, and DL frameworks to identify its benefits and limitations. Our results show that multi-tenancy significantly improves DL inference throughput by up to $3.3\times-3.8\times$ on Jetson TX2. These AI multi-tenancy techniques also open up new opportunities for flexible deployment of multiple DL services on edge devices and AI accelerators.

Index Terms—Edge Computing; AI Multi-Tenancy; Deep Learning at the Edge; Concurrent Model Executions; Dynamic Model Placements; Performance Evaluation.

I. INTRODUCTION

There have been massive strides in Artificial Intelligence (AI) and Deep Learning (DL) technologies in recent years. Newer DL algorithms coupled with highly cost-effective and scalable mechanisms to gather, store, and process large amounts of data have led to what some researchers believe to be the golden age of AI/DL [1]. It is widely expected that in the near future, AI will drive applications in many massively distributed domains, such as autonomous vehicles, disaster response, precision agriculture, and drone-based surveillance [2], [3]. These domains are often distinguished by two fundamental characteristics, namely, stringent response time requirements (i.e., real-time or near real-time), data sources that are distributed at the edge of the Internet and highly resource-constrained operational environments [4].

The predominant paradigm for building AI systems is to centralize all AI tasks at the cloud [5]–[9]. In other words, in this *cloud-based AI paradigm*, pre-trained (often large-scale) DL models are deployed exclusively at the cloud [10]–[15]. While cloud-based AI offers distinct advantages, particularly to domains, e.g., social networks, e-commerce, and finance, where the data is naturally available on the cloud, this paradigm is not well suited for the aforementioned domains. This is because transferring large amounts of data from the network edge to the cloud over low-bandwidth connections is

prohibitively expensive, often resulting in AI service disruptions caused by network disconnections, which are not well tolerated by these applications.

Towards addressing the above limitations, researchers have recently been exploring the AI at the edge paradigm [2], [16]–[19], where DL applications are hosted at the edge of the Internet (e.g., closer to the data sources). Advent and proliferation of miniaturized yet powerful computing boards, e.g., Raspberry Pi [20], Nvidia Jetson Nano [21], and Google's EdgeTPU [22], have served as key enablers for moving DL tasks to the edge of the Internet. Several studies have been conducted to quantify the efficiency of various edge devices for DL inference tasks [23]–[28]. Most existing studies have focused on characterizing the performance (e.g., latency and throughput) of edge devices and AI accelerators with single DL tasks. However, many advanced applications often require AI multi-tenancy where multiple DL tasks are co-running on edge devices. For instance, drone-based surveillance requires simultaneous executions of inference tasks on video and audio streams [29]. Unfortunately, very few researchers have tried to quantify and optimize the AI multi-tenancy on edge devices to the best of our knowledge.

Leveraging AI multi-tenancy on edge devices has the potential to provide distinct benefits in offering DL services. AI multi-tenancy can be achieved via leveraging concurrent model executions (CMEs) and dynamic model placements (DMPs). CME allows the deployment of multiple DL models on either GPU or EdgeTPU resources and runs them in parallel. Thus, CME can potentially improve the overall DL inference throughput and enable the execution of different DL applications/models simultaneously. DMP enables AI multitenancy by deploying and executing DL models on different resources on edge devices at the same time. e.g., DL models on both GPU and EdgeTPU. DMP is particularly useful when AI accelerators (e.g., EdgeTPU) enhance edge devices, and it can significantly increase the resource utilization and the DL inference throughput by utilizing multiple resources on the devices and the accelerators.

While there are expected advantages of AI multi-tenancy on edge devices, it is also important to identify the limitations of AI multi-tenancy to maximize the benefits of AI at the edge. Specifically, in this work, we seek answers to the following research questions. What are the performance benefits of enabling AI multi-tenancy in the device level? What are the limitations of the edge devices and accelerators to support AI multi-tenancy, such as the limit of model concurrency, resource

contention, and resource bottleneck?

To answer the above research questions, this study performs comprehensive evaluations of CME and DMP for AI multitenancy and discovers the opportunities and limitations of such approaches. Both CME and DMP are thoroughly evaluated with widely used edge devices and EdgeTPU accelerators. We use *image classification* as an example application scenario of AI at the edge and assess nine pre-trained DL models¹ with four DL frameworks.

We first characterize the behavior and performance (e.g., inference throughput) of both edge devices and EdgeTPU accelerators and identify critical resource factors affecting the DL inference throughput on the edge devices and accelerators. Then we apply two AI multi-tenancy approaches to DL inference tasks on the devices and accelerators, and then we discover the empirical upper bound of DL inference throughput as well as the impact from resource contention. Our evaluation results show that modern edge devices and EdgeTPUs can achieve $1.9\times-3.3\times$ higher inference throughput with CME. Moreover, the DMP approach can increase throughput by up to $3.8\times$. These two approaches for AI multi-tenancy open up new opportunities for maximizing the resource utilization of devices and flexible deployment of multiple DL applications on edge devices.

The research contributions of this work are as follows:

- 1. We thoroughly characterize and quantify the performances (DL inference throughput) and behaviors of various edge devices and AI accelerators when enabling AI multitenancy. Such characterizations are performed by employing a set of DL frameworks and DL models widely used for image classifications.
- 2. We discover the empirical upper bound of the performance and the model concurrency on edge devices and EdgeTPUs when AI multi-tenancy is enabled by CME.
- 3. We identify the performance benefits and limitations when adopting DMP to utilize heterogeneous resources on edge resources and EdgeTPUs. This work is the first study to characterize and evaluate DMP for AI multi-tenancy to the best of our knowledge.

We structure the rest of the paper as follows. Section II describes edge devices, EdgeTPUs, DL models, and DL frameworks used in this work. Section III characterizes the performance and the behavior of the devices with single-tenancy cases. Section IV conducts evaluations of two AI-multi-tenancy techniques on edge devices and AI accelerators and describes their benefits and limitations. Section V summarizes and discusses our findings from this work. Section VI describes related work, and Section VII concludes this paper.

II. EDGE DEVICES, EDGETPU ACCELERATORS, DEEP LEARNING MODELS, AND DEEP LEARNING FRAMEWORKS

This section describes edge devices and AI accelerators, DL models, and DL frameworks used in this study.

A. Edge Devices and EdgeTPU Accelerators

In this work, we employed the following four widely-used edge devices and two EdgeTPU AI accelerators.

Jetson TX2 (**J.TX2**) [30] is a high-performance edge device with six CPU cores (a dual-core Denver 2 CPU and a quadcore ARM Cortex-A57 at 2 GHz) and a 256-core Nvidia Pascal GPU for DL processing. J.TX2 has a 8 GB LPDDR4 RAM, which is shared by CPUs and GPUs. Among five different power modes in J.TX2 [31], we use mode-0 (MaxN) to enable all six CPU cores and provide the highest frequency of both CPUs (2.0 GHz) and GPUs (1.3 GHz).

Jetson Nano (J.Nano) [21] is a small yet powerful single board computer specialized in DL processing. It has a quadcore ARM Cortex-A57 (1.5 GHz), a 128-core Nvidia Maxwell GPU, and 4 GB LPDDR4 RAM (shared by both CPUs and GPUs). For J.Nano, we use a power mode of mode-0, which is default mode for maximizing the device performance.

Odroid-N2 (**ODN2**) [32] is a computing board with 4GB LPDDR4 RAM and six CPU cores (a quad-core Cortex-A73 at 1.8 GHz and dual-core Cortex-A53 at 1.9 GHz). While ODN2 has a GPU (Mali-G52 GPU), we cannot use this GPU for DL inference tasks due to a software compatibility issue.

Raspberry Pi 4 (RPi4) [20] is a small, low-cost, representative computing board for edge/IoT devices. RPi4 is based on Broadcom BCM2711 SoC and has a quad-core ARM Cortex-A72 (1.5 GHz) and 4 GB LPDDR4 RAM. RPi4 neither has a GPU nor specialized HW accelerators for DL processing.

Coral Dev Board (DevBoard) [33] is a single-board computer equipped with a quad-core Cortex-A53 CPU (1.5GHz) and 1GB LPDDR4 RAM², as well as onboard TPU (Tensor Processor Unit) co-processor, performing 4 trillion operations per second (TOPS) at 2W of power consumption.

Coral USB Accelerator (USB-Accelerator) [34] is a USB-type TPU accelerator for machine learning (ML) and DL. The performance of its onboard EdgeTPU accelerator is equivalent (4 TOPS at 2W) to that in DevBoard. USB-Accelerator can be connected with diverse host edge devices (e.g., RPi4 and J.Nano) and enhance DL processing. Since it only has an EdgeTPU co-processor, USB-Accelerator relies on the host device's memory system to store and load the DL models and their parameters.

B. DL Models, Frameworks, and Application

DL Models. This study used a set of DL models to evaluate AI multi-tenancy on edge devices and AI accelerators. The accuracy and the size of DL models keep increasing along with the rising complexity of model dimensions and the adding number of neural network layers. However, such large-size models do not fit into resource-constrained, low-capacity edge devices. Therefore, among many available DL models, we selected nine *pre-trained* DL models because these models

¹These DL models are pre-trained models of CNN (Convolutional Neural Network) models for image classifications.

²The newer version of DevBoard can have 2G or 4G of LPDDR4 RAM, but we use DevBoard with 1GB RAM.

| | Year | Input | Num. | Billion | # Params | Approx. | DL Framework (FW) Support | | | |
|--------------------|------|---------|--------|---------|-----------|----------------|---------------------------|-------|----------|--------|
| | | Size | Layers | FLOPS | (Million) | File Size (MB) | PyTorch | MXNet | TF | TFLite |
| AlexNet [35] | 2012 | 224×224 | 8 | 0.7 | 61 | 244 | 1 | 1 | ✓ | Х |
| DenseNet-161 [36] | 2016 | 224×224 | 161 | 7.9 | 28.7 | 115 | 1 | 1 | ✓ | Х |
| ResNet-18 [37] | 2015 | 224×224 | 18 | 1.8 | 11.7 | 46 | 1 | 1 | ✓ | Х |
| ResNet-50 [37] | 2015 | 224×224 | 50 | 4.1 | 25.6 | 102 | 1 | 1 | ✓ | × |
| SqueezeNet-V1 [38] | 2016 | 224×224 | 15 | 0.4 | 1.2 | 5 | 1 | ✓ | ✓ | × |
| VGG-16 [39] | 2014 | 224×224 | 16 | 15.4 | 138.36 | 553 | 1 | ✓ | ✓ | × |
| Inception-V3 [40] | 2015 | 299×299 | 48 | 2.9 | 27.2 | 101, 25* | 1 | 1 | ✓ | 1 |
| MobileNet-V1 [41] | 2017 | 224×224 | 28 | 1.1 | 4.3 | 17, 4.5* | 1 | 1 | ✓ | 1 |
| MobileNet-V2 [42] | 2018 | 224×224 | 20 | 0.3 | 3.5 | 14, 4* | 1 | 1 | √ | ✓ |

✓ denotes that the model runs on the DL FW, ✗ denotes that the model does not support the DL FW, * means information for TFLite.

have the suitable model sizes to be deployed on the resource-constrained edge devices to perform DL inference tasks (e.g., image classifications). Moreover, all these models have unique characteristics and behaviors, such as different network architectures, number of layers, number of parameters, and model sizes. Such differences and the overview of the nine selected models are described in Table I.

DL Frameworks. We also used four widely-used open-source DL frameworks; PyTorch [43], MXNet [44], Tensor-Flow (TF) [45], and TensorFlow Lite (TFLite) [46]. PyTorch, MXNet, and TF were used for performing CPU- and GPU-based DL inference tasks on edge devices (e.g., J.TX2, J.Nano, ODN2, and RPi4). TFLite was used to run DL models on EdgeTPU (e.g., DevBoard and USB-Accelerator).

Table I also shows DL frameworks' support for DL models. All DL models are available for PyTorch, TF, and MXNet. However, Inception-V3, MobileNet-V1, and MobileNet-V2 are the only DL models whose pre-trained *quantized* versions are available for TFLite.

DL Applications and Dataset. For the DL inference task, we used *image classification*, which is a common use case of computer vision and can be used as a key component in various AI applications (e.g., drone-based surveillance, hazard zone detection in autonomous driving) in edge computing [2], [16]. In an image classification task on edge, a pre-trained DL model determines text labels (e.g., dog or cat) from input image streams based on the contents. The DL models often generate multiple text labels for input images with the probabilities for images associated with a specific image class.

We used the validation dataset from ImageNet ILSVRC-2012 [47] for input images to DL inference tasks. The validation dataset contains 50K labeled images for 1K different object categories.

III. EVALUATION OF AI SINGLE-TENANCY ON EDGE DEVICES AND ACCELERATORS

We first evaluated and characterized the performance of the edge devices and the accelerators with single-tenancy cases. The results measured in this section will be used as baselines for comparison with AI multi-tenancy cases.

A. Measurement Methodology

To quantify the performance of single tenancy cases on the edge devices and the AI accelerators, we focused on the inference throughput of DL models as the main performance metric. The DL inference throughput results with AI single-tenancy were measured with a set of different configurations, which were the combinations of devices, DL models, batch sizes, DL frameworks. Please note that we tested various batch sizes ranging from 1 to 256, but we only report the batch size resulting in the highest inference throughput. Moreover, the maximum executable batch size could vary across different edge devices and DL models due to the limitation of devices' HW capacity (e.g., memory size) and the size of DL models. The DL inference throughput is calculated by equation-(1). For the single-tenancy case, the number of inferences in equation-(1) is calculated by "batch size" × "the number of batches."

$$DL \ Throughput = \frac{Number \ of \ Inferences}{Total \ Execution \ Time} \qquad (1)$$

Measurement Procedure.

We developed a benchmarker to measure the DL inference throughput and collect necessary system statistics. We deployed the benchmarker along with an image classification application on the devices and EdgeTPUs accelerators. The measurement procedure of the benchmarker is shown in Fig. 1.

The benchmarker begins by taking specific parameters for the measurement (step #1), including the DL model, DL framework, batch size, and others. Then, the benchmarker starts a DL framework-

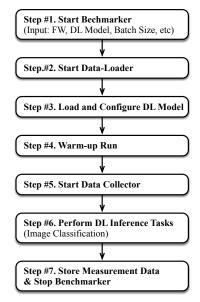


Fig. 1: Measurement steps

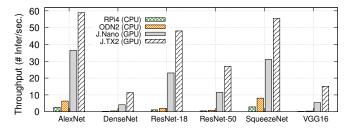


Fig. 2: Inference throughput of 6 DL models on edge devices using CPU and GPU resources. Note that throughput results of CPU- and GPU-based inference results are the average of the maximum throughput results from PyTorch, TF, and MXNet.

specific data-loader (step #2) that prepares input images (as per the batch size) from the dataset (ImageNet ILSVRC-2012) and sends them to the DL model. In step #3, the benchmarker loads the DL model into the main memory and configures it based on the parameters (e.g., use of CPU, GPU, or EdgeTPU). The next step (step #4) is the warm-up run phase, which ensures all the necessary components are loaded, and the DL framework configures suitable optimization strategies before performing the actual measurement. After the warm-up run, the benchmarker starts a data collector (step #5) that contains tools for measuring system statistics (e.g., sysstat) and power consumption (e.g., INA-219). Then, in step #6, the benchmarker performs DL inference tasks (image classification) for input images received from the data-loader. The inference tasks are performed at least 30 times to increase the statistical confidence of the measured data. While the inference tasks are performed, the data collector continuously measures resource usage and power consumption. After completing all the inference tasks, the benchmarker saves the measured data, and it will be terminated (step #7).

System Statistics and Power Measurement. In the above measurement step, diverse system statistics were collected while the inference tasks were being performed. sysstat [48] was used to collect the usage of CPU, memory, and Disk/USB IO.

For measuring the power consumption of edge devices, we used INA-219 [49], a voltage, current and power measurement chip. With a default resistance of $0.1\,\Omega$, the chip allows measuring the power consumption with a current sensing range of $\pm 3.2\,\mathrm{A}$ and a voltage range of $0\,\mathrm{V}$ to $26\,\mathrm{V}$. We used pi-ina219 [50], a python library to communicate with the INA-219 chip. We also used jetson-stats [51], a python library that provides power consumption statistics leveraging Nvidia's tegrastats utility [52] to measure the power consumption of J.TX2 and J.Nano. For EdgeTPUs, we used a USB power meter.

B. Measurement Results with Single-Tenancy

DL Inference Throughput with Single-Tenancy. Fig. 2 reports the maximum DL inference throughput with single-tenancy when the DL models were executed on either CPU or GPU resources in edge devices. The results show that

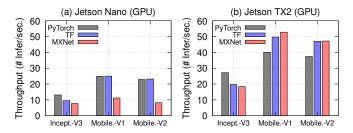


Fig. 3: GPU-based inference throughput variations across three different DL frameworks. While the results report GPU-based inference throughput with three models, the other 6 DL models showed similar patterns.

the inference throughput results varied significantly across different DL models as they had different model sizes, network architectures, and a set of parameters. The results also confirm that the GPU-based DL inference results showed significantly improved throughput over the CPU-based inference as GPU is more specialized in processing AI and ML workloads. The edge devices with GPUs (e.g., J.Nano and J.TX2) processed $4\times-96\times$ more inference requests compared to the devices without GPUs (RPi4 and ODN2). On average, J.Nano showed $23\times$ and $13\times$ higher throughputs over RPi4 and ODN2. J.TX2 had $50\times$ and $28\times$ higher throughput results than RPi4 and ODN2. Moreover, J.TX2 showed $2.28\times$ higher inference throughput than J.Nano because J.TX2's GPU is equipped with a larger capacity GPU module (128 GPU cores in J.Nano vs. 256 GPU cores in J.TX2).

Moreover, we observed that the inference throughput results with GPU (e.g., J.Nano and J.TX2) could vary significantly across three DL frameworks, as shown in Fig. 3. In particular, MXNet on J.Nano showed exceptionally (55%) lower performance than the other two frameworks. (But GPU with MXNet on J.TX2 did not show low inference throughput.) The lower performance with MXNet on J.Nano was due to MXNet's optimization mechanism to find the best convolution algorithm for inference tasks with DL models. Unfortunately, this is a memory-intensive operation, and J.Nano's 4GB memory is not large enough to complete this optimization step so that MXNet on J.Nano showed poor inference throughput. We found the same issue in our evaluation of AI multi-tenancy when using MXNet with the CME technique. We will provide a detailed analysis of this problem in Section IV-A.

Fig. 4 shows the comparison of maximum throughput of three DL models when they were executed on CPU, GPU, and EdgeTPU resources. To compute the throughput (red bar in the figure) of USB-Accelerator, we used four combinations³ of edge devices and USB-Accelerator, and we report the average of the maximum throughput of all four combinations. As expected, both GPU and EdgeTPU-based inferences showed $10 \times -63 \times$ higher throughput than CPU-based inferences. Between the GPU and EdgeTPU resources,

³The four combinations are RPi4 with USB-Accelerator, ODN2 with USB-Accelerator, J.Nano with USB-Accelerator, and J.TX2 with USB-Accelerator.

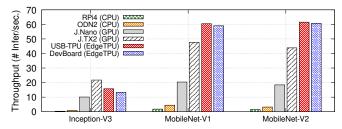


Fig. 4: Inference throughput of Inception-V3, MobileNet-V1, and MobileNet-V2 using CPU, GPU, and EdgeTPU. The throughput results of CPU- and GPU-based inferences are averages of maximum throughput results from PyTorch, TF, and MXNet. USB-Accelerator's throughput is the average of throughput results obtained from USB-Accelerator connected with four edge devices.

TABLE II: EdgeTPU throughput variation across different host edge devices.

| Model | Host Device + EdgeTPU | Avg. Through. | Std. Dev. | |
|-----------|--------------------------|---------------|-----------|--|
| | RPi4 + USB-Accelerator | 12.35 | 0.35 | |
| Inception | ODN2 + USB-Accelerator | 0 0 | 0.47 | |
| -V3 | J.Nano + USB-Accelerator | 16.42 | 0.34 | |
| - • • • | J.TX2 + USB-Accelerator | 18.54 | 0.48 | |
| | DevBoard Only | 13.26 | 0.19 | |
| | RPi4 + USB-Accelerator | 54.65 | 4.03 | |
| MobileNet | ODN2 + USB-Accelerator | 58.84 | 6.73 | |
| -V1 | J.Nano + USB-Accelerator | 63.60 | 5.58 | |
| - V 1 | J.TX2 + USB-Accelerator | 64.65 | 5.45 | |
| | DevBoard Only | 59.02 | 2.48 | |
| | RPi4 + USB-Accelerator | 55.79 | 4.15 | |
| MobileNet | ODN2 + USB-Accelerator | 59.70 | 5.78 | |
| -V2 | J.Nano + USB-Accelerator | 66.61 | 4.23 | |
| - • 2 | J.TX2 + USB-Accelerator | 64.01 | 6.57 | |
| | DevBoard Only | 60.67 | 5.23 | |

while J.TX2's 256-core Pascal GPU showed the maximum throughput (even higher than EdgeTPU's throughput) with Inception-V3, both DevBoard and USB-Accelerator showed 25% – 41% higher throughput than J.TX2 for performing inferences with MobileNet-V1/V2.

Table II reports EdgeTPU throughput fluctuations across different host edge devices. In particular, when performing DL inference tasks using Inception-V3, USB-Accelerator showed up to a 33% difference in the inference throughput on the different host devices. Several factors can result in such throughput fluctuations. Memory bandwidth on the (host) edge devices can be a factor for such fluctuations. For example, the latency when swapping in/out of a DL model and its parameters between the host devices and USB-Accelerator rely on the memory bandwidth. Furthermore, both storage IO and USB IO can also be factors for changing the DL inference throughput. Regarding these factors, we will further analyze them in the following paragraph.

Factors for Impacting DL Inference Throughput Changes. To identify factors that change the DL inference throughput on edge devices and EdgeTPUs, we performed correlation analysis by calculating the Pearson correlation coefficient (in equation-(2)) [53] of measured throughput results and

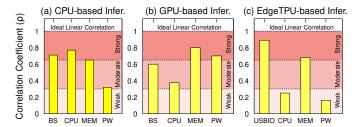


Fig. 5: Correlated factors that change the inference throughput. (BS: Batch Size, CPU: CPU usage, MEM: memory usage, PW: Power consumption, USBIO: USB IO bandwidth usage)

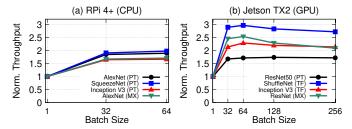


Fig. 6: Throughput changes with different batch sizes.

resource usage statistics. This coefficient represents the linear relationship between two variables, ranging from -1 to 1. Please note that the coefficient of 1 indicates an ideal positive correlation, negative values mean reverse correlation, and 0 means there is no correlation between two variables.

$$\rho = \frac{cov(x,y)}{\sigma_x \sigma_y} = \frac{\sum_i^n (x_i - \overline{x})(y_i - \overline{y})}{\sqrt{\sum_i^n (x_i - \overline{x})^2 (y_i - \overline{y})^2}}$$
(2)

Fig. 5 shows the correlated factors for the DL inference throughput when using CPU, GPU, and EdgeTPU. For the CPU-based inferences (e.g., RPi4, ODN2), the CPU, batch size, and memory were strongly correlated with the inference throughput results. CPU resources were mainly used to perform the DL tasks, and memory resources were used to load and store the DL models. The inference tasks with larger batch sizes naturally increased the input data for processing so that an increase in the batch sizes could improve the throughput until the limit of device resources.

For the GPU-based inference tasks (e.g., J.Nano and J.TX2), memory, power, and batch sizes were positively correlated with the DL inference throughput. Specifically, the power consumption showed a strong correlation with the throughput as the GPU module in edge devices consumed more power than typical CPUs in edge devices. And, CPU showed a relatively weaker correlation with the throughput as CPU was only used for managing the device and processes co-running (non-DL) applications rather than performing the DL tasks. Because the batch size showed a strong correlation for both the CPU and GPU-based inference tasks, we report the impact of batch size changes in Fig. 6. As shown in the results, the batch sizes changed the DL inference throughput significantly. In general, a larger batch size appeared to result in increased

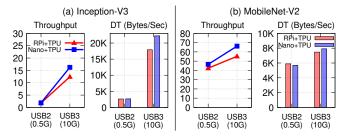


Fig. 7: Difference in DL inference throughput and data transfer with USB 2.0 and 3.0 interfaces. (DT: Data Transfer Amount)

throughput; however, an interesting observation is that using larger batch sizes did not always increase the DL inference throughput. This suggests that employing the right (or optimal) size of the input batch will be critical for improving the DL inference throughput on edge devices.

In the EdgeTPU-based inferences cases, the USB bandwidth (between a host edge device and the USB-Accelerator) and memory usage on host edge devices strongly correlated with the inference throughput. Both memory and USB IO were closely related to each other for executing DL models on the USB-Accelerator. Because USB-Accelerator does not have main memory (RAM)⁴, it relies on the host device's memory system to store models and uses context switching to swap models/parameters between the host device's RAM and EdgeTPU to perform DL inference tasks. Therefore, low USB IO bandwidth between the host device and USB-Accelerator limits data rates for switching models and parameters so that the throughput can decrease.

To further investigate the impact of the USB IO bandwidth, we measured the DL inference throughput changes from USB-Accelerator by connecting it with two edge devices (RPi4 and J.Nano). Also, to observe the throughput changes with different bandwidth, we used two USB interface types. i.e., USB 2.0 with up to 0.5GB of bandwidth, USB 3.0 with up to 10GB of bandwidth. As shown in Fig. 7, the results confirm that USB's IO bandwidth could considerably change the DL inference throughput of EdgeTPUs. With larger IO bandwidth supported by USB 3.0, RPi4 achieved 1.3× (MobileNet-V2) and 7× (Inception-V3) higher throughput than the inference with USB 2.0. J.Nano also showed 1.4× (MobileNet-V2) and 8.7× (Inception-V3) higher throughput than USB-Accelerator with USB 2.0. Larger USB IO bandwidth facilitated the switching of model parameters and input data between the host device and USB-Accelerator so that it significantly improved the overall DL inference throughput.

Summary. This section characterized the performance and behaviors of edge devices and EdgeTPU accelerators with AI single-tenancy, focused on the inference throughput. We found several factors that changed the DL inference throughout as well as identified correlated resources for the throughput changes. In the next section, these results will be used as

baselines for evaluating and characterizing the AI multitenancy on edge devices and EdgeTPUs.

IV. EVALUATION OF AI MULTI-TENANCY ON EDGE DEVICES AND ACCELERATORS

This section evaluates and characterizes two techniques for enabling AI multi-tenancy on edge devices and EdgeTPUs.

A. AI Multi-Tenancy with Concurrent Model Executions

Concurrent model executions (CMEs) leverage the idea of parallel processing and enable AI multi-tenancy by simultaneously executing multiple DL inference tasks on edge devices' resources. e.g., deploying and executing multiple DL models on either GPU or EdgeTPUs. CME can provide two potential benefits to edge devices and EdgeTPUs; 1) improving DL inference throughput and 2) allowing to run multiple (often different) DL services (e.g., inference tasks). Therefore, it is important to correctly identify the upper bound of throughput improvement and the concurrency level (the number of corunning DL models) on the devices' resources by CME. Moreover, the maximum concurrency level may not provide the highest throughput, so it is also important to determine the concurrency level that results in the highest throughput. Therefore, we performed an empirical evaluation of CME with DL models to answer the following questions;

- 1) What is the maximum DL inference throughput of the edge devices and EdgeTPUs with CME?
- 2) What is the maximum concurrency level on the edge devices and EdgeTPUs with CME?
- 3) What is the concurrency level on edge devices and EdgeTPUs to maximize DL inference throughput?

In this evaluation, we used three DL models (e.g., Inception-V3, MobileNet-V1, MobileNet-V2) for evaluating CME because all these models could be executed on three resource types in edge devices and EdgeTPU accelerators. Among all DL frameworks, we excluded TF from this CME evaluation since TF is not thread-safe. Specifically, kerascv [54] and tf.Graph [55] libraries did not fully support concurrent executions. Regarding the throughput calculation with CME, we changed equation-(1), and the number of inferences in the equation was calculated by "concurrency level" × "batch size" × "the number of batches."

Evaluation Steps for CME. We began the CME evaluation by deploying and executing a single DL model on edge devices and EdgeTPU. We then gradually increased the number of co-running DL models ("concurrency level") on the devices and EdgeTPUs to measure the changes in the DL inference throughput and resource usage patterns. This experiment was continued to increase the concurrency level until the benchmarker failed to run. The concurrency level obtained from the last successful execution was considered as the maximum concurrency level supported by the edge devices and EdgeTPUs. In this measurement, we only report the results with leveraging CME on GPUs (J.Nano and J.TX2) and EdgeTPUs (DevBoard and USB-Accelerator), and we omit the measurement results from CPU resources. This is

⁴USB-Accelerator has only 8MB of cache memory (SRAM).

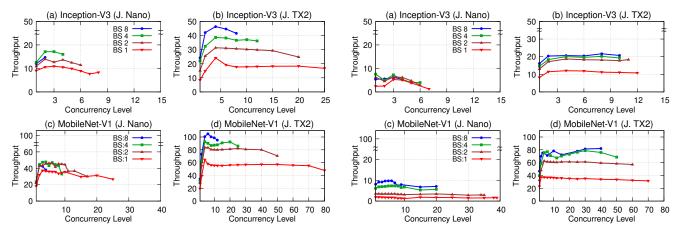


Fig. 8: CME measurement results of throughput and concur- Fig. 9: CME measurement results of throughput and concurrency level on GPUs with PyTorch (BS: Batch Size)

rency level on GPUs with MXNet (BS: Batch Size)

because, while we could find some benefits of CME on CPUs, e.g., six concurrent models could be executed on CPUs of RPi4 and ODN2, the throughput benefits were marginal, and the measured throughput results were exceptionally lower than the results with CME on either GPUs or EdgeTPUs.

CME Evaluation Results on GPUs. Fig. 8 and 9 show DL inference throughput changes with different concurrency levels on GPUs in J.Nano and J.TX2. Please note that, in both graphs, we omit the results from MobileNet-V2 due to the page limit, and the results were similar to the results with MobileNet-V1.

When enabling CME on GPU using PyTorch (shown in Fig. 8), the maximum concurrency level and throughput varied with different batch sizes. DL inference with a batch size of 1 provided the maximum concurrency level. We observed that J.Nano could run 8 (Inception-V3) to 25 (MobileNet-V1) models concurrently on GPU, and J.TX2 was able to deploy 25 (Inception-V3) to 80 (MobileNet-V1) models on its GPU simultaneously. Using larger batch sizes (e.g., batch size of 4 for J.Nano, batch size of 8 for J.TX2), the multi-tenancy enabled by CME significantly improved the DL throughput against the single-tenancy cases. In particular, with CME, J.Nano showed $1.3 \times$ to $1.9 \times$ improved throughput, and J.TX2 showed $1.7 \times$ to $2.7 \times$ higher throughput against the single-tenancy cases. Our further analysis revealed that memory resource was the critical factor to determine the maximum throughput when enabling CME. As Fig. 10 shows, the maximum throughput was highly correlated with memory utilization. Both J.Nano and J.TX2 showed that the maximum throughput was reached when the memory resource was saturated. After reaching the maximum throughput, the throughput was either decreased or stabilized with high memory utilization. It is worth noting that the high correlation between memory utilization and throughput increase was consistent with our observation reported in Fig. 5 in the previous section.

However, the CME evaluation with MXNet showed different results from the previous measurements with PyTorch. Both J.Nano and J.TX2 had lower throughput improvement. In particular, J.Nano showed considerably low performance,

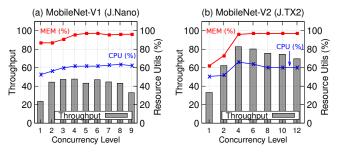


Fig. 10: Resource utilization and throughput changes with CME (PyTorch). J.Nano uses a batch size of 4, and J.TX2 employs a batch size of 8.

and on average, J.Nano with MXNet had even 13% lower throughput than single-tenancy cases. This low throughput was because J.Nano's experiments were performed by disabling MXNet's cuDNN auto-tune [56] parameter so that the framework used sub-optimal convolution layers for cuDNN. Enabling or disabling auto-tune option can significantly impact DL inference throughput because, if this option is enabled, MXNet first runs a performance test to seek the best convolutional algorithm, and the selected algorithm is used for further inference tasks. However, this performance test requires significant consumption of resources on edge devices. Unfortunately, due to the smaller memory size (4GB), J.Nano could not complete this performance test due to the frequent out-of-memory errors.

For J.TX2, while the throughput benefits using CME were smaller than the throughput with PyTorch, it showed 1.12× to $1.5 \times$ higher throughput compared to the single-tenancy cases. Regarding the concurrency level supported by CME with MXNet, J.Nano successfully ran 6 (Inception-V3), 39 (MobileNet-V1), and 45 (MobileNet-V2) concurrent models, and J.TX2 could run 12 (Inception-V3) and 70 (MobileNet-V1 and MobileNet-V2) models with a batch size of 1.

CME Evaluation Results on EdgeTPUs. Fig. 11 reports DL inference throughput variations with different concurrency

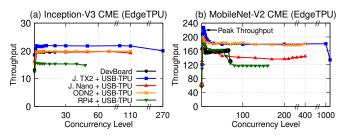


Fig. 11: DL inference throughput variations by enabling CME on EdgeTPUs

levels on EdgeTPUs (both DevBoard and USB-Accelerator). USB-Accelerator's throughput and concurrency level results were measured using four edge devices. Similar to the previous results on GPUs, CME on EdgeTPUs could also increase throughput over the single-tenancy cases. For Inception-V3 (Fig. 11(a)), DevBoard had 1.3× higher throughput, and USB-Accelerators showed 1.25× improved throughput over single-tenancy cases. For both MobileNet-V1 and MobileNet-V2 (Fig. 11(b)), EdgeTPUs showed 3.3× higher throughput over the single-tenancy cases. Please note that we omit the throughput results with MobileNet-V1 because the results are similar to MobileNet-V2.

In this evaluation, we found two interesting observations about the throughput improvement. One is that CME's throughput increase with Inception-V3 (1.3×) was much smaller than MobileNet-V1/V2 $(3.3\times)$. The other is that MobileNet-V1/V2 reached the maximum throughput with lower concurrency levels, and the throughput is decreased and stabilized with higher concurrency levels. Our further analysis revealed that the above two issues were related to the model size and EdgeTPU's 8MB of SRAM used to cache the DL model's parameters. In particular, a smaller throughput increase with Inception-V3 was because 25MB of Inception-V3 size could not be fully loaded in the EdgeTPUs' cache (SRAM), and thus, model parameter swapping operations between the EdgeTPU's cache and the edge devices' memory were continuously being performed. Therefore, the increased concurrency level did not increase the inference throughput due to the high overhead in the model parameter swaps. On the other hand, if the model size was small, e.g., 4MB of MobileNet-V2, the model could be fully loaded in EdgeT-PUs' cache and did not require frequent operations of model parameter swapping, hence low USB IO overhead and possibly significant throughput increases.

Regarding the second observation found in Fig. 11(b), the EdgeTPU cache could load even multiple smaller models simultaneously. While EdgeTPU could leverage only one model at a time, other loaded models were able to obtain data from the host device's memory, hence minimizing the delay when switching models in EdgeTPUs. On the other hand, if the concurrency level was high, frequent model swaps needed to be frequently performed in EdgeTPU's cache, resulting in increased data transfer between EdgeTPU and the host edge device's memory. Therefore, USB IO was quickly saturated, and

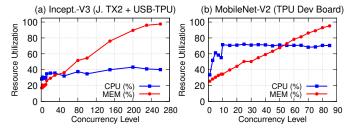


Fig. 12: Resource utilization changes with increased concurrency level (EdgeTPUs)

throughput could be degraded. This is why both MobileNet-V1 and MobileNet-V2 reached the maximum throughput with a low concurrency level, and throughput could be decreased and stabilized with higher concurrency levels. This analysis suggests that, when using CME on EdgeTPU, model size and concurrency level should be carefully determined to increase the throughput. Moreover, model compression techniques [16], e.g., quantization and parameter pruning, should be considered for optimizing model size for EdgeTPUs.

The three models reported much higher concurrency levels on EdgeTPUs than the concurrency level on GPUs. DevBoard supported the concurrency level of 20 for Inception-V3 and the concurrency level of 80 - 85 for both MobileNet-V1/V2 models. Furthermore, USB-Accelerators reached various maximum concurrency levels. Specifically, USB-Accelerators' concurrency levels varied considerably across different host edge devices. For example, for Inception-V3, the maximum concurrency level from USB-Accelerator with RPi4 was 48, but when it used J.TX2 as the host device, the maximum concurrency level reached 270. For MobileNet-V2, the maximum concurrency level from USB-Accelerator with RPi4 was 160, but it could be 1100 when leveraging J.TX2 as the host edge device. Regarding the varying concurrency levels, our further analysis revealed that the maximum concurrency levels supported by USB-Accelerators had a high correlation with the size and utilization of memory resources in the host edge devices. Fig. 12 shows resource utilization changes with different concurrency levels measured from USB-Accelerator with J.TX2 and DevBoard. The results show that memory utilization increased as the concurrency level went up. The maximum concurrency level was determined when the memory utilization reached close to 100%, indicating that memory size and bandwidth often limit the supported concurrency level DL models when enabling CME on USB-Accelerator.

B. AI Multi-Tenancy with Dynamic Model Placements

This section characterizes and evaluates the dynamic model placement (DMP) technique for AI multi-tenancy on edge devices and EdgeTPUs. DMP allows running multiple DL models simultaneously by placing DL models on an edge device's resource (CPU and/or GPU) and other DL models on EdgeTPUs. Because USB-Accelerator can be connected to edge devices via USB interfaces, the potential benefits from DMP can be improved DL inference throughput using hetero-

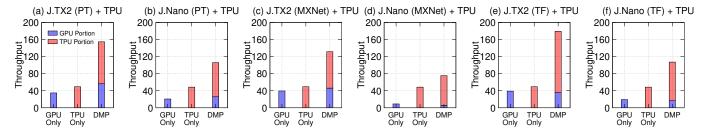


Fig. 13: Comparison of DL inference throughput between DMP and single-tenancy.

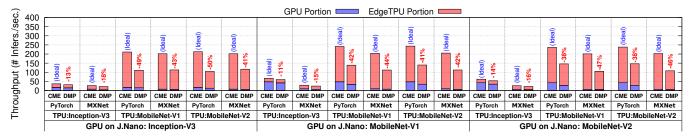


Fig. 14: J.Nano's DL inference throughput comparison between (ideal) results from CME and DMP. The (ideal) results from CME are calculated by the sum of CME throughput on GPU and CME throughput on EdgeTPU, which were measured separately.

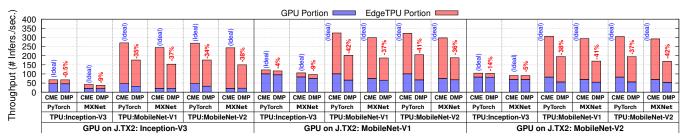


Fig. 15: J.TX2's DL inference throughput comparison between (ideal) results from CME and DMP. The (ideal) results from CME are calculated by the sum of separately measured CME throughput on GPU and EdgeTPU.

geneous resources in both edge devices and USB-Accelerator as well as high resource utilization of both resources. However, DL inference tasks from both on-board edge resources and USB-Accelerator are managed by the host edge devices so that there can be a performance penalty from resource contention. Therefore, in this evaluation, we focus on seeking answers to the following research questions;

- 1) What are the performance benefits (e.g., DL inference throughput) from DMP on heterogeneous resources?
- 2) What are the actual performance penalties of using DMP, compared explicitly to CME for AI multi-tenancy?

Similar to the CME evaluations, we used three DL models (Inception-V3, MobileNet-V1, and MobileNet-V2) because these models could perform inference tasks on all resource types in edge devices and EdgeTPUs. We also changed the equation-(1) to correctly calculate the throughput with DMP. Specifically, the number of inferences for DMP was calculated by the sum of the inference numbers from edge resources (CPU or GPU) and the inference numbers from USB-Accelerator.

We initially used four edge devices (RPi4, ODN2, J.Nano, J.TX2) connected with a USB-Accelerator and deployed DL models on both edge resources and the USB-Accelerator. However, we omit the evaluation results of RPi4 and ODN2 because we could not observe the benefits of using DMP on such devices. Specifically, CPUs on RPi4 and ODN2 were quickly saturated by both CPU-based and EdgeTPU-based DL inference tasks, and the overall inference throughput results with DMP on RPi4 and ODN2 could be even lower (about 10%) than EdgeTPU-only inference throughput.

We evaluated DMP with three DL frameworks for GPUs and TFLite for EdgeTPU. We enabled CME when the models are running on PyTorch (GPU), MXNet (GPU), and TFLite (EdgeTPU), and we used single-tenancy with TF on GPU.

DMP Evaluation Results. Fig. 13 shows DMP's DL inference throughput improvement against the single-tenancy cases. Both J.Nano and J.TX2 showed significantly increased throughput compared to the single-tenancy GPU or EdgeTPU-based inferences. In particular, J.Nano had $6.2\times$ improved throughput over the single-tenancy on GPU and $2\times$ increased

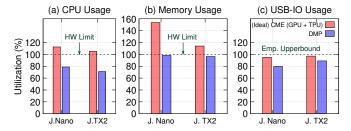


Fig. 16: Resource usage comparison between (ideal) sum of CME on GPU/EdgeTPU and DMP.

throughput over the single-tenancy on EdgeTPU. J.TX2 also showed throughput improvement by $3.8\times$ (for GPU) and $3.1\times$ (for EdgeTPU). However, this improved throughput can be in part due to leveraging both CME and DMP. We also compare the DL inference throughput between ideal throughput upper bound based on CME results (reported in Section IV-A) and DMP. Please note that the ideal throughput upper bound is calculated by accumulating GPU throughput with CME and EdgeTPU throughput with CME measured separately.

Fig. 14 and 15 report the throughput comparison between (ideal) CME results and DMP. The results contain the results measured from J.Nano and J.TX2 when using PyTorch/MXNet (for GPU) and TFLite (for EdgeTPU). As shown in the figures, while the differences between the ideal throughput and DMP's throughput varied with DL models and DL frameworks, J.Nano with DMP (Fig. 14) and J.TX2 with DMP (Fig. 15) showed 34.6% and 25.3% lower DL inference throughput than the ideal throughput with CME (on both GPU and EdgeTPU). Such differences were mainly due to the resource contention and resource limits in the edge devices.

To understand the gap between the DMP's throughput and ideal throughput, we performed further analysis on resource consumption. Fig. 16 shows the resource utilization (CPU, memory, USB IO) between the ideal sum of CME on GPU/EdgeTPU and DMP. As shown in the figure, the ideal throughput often could not be achievable with current HW specifications. Specifically, CPU and memory utilization should exceed the HW limits of the edge devices (more than 100%) to reach such high throughput. Moreover, similar to the CME analysis, memory was identified as a critical resource when enabling DMP. Specifically, we observed that memory utilization reached 100% with DMP, but CPU utilization did not reach 100%. Based on this observation, the DL inference throughput, when the memory resource is saturated, can be the empirical performance upper bound when enabling DMP. We also observed that resource contention could impact the DL inference throughput because the shared resources, such as memory and CPU, were needed to manage multiple DL models running on different resources. The decreased USB IO utilization (about 8% to 15%) with DMP (Fig. 16(c)) was because of such resource contentions, and the reduced USB IO utilization could decrease DL inference throughput from EdgeTPU in USB-Accelerator.

V. AI MULTI-TENANCY SUMMARY AND DISCUSSION

This section describes a summary of our evaluation results with CME and DMP and discusses important findings regarding AI multi-tenancy on edge devices.

When enabling CME on GPUs for AI multi-tenancy, we observed significant DL throughput improvement over singletenancy cases. In particular, J.Nano and J.TX2 showed 1.3× to 2.7× improved throughput, and both devices support the concurrency levels of 8 (Inception-V3 on J.Nano) to 80 (MobileNet-V1 on J.TX2). However, we found that high concurrency levels did not necessarily result in improving DL inference throughput. Moreover, both concurrency level and batch sizes can significantly change the DL inference throughput, so both configurations should be carefully determined and optimized when applying CME on GPUs. We also observed that the maximum throughput with CME on GPU could be determined when the memory utilization reached 100%. Finally, the throughput benefits of CME on GPUs can vary across different DL frameworks and edge devices. Sometimes, the throughput benefit can be limited, especially when applying CME on GPU with MXNet on edge devices with small memory sizes like J.Nano.

When enabling CME on EdgeTPUs, our evaluation confirmed considerable performance benefits, and high concurrency levels could be achieved. However, similar to CME on GPUs, high concurrency levels did not necessarily result in the maximum DL inference throughput. We observed that DL inference throughput could be affected by the DL model size and the small cache size in EdgeTPUs. Specifically, if the DL model size could not fit in the small cache (8MB) of EdgeT-PUs, the benefits of using CME could be limited. Moreover, lower concurrency levels often resulted in a maximum performance gain when using small DL models (e.g., MobileNet-V1/V2). This observation strongly suggests that the techniques for minimizing model size (e.g., quantization and model compression) will be critical for the throughput improvement. Moreover, we observed that the maximum concurrency level could be determined when the memory utilization reaches near 100%. This observation indicates that host edge devices' memory capacity can be critical for increasing the concurrency level when using USB-Accelerator.

When enabling DMP for AI multi-tenancy, our evaluation confirmed that DMP considerably improved DL inference throughput over single-tenancy cases by leveraging GPU and EdgeTPU resources simultaneously. We also compared the DMP's throughput against the ideal inference throughput, which was the sum of the maximum throughputs when applying CME on both GPU and EdgeTPU. While the DMP's maximum throughput showed 25% to 35% lower throughput than the ideal inference throughput, such differences were mainly due to the HW limitations. We also observed that memory could be the critical resource factor when enabling DMP, and memory resources were saturated when reaching the maximum throughput. We found the impact of resource contention with DMP. In particular, USB IO bandwidth usage

was decreased when applying DMP, and the reduced usage resulted in lower throughput from EdgeTPU.

VI. RELATED WORK

Several studies have been conducted to quantify the performance of various edge devices for DL/ML inference tasks [23]–[28]. However, most studies have focused on characterizing performance (e.g., latency and throughput) and efficiency (e.g., energy consumption) of edge devices and AI accelerators with single DL tasks.

pCamp [23] evaluated ML packages and frameworks' performance when executing image classification tasks on edge platforms, including J.TX2, RPi4, and Nexus 6p. This work reported latency (including model loading time), memory usage, and energy consumption from different ML packages. Hadidi et al. [27] have characterized various edge devices and AI accelerators (e.g., EdgeTPUs) with DL inference tasks. The authors analyzed the impact of DL frameworks and SW stacks as well as measured energy consumption and temperature when performing DL inference tasks. Moreover, several studies [24], [25], [57] have focused on characterizing the performance of DL inference tasks on different HW architectures and resource models (CPU, GPU, EdgeTPU). EmBench [24] has performed a per-layer analysis of DL inference tasks to identify performance bottlenecks. Libutti et al. [26] conducted performance evaluations of DL inference tasks with portable, USB-based edge accelerators, including Coral USB Accelerator and Intel Neural Compute Stick [58].

More recently, Liang et al. [28] have conducted an experimental study to evaluate model splitting and compression techniques on edge devices and accelerators. Network latency, bandwidth usage, and resource utilization with various configurations were also reported when applying model splitting and compression to cloud-edge co-inference usecases. Additionally, the authors have evaluated the concurrency model executions for multi-tenancy use cases. However, the concurrency evaluation is narrowly performed with only one model having a single batch size. Moreover, in addition to evaluating the CME strategy, our work also evaluated and characterized the DMP strategy for AI multi-tenancy that leverages heterogeneous resources in edge and EdgeTPU.

VII. CONCLUSION

In this work, we evaluated the performance of two AI multitenancy techniques for edge computing; CME (Concurrent Model Executions) and DMP (Dynamic Model Placements). These two techniques were evaluated on various edge devices and EdgeTPU accelerators with widely used DL frameworks and models for image classification tasks. Our evaluation confirmed that both AI multi-tenancy techniques could significantly improve the DL inference throughput. We empirically identified the maximum concurrency level of DL models supported by various edge devices and EdgeTPU accelerators for the CME technique. Moreover, we also investigated resource factors impacting the concurrency level with CME. We also identified the benefits and limitations of DMP on heterogeneous resources. Specifically, memory resources can be the critical resource factor determining the maximum DL inference throughput with DMP. Additionally, we observed that the USB IO bandwidth usage could be decreased due to the resource contention from DMP.

Both techniques open up new opportunities for AI multitenancy, including flexible and high-performance DL service deployment. Furthermore, further research efforts need to be followed to maximize the benefit of AI multi-tenancy, such as safe placement of multiple DL models to minimize the resource contention and a better isolation mechanism for dynamic control of DL inference throughputs.

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