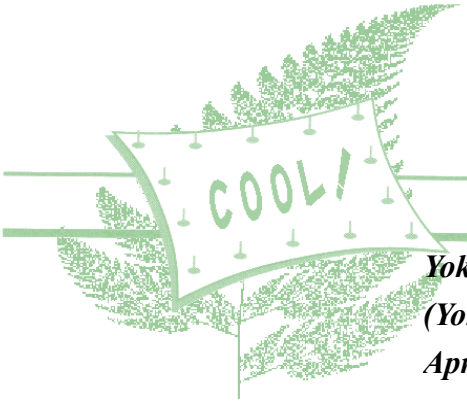


# *2013 IEEE COOL Chips XVI*

***Yokohama Joho Bunka Center, Yokohama, Japan***
***(Yokohama Media & Communications Center, Yokohama, Japan)***
***April 17-19, 2013***

## *Message from the Program Committee Chairs*

Welcome to COOL Chips XVI, an international symposium that provides you with the latest developments on low-power and high-speed chips. This year we are bringing you an exciting program that includes four keynote speeches, three invited talks, and two instructive special sessions in this noble harbor city of Yokohama.

We have three keynote speeches on 18th April. The first one will be given by Dr. Michael McCool from Intel Corp. He will talk about power management facilities in Intel processors across the compute continuum. The second one will be from Dr. Shintaro Momose of NEC, Japan. He will give us the next generation vector supercomputer. The third one will be from Dr. Bert Gyselinckx of Holst Centre, IMEC. He will give us very small and very low power chips for healthcare applications.

We have another keynote speech on 19th April. It will be from Dr. Hiroshi Kanayama of IBM, Japan. He will talk about the grand challenge and technologies to build "Watson" a question answering system, including hardware points of view.

We have invited three speakers: Dr. James Myers from ARM, UK will talk about state-retention power-gating strategies of dual-core ARM Cortex-A5 MPCore processor. Mr. Toshio Yoshida from Fujitsu, Japan will talk about Fujitsu's new generation 16 core processor, SPARC64 X. Mr. Takeshi Kataoka from Renesas Mobile, Japan will talk about a single-chip realization of dual-core application processor with baseband processor.

This year's technical presentations will be covered in five sessions: the areas to be covered include multi/many-core processors, low-power processors, HW/SW technologies, resource managements, and 3D technologies. The program committee chose 12 regular papers out of 20 papers submitted to suit the interests of the symposium audiences. The papers were

submitted from around the world, namely, China, Korea, US, France and Japan.

On the first day, April 17th, we will hold two special sessions. The first will be presented by Dr. Pierre G. Paulin of STMicroelectronics, Canada, on STMicroelectronics STHORM, multi-processor fabric and its programming environment. The second is on main memory sub-systems by Prof. Jung Ho Ahn of Seoul National University, Korea and Prof. Sungjoo Yoo of POSTECH, Korea. On April 18th, a poster session organized by Prof. Koji Hashimoto of Fukuoka University will be held with 26 poster short presentations. The posters presented in this session will be exhibited in the poster show room. A panel discussion on the future multi-layer co-design of computer systems will be held on April 18th. We hope to see lively discussion among the panelists and audience.

Many people have contributed to the organization of COOL Chips XVI. We would like to express our sincere thanks to all the members of the Program Committee, Vice Program Chair, Prof. Jun Yao and Hajime Shimada for the great deal of extra work they put into organizing this symposium. Prof. Koji Hashimoto, who acted as Poster chair, Prof. Hiroyuki Tomiyama, who acted as Special Session Chair, and all session chairs for their special contributions to this symposium. Moreover, on behalf of the program committee, we would like to greatly thank Prof. Hiroaki Kobayashi, the organizing committee chair, and all the people of the organizing committee and the advisory committee for their great efforts in making the symposium possible.

Finally, we would like to thank the speakers of this symposium and all attendees. We hope enjoy the COOL Chips XVI.

池田誠

Makoto Ikeda

Co-Chair of the Program Committee

荒川文男

Fumio Arakawa

Co-Chair of the Program Committee