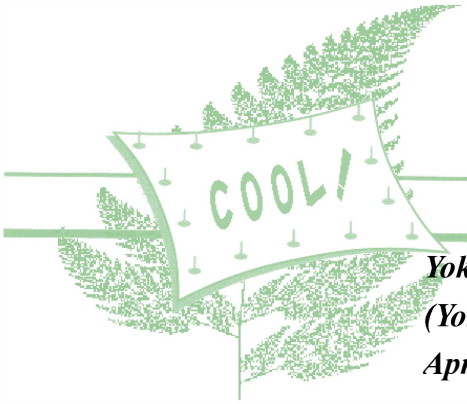


2016 IEEE COOL Chips XIX

Yokohama Joho Bunka Center, Yokohama, Japan
(Yokohama Media & Communications Center, Yokohama, Japan)
April 20-22, 2016

Message from the Program Committee Chairs

Welcome to COOL Chips XIX, an international symposium that provides you with the latest developments on low-power and high-speed chips. This year we are bringing you an exciting program that includes six keynote speeches, one invited talk, two instructive special invited lectures and one panel discussion in this noble harbor city of Yokohama.

We have four keynote speeches on April 21st. The first keynote speech will be given by Dr. Luca Benini of ETHZ. He will talk about the next challenge to sub-pj per operation scalable computing. The second will be from Dr. Ashraf Lotfi of Intel. He will talk about power optimization leveraging FPGA and voltage regulator chip co-design. The third will be given by Mr. Teruo Hirayama of Sony. He will talk about modality of CMOS image sensor competition. The forth will be given by Prof. Oskar Mencer of Imperial College London and Maxeler Technologies. He will talk about a multiscale dataflow computing chip.

We have other two keynote speeches and one invited talk on April 22nd. The first will be from Dr. Michael McCool of Intel. He will talk about new frontiers in computing. The second will be from Prof. Mateo Valero of Barcelona Supercomputing Center. He will talk about cool techniques for hot chips. Mr. Makoto Miyamura of NEC will give an invited talk on NanoBridge-based FPGA in harsh environments.

A panel discussion entitled “Computing and Communication Evolution for IoT Innovations” will be held on April 21st. We expect to see lively discussion among the panelists and audience.

On the first day, April 20th, we will hold two special invited lectures. The first will be presented by Prof. Jiang Xu of Hong Kong University of Science and Technology. He will talk about inter/intra-chip optical networks. The second will be presented by Prof. Kiyoung Choi of Seoul National University. He will talk about architectural approaches to using STT-RAM for low-power caches.

This year’s technical presentations in four sessions will cover recognition technologies, low power processing, memory, FPGA and software. The program committee accepted 11 oral presentations out of 22 papers submitted to suit the interests of the symposium audiences. The papers were submitted

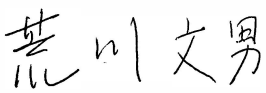
from around the world, namely, India, Korea, Taiwan, Germany, Italy, Malaysia, Egypt and Japan. Along with the technical presentations, a poster session is organized by Prof. Koji Hashimoto of Fukuoka University. 26 technical-posters are exhibited in the poster show room. The posters will have short presentations on April 21st.

Many people have contributed to the organization of COOL Chips XIX. We would like to express our sincere thanks to all the members of the Program Committee, Vice Program Chair, Prof. Yutaka Wada for the great deal of extra work he put into organizing this symposium. Prof. Koji Hashimoto, who acted as Poster chair, Prof. Tohru Ishihara, who acted as Special Session Chair, and all session chairs for their special contributions to this symposium. Moreover, on behalf of the program committee, we would like to greatly thank Prof. Hiroaki Kobayashi, the organizing committee chair, and all the people of the organizing committee, and Prof. Tadao Nakamura, the advisory committee chair, and all the people of the advisory committee for their great efforts in making the symposium possible.

Finally, we would like to thank the speakers of this symposium and all attendees. We hope you will enjoy the COOL Chips XIX.

Makoto Ikeda

Co-Chair of the Program Committee



Fumio Arakawa

Co-Chair of the Program Committee