Fault Injection in Native Logic-in-Memory Computation on Neuromorphic Hardware

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Abstract-Logic-in-memory (LIM) describes the execution of logic gates within memristive crossbar structures, promising to improve performance and energy efficiency. Utilizing only binary values, LIM particularly excels in accelerating binary neural networks, shifting it in the focus of edge applications. Considering ee its potential, the impact of faults on BNNs accelerated with LIM still lacks investigation. In this paper, we propose faulty logic-inmemory (FLIM), a fault injection platform capable of executing full-fledged BNNs on LIM while injecting in-field faults. The results show that FLIM runs a single MNIST picture $66754 \times$ faster than the state of the art by offering a fine-grained fault injection methodology.

Index memory Index Terms-ReRAM, memristor, faults, reliability, logic-in-

I. INTRODUCTION The von Neumann architecture describes a computing system consisting of two main distinct components: the memory and the computing unit. The computing unit must fetch/push from/to the memory in order to process data, representing the so-called von Neumann bottleneck. The bottleneck drastically limits conventional computing systems' performance and energy efficiency. Consequently, novel computing paradigms are being investigated to overcome this limitation [1]. Emerging non-volatile memories such as spin-torque-transfer memory (STT-RAM/MRAM), phase-change random-access memory (ReRAM) provide an ideal substrate for high-density memories by also enabling the computing-in-memory (CIM) paradigm. CIM executes operations within the memory without moving data to the processing unit. Implementing these operations in an analog fashion requires expensive ADCs/DACs but accomplishes the best performance [2]. In comparison, logic-inmemory (LIM) uses binary values to perform logic operations memory (LIM) uses binary values to perform logic operations within memory, omitting the conversion from the analog to the digital domain, while being more resilient against technologyspecific non-idealities [3], [4]. Fig. 1 exemplifies a memristive crossbar array executing parallel XNOR operations.

Binary neural networks (BNNs) represent a set of machine learning models that replace the typically used full-precision weights with binary values. These networks trade a lower overall accuracy with a significant performance improvement and a lower memory footprint. Due to the quantification of its



Fig. 1: Memristive crossbar array executing parallel XNOR operations.

internal layers, the inference is dominantly computed through the XNOR operation [5]. Hence, BNNs benefit from the massive parallelization of LIM, particularly in the context of edge applications.

However, the benefit of non-volatile memories for implementing these emerging applications depends on being able to guarantee reliability during their lifetime. In more detail, as observed in CMOS-based memories, these novel memories are susceptible to time-dependent deviations, causing in-field faults that affect their lifetime reliability [6], [7]. Time-dependent deviations are primarily a result of environmental variations, causing transient faults, such as bit-flips, and temporal variations, causing degradation over a lifetime. Furthermore, towards the end of their life cycle, memories encounter stuck-at faults.

The impact of transient faults has been thoroughly investigated for analog CIM [8]. Unfortunately, there is only limited work on the effect on LIM. X-Fault [9] describes the most detailed end-to-end fault injection platform injecting different traditional faults at the device level. However, this approach limits the platform's performance, dramatically lowering the feasibility of real-world models and datasets.

Contributions: In this paper, we propose an ultra-fast fault injection platform called FLIM, capable of simulating fullfledged BNN models. FLIM processes an MNIST data frame 66754× faster than X-Fault while injecting different faults related to time-dependent deviations. In detail, we present the following investigations. (1) First, we develop a simulation methodology that abstracts in-field faults toward a high-

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Fig. 2: Overview of the simulation methodology: (a) Noise vector generator and (b) fault injector.

performance fault model. (2) Second, we introduce a notion of time within our simulator, which allows the injection of faults per layer. (3) Finally, we perform a reliability assessment considering in-field faults of BNNs using different datasets and models.

The rest of the paper is organized as follows. Section II summarizes the state-of-the-art fault injection platforms, as well as the background related to BNNs and LIM. Section III, describes the simulation methodology, including the implemented fault models. Experimental results and a detailed discussion are presented in Section IV. Section V concludes the paper.

II. BACKGROUND

This section summarizes the main approaches proposed for performing reliability and security assessments, considering different types of faults that can affect these novel applications after manufacturing and during their lifetime. In addition, it describes the background of BNNs and LIM.

A. Related Work

Fault injection platforms allow for a hands-on investigation of the impact of faults on various aspects of computing systems. For instance, these platforms are heavily used to investigate hardware security primitives [10]-[12]. Especially analyzing faults in machine learning algorithms has become a vital field of research considering their widespread usage [13]-[15]. Non-idealities of emerging non-volatile memories and their impact on CIM have been thoroughly investigated [16], [17]. Chakraborty et al. [18] propose a general approach to model faults on memristive crossbars executing neural networks. The framework is capable of simulating linear and non-linear nonidealities at an architectural level. PytorX [19] presents an end-to-end neural network tool based on PyTorch. The tool adjusts the mapping and optimizes the training to overcome the effect of non-ideal crossbars, and drastically limits the impact of faults. In general, existing research has mainly focused on analog-based CIM. The only framework able to simulate LIM on memristive crossbar is presented by X-Fault [9]. The framework offers a wide range of features, including various fault models and injection mechanisms. However, the tool simulates faults on memristor level limiting performance significantly. Hence, X-Fault cannot simulate larger models or datasets due to performance issues. Consequently, we propose FLIM, which closes this gap and allows for an extensive investigation of faults on LIM-based machine learning algorithms.

B. Binary Neural Networks (BNNs)

BNNs represent a class of neural networks using aggressive quantization, drastically improving power efficiency but reducing accuracy [20]. This approach is auspicious for deploying deep neural networks to resource-constrained devices. Compared to full-precision neural networks, BNNs are behind in terms of accuracy. However, simple classification tasks achieve competitive performance. The open-source library Larg [21] offers an easy entry to build and train BNNs. The library builds upon Tensorflow and provides pre-trained models. An XNOR operation within BNNs replaces the matrix-matrixmultiplication of convolutions in full-precision neural networks. Thus, BNNs map directly to LIM on memristive crossbars and position it as a preferred application for CIM on edge. Since BNNs still require some non-binary computation (e.g., activation and integer bit-count), only convolutional and dense layers are mapped on memristive crossbar arrays. We follow X-Fault's conservative approach by assuming that these nonbinary operations are executed in CMOS.

C. Logic-in-Memory (LIM)

Compared to conventional CIM, LIM utilizes the memristive crossbar array in a binary fashion omitting expensive ADCs/DACS. Due to its binary working mode, LIM trades a higher error resilience with lower latency. Internally, logical states (0 or 1) are represented as either high or low resistive values of the memristive cell. Logic gates are composed of multiple memristors. An operation voltage applied to the connecting word line calculates the respective output based on the given inputs. Kvatinsky et al. [22] classified logic families into three categories: statefulness, the proximity of computation, and flexibility. MAGIC [22] and IMPLY [23] describe two stateful logic families capable of implementing a complete set of logic operations. Within the scope of this work, we abstracted the computation to the application level. Hence, we assume the underlying usage of a logic family implementing the XNOR logic gate without modeling it in detail.

III. FAULTY LOGIC-IN-MEMORY (FLIM)

FLIM embodies an end-to-end simulator capable of emulating the impact of faults on BNNs using binary memristive crossbar arrays. Fig. 2 depicts the internal structure of the fault injection platform, which consists of a *Fault Generator* and a *Fault Injector*. The *Fault Generator* constructs a set of fault vectors encoding the fault type, location, and injection rate. This



Fig. 3: Internal structure of FLIM consisting of the Fault Generator and the Fault Injector module.

tool is implemented in vanilla Python and hence, independent of the fault injection mechanism. The *Fault Injector* extends the Tensorflow/Larq framework to dynamically inject faults in arbitrary BNN models. As depicted in Fig. 2b, the *Fault Injector* employs the previously generated fault vectors and a defined dataset to initiate the inference procedure.

Fault masking: FLIM implements bit-flip and stuck-at faults to investigate the impact of time-dependent deviations. In contrast to X-Fault, the proposed platform models and injects faults on the XNOR operation level yielding enhanced simulation performance.

For bit-flip and stuck-at faults, a *fault mask* is generated, encoding the fault's location and binary representation. The bit-flip mask defines a 2-dimensional Boolean array initialized with zeros. The injection rate specifies the number of elements within the array set to 1. In addition to these randomly distributed bit-flips, entire rows/columns may also be faulty. Thus, these rows/columns are set to 1, respectively.

Furthermore, the platform supports *dynamic faults* which occur every n-th XNOR operation [24]. To model dynamic faults, the fault mask has to be repeated over several layers. Therefore, multiple bit-flip masks are assembled, which are consecutively applied to the respective layers of the model during inference. Likewise, the stuck-at mask follows the same structure by initializing a 2-dimensional array with zeros and marking all faulty elements with ones. In general, mask generation happens as an offline process that significantly improves performance because the expensive mapping and distribution of faults are performed once and reused over the whole simulation.

Fault mapping: The generated masks are assigned to specific layers within the BNN model in the next step. Therefore, the *Fault Generator* has to be provided with the dimensions and the number of crossbars used during the simulation. First, the mapping tool calculates the number of parallel XNOR operations based on the crossbars. Considering the implementation of MAGIC [22] or IMPLY [23], four memristors are required to facilitate one XNOR operation. Second, the model extracts the total number of required XNOR operations. Within a BNN, only the 2-dimensional convolution (conv2D) layer and fully binarized dense layers are dominantly using the XNOR operation. Consequently, these layers would be mapped and accelerated onto memristive crossbar arrays, while all remaining layers are executed on conventional CMOS. Hence, the mapping tool extracts the dimensions of these layers and assigns the previously generated fault masks.

Fault vector extraction: Finally, the required fault vectors are extracted from the virtual crossbar representation. The 2-dimensional arrays are flattened to 1 dimension. Furthermore, the vectors are stored in a binary file annotated with meta-information about the assigned layer and mask type. The binary file is independent of the dataset and reusable for a myriad of experiments.

Fault Injector: The *Fault Injector* represents the centerpiece of the FLIM platform. The tool is deeply integrated with the Larq and Tensorflow framework to aim for maximum performance by achieving a granular fault injection.

Fig. 3 depicts the internals of the injection mechanism. The Larq library generally extends the Keras framework to facilitate BNNs [21]. Larq defines custom quantized layers as an extension of Keras layers. We extended this layer base class by adding an instance of the Fault Injector. To trigger the injection mechanism during the inference, the original convolution method has been overwritten. The following describes the procedure of the faulty convolution method. First, the standard



Fig. 4: Simulation results: Impact of (a) bit-flips, (b) stuck-at, (c) dynamic faults, (d) faulty columns, and (e) faulty rows on different layers. (f) Performance benchmark.

convolution function calculates the feature map. The feature map does not yet take into account any faults and, therefore, represents the correct result of the computation. Second, before both fault masks are applied on the feature map, the vectors must be adjusted in length depending on the batch size and the input dimension. Finally, the fault masks are applied by performing another XNOR operation.

IV. RESULTS AND DISCUSSION

This section discusses the simulation results. Table I shows the system specifications used to conduct all experiments. We verified the functionality of FLIM in two distinct experiments. The fault injector extends the Tensorflow/Larq framework. Hence, we compared the inference results of FLIM (without injecting any faults) with the results of vanilla Tensorflow/Larq. The fault distribution and mapping have been verified with X-Fault. Our investigations exhibit the impact of faults on BNNs from various perspectives. First, the impact on individual layers is studied. Second, we compare the performance of our simulator to X-Fault and vanilla Tensorflow. Finally, we thoroughly explore the resilience of various models on bit-flip and stuck-at faults.

Layer resilience: This experiment aims to investigate the resilience of individual layers of a BNN. We use a binary version of LeNet [25] trained on the MNIST dataset. LeNet represents a convolutional neural network which, in this experiment, consists of three convolutional layers and two dense layers. The former aims to extract the visual features from

TABLE I: Adopted experimental setup.

Hardware				
CPU	AMD Ryzen 7 5800X			
RAM	DDR4 2666MHz 64GB			
GPU	NVIDIA GeForce RTX 3080 Ti 12GB			
Software				
GPU Driver	470.129.06			
CUDA	11.4			
CuDNN	8.1.0.77-1			
TensorFlow	2.8.0			
LARO	0.12.0 (modified)			

the input picture. The latter is responsible for the feature classification. The MNIST dataset embodies a set of 28×28 greyscale pixel images depicting handwritten digits [26]. After training, the model achieves an accuracy of 97.62% without any injected faults.

Throughout the experiment, each layer is mapped onto a single crossbar while sweeping the injection rate of bit-flips, dynamic faults, and stuck-at faults. To mitigate the impact of randomly placing the faults on the crossbar, we performed every experiment hundred times which reinitialized the random generator with a new seed value.

Fig. 4(a-b) illustrates that stuck-at faults impact the model more severely than bit-flips independent of the layer. While stuck-at faults influence almost all layers equally strongly, bitflip faults affect the accuracy depending on the layer depth. Moreover, convolutional layers appear more susceptible to bitflips than dense layers. The impact of dynamic bit-flip faults is



Fig. 5: Simulation results of (a) bit-flips, (b) stuck-at, and (c) dynamic faults on different models.

shown in Fig. 4(c), whereas the x-axis represents the number of XNOR operations required to sensitize the fault. The results show that the BNN model's accuracy stabilizes around its original value at around four consecutive XNOR operations.

Next, we investigate the impact of faulty rows/columns on the model's accuracy. This experiment instantiates a 40×10 crossbar for each layer. Fig. 4(d-e) portrays the results of this experiment. Once again, the layer's depth directly correlates with the impact on accuracy. In particular, the last dense layer declines almost linearly. In general, the impact of faulty columns is more substantial than of faulty rows. Considering the column-wise parallelism of XNOR operations, this result appears plausible.

Performance evaluation: We evaluate the performance of our fault injection platform by executing the inference on the previous LeNet model together with the complete MNIST test dataset consisting of 10.000 images. While FLIM and the vanilla Larq implementation perform fifty consecutive runs of the complete dataset, we estimate the total run time of X-Fault based on five images. During the inference, the fault injection mechanism maps the respective operations but does not inject actual faults. Thus, the vanilla Larq implementation serves as a lower boundary regarding the total simulation time.

Fig. 4(f) shows the substantial performance improvement of our work. *FLIM classifies the 10.000 images 29375 \times faster than X-Fault.*Due to the deep integration within Larq and Tensorflow, FLIM takes advantage of GPUs,*doubling the*

performance to a speed-up of 66754× compared to X-Fault. Conclusively, FLIM abstracts the fault model on the XNOR operation level and, hence, trades simulation accuracy with noteworthy performance improvement.

Model resilience: The last experiment investigates the resilience of various models (see Table II). We pre-trained the models with the ImageNet [27] dataset and injected bit-flips, dynamic, and stuck-at faults. Once again, we run every experiment hundred times to mitigate the impact of the randomly placed faults.

Fig. 5(a-c) displays the simulation results. As expected, the obtained results indicate that stuck-at faults cause a more substantial impact on the accuracy than bit-flips. In other words, it is possible to see that faults related to time-dependent deviations can affect the reliability of emerging applications differently. Depending on the injection rate, transient faults will compromise the reliability of such applications at different levels. In addition, it is possible to see that the reliability of emerging applications is more affected by permanent faults. The BiRealNet and XNOR-Net represent a particular case because their convolutions are not strictly binarized. BiReal-Net utilizes real-valued activation functions through identity shortcuts [28]. On the other hand, XNOR-Net's weights are multiplied by an individual gain based on the magnitude of the channel. Still, FLIM is capable of simulating both models by slightly adjusting the bit-flip mask.

TABLE II: Overview of the BNN models and their characteristics.

Model	Top-1 Acc.	Size	Parameters	MACs	Binarized
RealToBinaryNet [29]	65.0%	5.13MB	12M	1.81B	92.39%
BinaryDenseNet45 [30]	65.0%	7.54MB	13.9M	6.67B	96.34%
BinaryDenseNet37 [30]	62.9%	5.25MB	8.7M	4.71B	96.76%
BinaryDenseNet28 [30]	60.9%	4.12MB	5.13M	3.79B	94.66%
BinaryResNetE18 [31]	58.3%	4.03MB	11.7M	1.81B	92.4%
BinaryAlexNet [32]	36.3%	7.49MB	61.8M	841M	91.34%
MeliusNet22Z [33]	62.9%	3.88MB	6.94M	4.76B	97.14%
Bi-Real Net [28]	57.5%	4.03MB	11.7M	1.81B	92.4%
XNORNet [34]	45.0%	22.81MB	62.4M	1.14B	90.05%

V. CONCLUSION

This work proposed a fault injection platform, called FLIM, able to evaluate the impact of in-field faults related to timedependent deviations in emerging applications. The platform injects bit-flips (static and dynamic), related to environmental variations, and stuck-at faults, associated with temporal variations. We investigated the impact of these faults on individual layers and various models. Furthermore, FLIM outperforms the current state-of-the-art platform by four orders of magnitude in terms of performance. The obtained results show that a certain level of in-field faults can be tolerated and that the impact of bit-flips, even if multiple, compromises the reliability of emerging applications less than stuck-at faults. These results also demonstrate that in order to guarantee the development of high-reliability emerging applications, it is mandatory to adopt not only fault-tolerant approaches but also strategies able to monitor and/or mitigate applications' degradation during their lifetime. In the future, we want to extend the capabilities of FLIM to inject faults during training.

REFERENCES

- F. Staudigl *et al.*, "A survey of neuromorphic computing-in-memory: Architectures, simulators, and security," *IEEE Design & Test*, vol. 39, no. 2, pp. 90–99, apr 2022.
- A. Ankit et al., "PUMA," in Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems. ACM, apr 2019.
 P.-E. Gaillardon et al., "The programmable logic-in-memory (plim)
- [3] P.-E. Gaillardon et al., "The programmable logic-in-memory (plim) computer," in 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE), 2016, pp. 427–432.
- [4] G. Papandroulidakis *et al.*, "Crossbar-based memristive logic-in-memory architecture," *IEEE Transactions on Nanotechnology*, vol. 16, no. 3, pp. 491–501, may 2017.
- [5] H. Qin et al., "Binary neural networks: A survey," Pattern Recognition, vol. 105, p. 107281, 2020.
- [6] E. I. Vatajelu et al., "State of the art and challenges for test and reliability of emerging nonvolatile resistive memories," *International Journal of Circuit Theory and Applications*, vol. 46, no. 1, pp. 4–28, 2018.
- [7] W. Li et al., "Rramedy: Protecting reram-based neural network from permanent and soft faults during its lifetime," in 2019 IEEE 37th International Conference on Computer Design (ICCD). IEEE, 2019, pp. 91–99.
- [8] M. J. Rasch et al., "A flexible and fast PyTorch toolkit for simulating training and inference on analog crossbar arrays," in 2021 IEEE 3rd International Conference on Artificial Intelligence Circuits and Systems (AICAS). IEEE, jun 2021.
- [9] F. Staudigl et al., "X-fault: Impact of faults on binary neural networks in memristor-crossbar arrays with logic-in-memory computation," in 2022 IEEE 4th International Conference on Artificial Intelligence Circuits and Systems (AICAS). IEEE, jun 2022.

- [10] M. Gay *et al.*, "Hardware-oriented algebraic fault attack framework with multiple fault injection support," in 2019 Workshop on Fault Diagnosis and Tolerance in Cryptography (FDTC). IEEE, aug 2019.
- [11] F. F. dos Santos et al., "Revealing GPUs vulnerabilities by combining register-transfer and software-level fault injection," in 2021 51st Annual IEEE/IFIP International Conference on Dependable Systems and Networks (DSN). IEEE, jun 2021.
- [12] H. Wang et al., "SoFI: Security property-driven vulnerability assessments of ICs against fault-injection attacks," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 41, no. 3, pp. 452– 465, mar 2022.
- [13] J.-D. Guerrero-Balaguera et al., "Reliability assessment of neural networks in GPUs: A framework for permanent faults injections," in 2022 IEEE 31st International Symposium on Industrial Electronics (ISIE). IEEE, jun 2022.
- [14] T. Spyrou *et al.*, "Neuron fault tolerance in spiking neural networks," in 2021 Design, Automation & Test in Europe Conference & Exhibition (DATE). IEEE, feb 2021.
- [15] Y. Liu et al., "Fault injection attack on deep neural network," in 2017 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). IEEE, nov 2017.
- [16] S. Kannan et al., "Modeling, detection, and diagnosis of faults in multilevel memristor memories," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 34, no. 5, pp. 822–834, may 2015.
- [17] Y.-X. Chen et al., "Fault modeling and testing of 1t1r memristor memories," in 2015 IEEE 33rd VLSI Test Symposium (VTS). IEEE, apr 2015.
- [18] I. Chakraborty et al., "GENIEx: A generalized approach to emulating non-ideality in memristive xbars using neural networks," in 2020 57th ACM/IEEE Design Automation Conference (DAC). IEEE, jul 2020.
- [19] Z. He et al., "Noise injection adaption: End-to-end reram crossbar non-ideal effect adaption for neural network mapping," in 2019 56th ACM/IEEE Design Automation Conference (DAC), 2019, pp. 1–6.
- [20] H. Qin et al., "Binary neural networks: A survey," Pattern Recognition, vol. 105, p. 107281, 2020.
- [21] L. Geiger et al., "Larq: An open-source library for training binarized neural networks," *Journal of Open Source Software*, vol. 5, no. 45, p. 1746, 2020.
- [22] S. Kvatinsky et al., "MAGIC—memristor-aided logic," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 61, no. 11, pp. 895–899, nov 2014.
- [23] S. Kvatinsky et al., "Memristor-based material implication (IMPLY) logic: Design principles and methodologies," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 10, pp. 2054–2066, oct 2014.
- [24] K. M. Priya et al., "A survey on dram testing and its algorithms," International Journal of Computer Science Trends and Technology (IJCST), vol. 2, no. 5, pp. 1–3, 2014.
- [25] Y. LeCun et al., "Handwritten digit recognition with a back-propagation network," Advances in neural information processing systems, vol. 2, 1989.
- [26] Y. LeCun et al., "Gradient-based learning applied to document recognition," Proceedings of the IEEE, vol. 86, no. 11, pp. 2278–2324, 1998.
- [27] O. Russakovsky *et al.*, "Imagenet large scale visual recognition challenge," *International journal of computer vision*, vol. 115, no. 3, pp. 211–252, 2015.
- [28] Z. Liu et al., "Bi-real net: Binarizing deep network towards real-network performance," *International Journal of Computer Vision*, vol. 128, no. 1, pp. 202–219, 2020.
- [29] B. Martinez et al., "Training binary neural networks with real-to-binary convolutions," arXiv preprint arXiv:2003.11535, 2020.
- [30] J. Bethge et al., "Back to simplicity: How to train accurate bnns from scratch?" arXiv preprint arXiv:1906.08637, 2019.
- [31] K. He et al., "Deep residual learning for image recognition," in Proceedings of the IEEE conference on computer vision and pattern recognition, 2016, pp. 770–778.
- [32] A. Krizhevsky et al., "ImageNet classification with deep convolutional neural networks," *Communications of the ACM*, vol. 60, no. 6, pp. 84– 90, may 2017.
- [33] J. Bethge et al., "Meliusnet: An improved network architecture for binary neural networks," in Proceedings of the IEEE/CVF Winter Conference on Applications of Computer Vision, 2021, pp. 1439–1448.
- [34] M. Rastegari *et al.*, "Xnor-net: Imagenet classification using binary convolutional neural networks," in *European conference on computer vision*. Springer, 2016, pp. 525–542.