# Compact and High-Performance TCAM Based on Scaled Double-Gate FeFETs

Liu Liu<sup>†</sup>, Shubham Kumar<sup>\*‡</sup>, Simon Thomann<sup>\*</sup>, Yogesh Singh Chauhan<sup>‡</sup>, Hussam Amrouch<sup>§</sup>, and Xiaobo Sharon Hu<sup>†</sup>

<sup>†</sup>Department of Computer Science and Engineering, University of Notre Dame, USA,

\*Chair of Semiconductor Test and Reliability (STAR), University of Stuttgart, Germany

<sup>‡</sup>Department of Electrical Engineering, Indian Institute of Technology Kanpur, India

<sup>§</sup>Chair of AI Processor Design, Technical University of Munich (TUM), Germany

Email: {lliu24, shu}@nd.edu, amrouch@tum.de

Abstract-Ternary content addressable memory (TCAM), widely used in network routers and high-associativity caches, is gaining popularity in machine learning and data-analytic applications. Ferroelectric FETs (Fe-FETs) are a promising candidate for implementing TCAM owing to their high ON/OFF ratio, non-volatility, and CMOS compatibility. However, conventional single-gate FeFETs (SG-FeFETs) suffer from relatively high write voltage, low endurance, potential read disturbance, and face scaling challenges. Recently, a double-gate FeFET (DG-FeFET) has been proposed and outperforms SG-FeFETs in many aspects. This paper investigates TCAM design challenges specific to DG-FeFETs and introduces a novel 1.5T1Fe TCAM design based on DG-FeFETs. A 2-step search with early termination is employed to reduce the cell area and improve energy efficiency. A shared driver design is proposed to reduce the peripherals area. Detailed analysis and SPICE simulation show that the 1.5T1Fe DG-TCAM leads to superior search speed and energy efficiency. The 1.5T1Fe TCAM design can also be built with SG-FeFETs, which achieve search ( latency and energy improvement compared with 2FeFET TCAM.

## I. INTRODUCTION

**I. INTRODUCTION**Ternary content addressable memories (TCAMs) support fast par-allel search directly in the memory, which is a promising in-memory-computing (IMC) kernel to address the processor-memory bottle-neck [1]. Beyond conventional applications, such as network routers and associative caches, TCAMs have been used for a variety of data-centric applications, such as machine learning, neuromorphic computing, and bioinformatics [2]–[7].
The design space for content addressable memory (CAM) has been rapidly expanding in recent years largely due to the employ-ment of non-volatile memories (NVMs) in CAM design. Unlike the conventional CMOS TCAM with large area and high energy overhead, NVM-based TCAMs (NV-TCAMs) are more compact, energy-efficient, and non-volatile [8], which are more suitable for many emerging applications. A wide range of NV-TCAM designs have been proposed based on two-terminal NVMs, such as resistive RAM (RRAM) [6], [9], [10], phase change memory (PCM) [11], spin transfer torque magnetic RAM (STT-MRAM) [12], and three-terminal ferroelectric FETs (FeFETs) [13], [14]. The two-terminal NVM-based TCAMs typically require current-driven write schemes and large access transistors, leading to higher energy consumption. The low ON/OFF ratio of many two-terminal NVMs often requires more transistors in the CAM cell design, limits the word length of the TCAM array, and makes sensing more challenging [9], [11], [15]. The three-terminal FeFET is a promising candidate to implement NV-TCAMs for its high ON/OFF ratio, high OFF resistance, relatively low write energy, and CMOS compatibility [16]. Recent work proposed to use only two FeFETs to build an ultra-high density TCAM cell [13].

However, conventional FeFETs also face key challenges. (1) The thick ferroelectric (FE) layer ( $\sim 10$  nm) incurs severe charge trapping which limits the endurance, read throughput, and reliability of FeFET [17], [18]. (2) Although the electric field-driven write scheme of FeFETs is energy efficient, it requires  $\pm 4V$  write voltage to switch the state of the FE layer. The write voltage is higher than most standard

CMOS technologies hence posing challenges to the write drivers and high-voltage tolerance for other peripherals. For emerging applications with seldom writes and frequent searches, the write drivers stay idle most time but consume a large area and high leakage power. (3) Conventional FeFETs write and read the state from the same gate of a FeFET, which may lead to the read disturbance issue.

Recently, a double-gate FeFET (DG-FeFET) device has been proposed to mitigate the high write voltage and charge trapping concerns [17]. By reducing the FE thickness and using the separated front gate (FG) and back gate (BG) for write and read operation, respectively, DG-FeFETs only require 2V write/read voltage and facilitate technology scaling [19]. The separated write/read path avoids accumulated read disturbance presented in conventional FeFETs. The lower write voltage also helps to improve the endurance of the FeFET (>  $10^{10}$ ) [18]. Nevertheless, DG-FeFETs need BGs with separate control during read, resulting in area penalties. We refer to the conventional FeFETs as single-gate FeFETs (SG-FeFETs) to be differentiated from the emerging DG-FeFETs.

It comes naturally to consider implementing the 2FeFET TCAM design based on DG-FeFET. However, the 2 FeFETs per cell design magnifies the BG control overhead. This is also a common concern that NV-TCAM cells are typically implemented by two NVM devices with several transistors. In general, NVM devices are more expensive than CMOS transistors and increase the overhead of peripherals. Single NVM per TCAM cell design can be a possible solution.

This paper introduces a compact and high-performance TCAM design with only one FeFET per cell. Our contributions are below.

- We propose a 1.5T1Fe TCAM design using only one DG-FeFET per cell, which minimizes the BG control overhead and achieves fast parallel search. A two-step search with an early termination scheme is adopted to reduce the cell area and achieve superior energy efficiency. Simulation results show that our proposed 1.5T1DG-Fe TCAM design achieves  $4 \times / 1.21 \times / 1.21 \times$  write energy/search latency/search energy improvement compared to 2SG-FeFET TCAM, and  $1.83 \times / 3.79 \times$  cell area/search energy improvement compared to 16T CMOS TCAM. To the best of our knowledge, this is the first DG-FeFET-based CAM design.
- · We also build the widely-adopted 2FeFET TCAM based on DG-FeFET and find that the 2DG-FeFET TCAM cannot achieve competitive performance due to the DG-FeFET device limitation.
- We introduce a shared driver design across the TCAM subarrays through device-circuit co-optimization to reduce driver area and improve driver utilization.
- The proposed 1.5T1Fe TCAM design can also be implemented by SG-FeFET and achieve  $2 \times / 1.66 \times / 1.42 \times$  write energy/search latency/search energy improvement compared to 2SG-FeFET TCAM, and  $2.12 \times 4.42 \times$  cell area and search energy improvement compared to CMOS TCAM.



Fig. 1: Schematic representation of FDSOI FeFET with (a) Single-gate and (b) Double-gate. Arrows in the channel region show the formation of the channel due to reading voltage at the front and back gates. I-V characteristic of (c) FG read FeFET with write voltage  $V_w = \pm 4V$  and MW = 1.8V and (d) BG read FeFET with  $V_w = \pm 2V$  and MW = 2.7V.

# **II. PRELIMINARIES**

# A. Single-Gate & Double-Gate FeFET

A FeFET is composed of a FE layer integrated into the gate stack of a MOSFET. The coupling effect of FE capacitance and MOSFET gate capacitance exhibits a tunable hysteresis leading to the non-volatile feature. By applying a positive/negative voltage on the FG, the FE layer is polarized to place the underlying transistor in either the low- $V_{\rm TH}$  (LVT) or high- $V_{\rm TH}$  (HVT) state.

As the memory window (MW) is proportional to the FE thickness  $(t_{FE})$ , conventional SG-FeFETs need a thick FE layer (10nm) to achieve the required memory window (MW) [19], [20]. However, the thick FE layer leads to severe charge trapping and requires a relatively high write voltage (+/-4V), which also hinders the technology scaling. Besides, as shown in Fig. 1(a), the write and read operations of SG-FeFET shares the common FG, hence frequent read operations can alter the polarization state causing accumulated read disturbance.

Recently, a double-gate FeFET structure is proposed to address the aforementioned issues [21]. The device structure of DG-FeFET is similar to SG-FeFET except for the employment of BG, as shown in Fig. 1(b). For the SG-FeFET, the back side is the body bias (BB) and is not applied to write or read pulse. For the DG-FeFET, the write pulse and read pulse are applied to FG and BG separately, which can efficiently avoid the accumulated read disturbance. Additionally, the BG read scheme amplifies the MW of the DG-FeFET, as the comparison between in Fig. 1(c) and Fig. 1(d). A 3nm  $t_{FE}$  is sufficient to achieve MW of 2.7V [19], [21]. Therefore, write voltage can be significantly reduced and endurance can be improved to  $10^{10}$  level [18]. A compact SPICE model for DG-FeFET is recently presented and is well calibrated with TCAD simulation results [22].

However, two aspects need to be carefully considered for the DG-FeFET-based design. First, to support individual control for BG, isolated P-wells are required, resulting in area penalties. Second, though the BG read scheme can amplify the MW, it reduces the sub-threshold slope (SS) of DG-FeFET, as shown in Fig. 1(d). In this case, the ON current of DG-FeFET is more sensitive to bias change.



Fig. 2: The architecture of a general  $M \times N$  NOR-type CAM array.

# B. Existing TCAM Designs

TCAM is the most widely used CAM type since TCAMs provide an additional 'don't care' state ('X' state) to allow a wildcard operation in addition to the '0' and '1' states offered in the binary CAM (BCAM). Conventional CMOS TCAM designs require 10-16 transistors per cell, thus the high energy and area costs limit their applications. NV-TCAMs are typically implemented by two NVM devices to encode '0' and '1' states using high and low resistance states with several control transistors, which are more compact and energy efficient. A 2T-2R compact TCAM structure is proposed based on either PCM [11] or RRAM [6]. A 2FeFET TCAM design is proposed to achieve an ultra-dense TCAM cell without any control transistors, which is the most widely-adopted FeFET TCAM design [2], [5], [7], [13] (see Fig. 3(b)). The NV-TCAM designs based on two-terminal NVMs usually require current-driven write schemes and have a large leakage current for search. The low ON/OFF ratio and capacitance from the large access transistors also limit the search speed and word length of the CAM array. Conventional SG-FeFETs seem to be free from the issues of two-terminal NVMs, but the write voltage (+/-4V) is higher than most standard CMOS technologies hence posing challenges to the write drivers and high-voltage tolerance for other peripherals.

Besides, two NVMs per cell design is also relatively expensive and increases the overhead of peripherals, which is not only reflected in the cell-level metrics, it also impacts the array-level performance. Some NV-CAM designs are proposed to implement a TCAM cell with only one NVM device. A 3T1R RRAM TCAM [10] and a similar 2.5T1R RRAM TCAM [9] are proposed based on the voltage-divider concept, but they require complex control signals and additional access transistors. Recent work proposed a 2T1Fe CAM design, but it is only a BCAM design that cannot support a 'don't care' state [23]. A 3T1Fe multi-bit CAM design is proposed, but the sensing circuit and control signals are complex [24]. In a TCAM array, an input query is compared against all the stored entries in parallel and the address of the matched entry is returned. As shown in Fig. 2, in a CAM array, match lines (MLs) are shared by the CAM cells in a row and sensed by the sense amplifier (SA). For a search operation, MLs are first precharged, and then the input query is applied to the search lines (SLs). If the corresponding ML discharges to 0, indicating a mismatch; otherwise, ML stays high, indicating a match.

# III. DG-FEFET-BASED TCAM DESIGN

In this section, we first discuss 2DG-FeFET TCAM design and point out its unique challenges. We then present our 1.5T1DG-Fe TCAM design and the shared driver architecture.

## A. 2DG-FeFET TCAM

Fig. 3(b) depicts the 2DG-FeFET TCAM design. The operations of 2DG-FeFET TCAM are summarized in Tab. I. the bit lines (BLs) for



Fig. 3: The schematic comparison of  $2 \times 2$  (a) 2DG-FeFET and (b) 2SG-FeFET TCAM. TABLE I

Operations of 2DG-FeFET TCAM Cell

Operation	State	BL	BL	SL	$\overline{SL}$	2FeFET states
Write	0	-V <sub>w</sub>	$+V_w$	0	0	HVT / LVT
	1	$+V_w$	$-V_w$	0	0	LVT / HVT
	Х	$-V_{w}$	$-V_{w}$	0	0	HVT / HVT
Search	0	0	0	Vs	0	
	1	0	0	0	$V_s$	-
$V_{\rm ev} = 2V$ : $V_{\rm e} = 2V$						

the write operation and SLs for the search operation are separated and connected to the FG and BG of DG-FeFET, respectively. The 2DG-FeFET TCAM design inherits the advantages of DG-FeFET but also faces the corresponding challenges. First, for a  $M \times N$  TCAM array, 2N column-wise P-wells are required to accommodate the dedicated SLs for the 2N FeFETs in each column, which can be substantially expensive. Second, due to the reduced SS of the DG-FeFET, the search latency of 2DG-FeFET TCAM is longer than its SG-FeFET counterpart. Therefore, the straightforward 2DG-FeFET TCAM design may not be an ideal choice.

### B. 1.5T1DG-Fe TCAM

1) **1.5TIDG-Fe TCAM Overview:** To address the issues of the 2DG-FeFET TCAM design, we propose a 1.5T1DG-Fe TCAM design that only uses a single FeFET in a TCAM cell, as shown in Fig. 5(a). Based on the voltage-divider scheme, we use the HVT, LVT, and medium- $V_{TH}$  (MVT) of a DG-FeFET to encode the ternary states of TCAM. To reduce the cell area, every two DG-FeFETs are grouped in a 2-cell pair and adopt a two-step search to share the control transistors TP, TN, and TML. TML, a small NMOS transistor, is connected to the ML for every two TCAM cells, which reduces the search latency and ML precharge energy. The DG-FeFET devices do not directly participate in the ML discharge process, hence the impact of reduced SS is mitigated. Compared with the 2DG-FeFET TCAM design, for every two TCAM cells, the direct capacitance load on the ML reduces from 4 large DG-FeFET devices to 1 small NMOS transistor, leading to a shorter ML delay.

2) TCAM Cell Operation: The operations of the 1.5T1DG-Fe TCAM design are shown in Tab. II. During the write operation, to keep the source, drain, and BG of the DG-FeFET to the ground level, the Wr/SL is set to  $V_{DD}$ , and SL and SeL are set to 0. The write voltage is applied on the BL to program the DG-FeFET state. Besides the '0' (HVT,  $R_{OFF}$ ) and '1' state (LVT,  $R_{ON}$ ), an 'X' state is required, and the corresponding DG-FeFET resistance  $R_M$  is between  $R_{OFF}$  and  $R_{ON}$ . The array-level write scheme will be discussed in Sec. III-B3.

During the search operation, TCAM  $cell_1$  and  $cell_2$  are searched in two steps. Select signals  $SeL_a$  and  $SeL_b$  are connected to the BG of  $cell_1$  and  $cell_2$ , respectively. The select voltage  $V_{SeL}$  equals the BG

TABLE II Operations of 1.5T1DG-Fe TCAM Cell

Operation	State	BL	SeL	Wr/SL	SL	FeFET state
	0	$-V_{w}$	0	V <sub>DD</sub>	0	HVT (R <sub>OFF</sub> )
Write	1	$+V_w$	0	$V_{DD}$	0	LVT (R <sub>ON</sub> )
	Х	$V_{m}$	0	$V_{DD}$	0	$MVT (R_M)$
Search	0	V <sub>b</sub>	V <sub>SeL</sub>	V <sub>DD</sub>	V <sub>DD</sub>	
	1	0	V <sub>SeL</sub>	0	0	-

 $V_w = 2V; V_m = 1.6V; V_{SeL} = 2V; V_{DD} = 0.8V; V_b = 0.25V.$ 



Fig. 4: The transient waveform of (a) select signals  $SeL_a$  and  $SeL_b$ , and (b) ML and (c) SA output of step-1 miss, step-2 miss, and match cases.

read voltage of the DG-FeFET. Cell<sub>1</sub> is searched in the first step (SeL<sub>a</sub> =  $V_{SeL}$ , SeL<sub>b</sub> = 0), and cell<sub>2</sub> is searched in the second step (SeL<sub>a</sub> = 0, SeL<sub>b</sub> =  $V_{SeL}$ ). We use cell<sub>1</sub> as an example to explain the way to apply the search query, and cell<sub>2</sub> follows the same process.

To ensure the correct operation of the TCAM, the resistance values of TN, TP, and DG-FeFET must be carefully selected. Specifically, The ON resistance of TP ( $R_P$ ), TN ( $R_N$ ) and the DG-FeFET resistance of '0' ( $R_{FE} = R_{OFF}$ ), '1' ( $R_{FE} = R_{ON}$ ), and 'X' ( $R_{FE} = R_M$ ) states should satisfy:

$$\mathbf{R}_{ON} < \mathbf{R}_{N} < \mathbf{R}_{M} < \mathbf{R}_{P} \ll \mathbf{R}_{OFF}$$
(1)

When searching for '0',  $V_{DD}$  is applied to Wr/SL and SL, thus TN is turned on and the equivalent circuit is shown in Fig. 5(b). The voltage of SL\_bar can be estimated as

$$V_{SL\_bar} = \frac{V_{DD} \times R_N}{R_{FE} + R_N}$$
(2)

If the stored value is '0' ( $R_{FE} = R_{OFF}$ ),  $R_{FE}$  is much larger than  $R_N$ , which keeps the voltage of SL\_bar ( $V_{SL_bar}$ ) smaller than the threshold voltage of TML ( $V_{TH}$ ). TML is turned off and the ML stays high, resulting in a match. If the stored value is '1' ( $R_{FE} = R_{ON}$ ),  $R_{FE}$  is smaller than  $R_N$ , and  $V_{SL_bar}$  is higher than  $V_{TH}$ . TML is turned on and the ML discharges through TML, resulting in a mismatch. To keep the  $R_{ON}$  relatively constant when connecting in series with  $R_N$ , a small bias ( $V_b$ ) is applied to the BL to provide better FG to source voltage potential of DG-FeFET.

When searching for '1', Wr/SL and SL are connected to the ground, thus TP is turned on and the equivalent circuit is shown in Fig. 5(c). The voltage of SL\_bar can be estimated as

$$V_{SL\_bar} = \frac{V_{DD} \times R_{FE}}{R_{FE} + R_P}$$
(3)

Similarly, if the stored value is '0' ( $R_{FE} = R_{OFF}$ ),  $R_{FE}$  is much larger than  $R_P$ , which makes  $V_{SL\_bar}$  higher than  $V_{TH}$ . TML is turned on and



Fig. 5: (a) The proposed 1.5T1DG-Fe TCAM in 2-cell pair. (b) The equivalent circuit of searching '0' and searching '1'. The  $2 \times 4$  (c) 1.5T1DG-Fe TCAM array and (d) 1.5T1SG-Fe TCAM array.

the ML discharges, resulting in a mismatch. If the store value is '1' ( $R_{FE} = R_{ON}$ ),  $R_{FE}$  is smaller than  $R_P$ , hence  $V_{SL\_bar}$  is lower than the  $V_{TH}$  of TML. TML is turned off and the ML stays high, resulting in a match. For the TCAM cell storing the 'X' state, the corresponding  $R_M$  is between  $R_N$  and  $R_P$ , hence regardless of searching '0' or '1',  $V_{SL\_bar}$  is always below  $V_{TH}$ , and TML is always turned off, achieving the 'don't care' function.

3) TCAM Array & Early Search Termination: A  $2\times4$  array of the proposed 1.5T1DG-Fe TCAM is shown in Fig. 5(c). Signals Wrs/SLs, BLs, and SLs are shared column-wise, and SeL<sub>a</sub>, SeL<sub>b</sub>, and MLs are shared row-wise. Since the search controls (i.e., SeL<sub>a</sub>/SeL<sub>b</sub>) are connected row-wise in our 1.5T1DG-Fe TCAM design, 2*M* separated P-wells are required for a  $M \times N$  TCAM array. Compared to the 2*N* P-wells required by the 2DG-FeFET design, though the number of P-wells is comparable if *M* and *N* are similar, the total number of DG-FeFETs in the TCAM array is reduced by half.

We should point out that our proposed 1.5T1DG-Fe TCAM uses three  $V_{\text{TH}}$  levels hence three-step write is required. Though one more write step than the 2FeFET TCAM design is needed to write the 'X' state, write is much less frequent than search. Other NV-TCAM designs based on single NVMs have similar 3-step write schemes [9], [10].

At the array level, a two-step search with early termination is adopted for the 1.5T1DG-Fe TCAM, as shown in Fig. 4. In the first step, the search query is applied to search all the cell<sub>1</sub>s (SeL<sub>a</sub> =  $V_{SeL}$ ) in the 2-cell pair, as shown in Fig. 4(a). If no mismatch exists and the ML stays high, then we search all the cell<sub>2</sub>s in the second step  $(SeL_b = V_{SeL})$ . If both two steps find no mismatch, ML stays high, and SA outputs '1', indicating a match for the entry (match case in Fig. 4(b) and (c)); otherwise, ML discharges to the ground and SA outputs '0', indicating a mismatch (step-2 miss case in Fig. 4(b) and (c)). If the stored entries are mismatched in the first step, the search operation terminates, then ML discharges to the ground and SA outputs '0', indicating a mismatch (step-1 miss case in Fig. 4(b) and (c)). The SeL<sub>b</sub> signal (green dot line in Fig. 7) is grounded and will not apply V<sub>SeL</sub>. In this case, the DG-FeFET is in the OFF state, hence the leakage current going through the voltage divider structure can be reduced (see Fig. 5(b)), leading to search energy savings. In real-world applications, most of the stored entries return mismatches. Therefore, the energy saving from the early termination is significant. In addition, regardless of the match results of the first and second steps, the ML



Fig. 6: (a) The shared HV drivers architecture between the adjacent TCAM subarrays, and (b) the schematic of a shared HV driver.

## is precharged once, further improving energy efficiency.

4) **High Voltage Driver Optimization**: If the search and write voltage of an NV-TCAM is the same, they would be able to share the same driver, which can save not only the area but also increase the driver utilization and reduce the leakage power.

Toward this end, we have explored the DG-FeFET design space and identified a delicately optimized combination of device parameters like gate work-function tuning such that the LVT write voltage and read voltage of the DG-FeFET are the same voltage level (2.0V) and the resulting Id-Vg curve is shown in Fig.1(d). The DG-FeFET can achieve 2.7V MW and  $10^4$  level ON/OFF ratio.

Given that the search and LVT programming share the same voltage level, we design a specific driver-sharing scheme for the 1.5T1DG-Fe TCAM design, shown in Fig. 6(a). The shared drivers drive the BLs in the write operation and drive the SeLs in the search operation. Since the BLs and SeLs are placed perpendicularly in each subarray and they are not employed at the same time, we share the HV driver between adjacent subarrays in a time-multiplexed manner. The adjacent subarray is rotated by 90° and four subarrays compose a mat. The number of drivers is cut in half, which not only reduces the driver area but also increases driver utilization. The schematic of a shared HV driver is shown in Fig. 6(b), and the driver connection is controlled by the write/search enabled signal.

# IV. 1.5T1SG-FE TCAM

The proposed 1.5T1DG-Fe TCAM design can also be adapted to using SG-FeFETs. Compared with 1.5T1DG-Fe TCAM, the select

Write 	0 1 X 0	-V <sub>w</sub> +V <sub>w</sub> V <sub>m</sub>	V <sub>DD</sub> V <sub>DD</sub> V <sub>DD</sub>	0 0 0	HVT (R <sub>OFF</sub> ) LVT (R <sub>ON</sub> ) MVT (R <sub>M</sub> )
Write 	1 X 0	+V <sub>w</sub> V <sub>m</sub>	V <sub>DD</sub> V <sub>DD</sub>	0 0	LVT (R <sub>ON</sub> ) MVT (R <sub>M</sub> )
Search	X 0	V <sub>m</sub>	V <sub>DD</sub>	0	MVT (R <sub>M</sub> )
Search	0	V	17	17	
Search	-	▼ SeL	V DD	V <sub>DD</sub>	
Sturth	1	V <sub>SeL</sub>	0	0	-
$V_{w} = 4V; V_{m}$ (a)	= 3.2	V; V <sub>SeL</sub> =0.	8V; V <sub>DD</sub> =	=0.8V.	
0.40 					

TABLE III



128

0.20 40.20 Search S 0.15

0.10

16

32

128

64 Word Length (bit)

signal and write signal (BL/SeL) are merged and connected to the FG of SG-FeFET, as shown in Fig. 5(d). The operations are summarized in Tab. III. The 1.5T1SG-Fe TCAM design has a smaller cell area compared with the DG-FeFET-based counterpart because the SG-FeFET-based design does not require individual BG control.

# V. EVALUATION

## A. Simulation Setup

32

Word Length (bit)

64

Search Latency 2000

150

100

50

To evaluate our proposed 1.5T1Fe TCAM and benchmark with 2FeFET TCAM design, we have performed extensive SPICE simulations. A 14nm BSIM-IMG model is calibrated with the experimental data [26] and is used for the MOSFETs modeling. To ensure a fair comparison, we use the 14nm FDSOI SG-FeFET and DG-FeFET models based on the same 14nm BSIM-IMG model and are calibrated with TCAD simulation results [22]. The device size of SG-FeFETs and DG-FeFETs is  $20 \times 50$  nm. The FE layer thickness of SG-FeFET and DG-FeFET is 10nm and 5nm, respectively. The wire parasitics are extracted from Eva-CAM [15].

## B. TCAM Array Evaluation

Tab. IV compares the figures-of-merit (FoM) of four FeFET TCAM designs with standard 16T CMOS TCAM designs. We comprehensively evaluate the four designs from both FeFET devices and CAM cell circuits aspects. The FoM includes write voltage, FE thickness of FeFET, TCAM cell area, write energy per cell, search latency, and search energy per cell. The data of the four designs are obtained from the simulation results of a 64×64 TCAM array size. A 16T CMOS TCAM design implemented in 14nm SOI technology with 64-bit word length is also included to fairly compare with mature TCAM technology [25]. The FoM of 2SG-FeFET design has been extensively compared with other NV-TCAM designs [13], [14], [23], hence here we mainly focus on the FeFET TCAM evaluation and set the 16T CMOS design as the baseline. For the DG-FeFET-based design, the write voltage is reduced to +/-2V, which is only half of the SG-FeFET-based design. The reduced write voltage can not only improve the endurance but also lead to greater advantages from the peripherals that may not be fully reflected in cell-level metrics.

The TCAM cell areas are estimated by their layouts based on [27]. We consider the large spacing between different P-wells in our estimation. Due to the separated P-wells for BG control, the cell area of the DG-FeFET-based design is larger than the SG-FeFET-based counterpart. Besides, to achieve ideal resistance relations presented in equation (1), relatively large TP and TN transistors are required for the 1.5T1Fe TCAM design, so the cell area of our proposed 1.5T1SG-Fe and 1.5T1DG-Fe designs are larger than the 2SG-FeFET designs. But the cell areas of all four FeFET TCAM designs are smaller than 16T CMOS TCAM in the same 14nm technology node. The 2FeFET design encodes TCAM states using HVT and LVT of 2 FeFETs in a complimentary manner, so the write energy per cell does not depend on the stored state of TCAM. Our proposed 1.5T1Fe design only uses one FeFET to store the TCAM state, hence stored data impacts the write energy evaluation. To do a fair comparison, we evaluate the average case that half of the 1.5T1DG-Fe cells are programmed to '0' and half of the cells are programmed to '1'. DG-FeFET designs have lower write energy than their SG-FeFET counterpart for their lower write voltage. In addition, due to the single FeFET-based design, the write energy per cell of 1.5T1Fe TCAM is reduced to half of the 2FeFET design. As a result, the implemented 2DG-FeFET, 1.5T1SG-Fe, and 1.5T1DG-Fe designs achieve  $2\times$ ,  $2\times$ , and  $4\times$  write energy compared to the 2SG-FeFET design, respectively. The search latency is impacted by the total capacitance and resistance on the ML. We consider the worst-case latency of one-cell mismatch. For the proposed 1.5T1Fe TCAM design, every two cells only have a minimum size NMOS transistor connected to the ML, thus the search latency is reduced significantly. We include the latency of the two-step search and leave some time slack for the search signal switching between the two steps. The 1.5T1SG-Fe and 1.5T1DG-Fe TCAM designs achieve 1.66× and 1.21× search latency improvement compared with the 2SG-FeFET design. The search latency of the 1.5T1DG-Fe design is slightly slower than the 1.5T1SG-Fe design, because of the higher ON resistance of DG-FeFET. For the store '1' search '0' case, as discussed in Sec. III-B2, the TML is not fully turned on hence limiting the ML discharge speed. The 2DG-FeFET design search latency is longer than the 2SG-FeFET design for a similar reason. The 16T CMOS search latency from simulated results [25] is shorter than our 1.5T1Fe TCAM design, which may be due to CMOS TCAM using the minimum channel size to achieve a faster switch in the advanced technology node.

The search energy of the TCAM cell mainly consists of the ML precharge, SA, and the search signals energy consumption. For the 2FeFET design, the ML precharge and SA energy consume the majority of the search energy. For the 1.5T1Fe TCAM design, the ML precharge energy is smaller than the 2FeFET design, but the voltage divider structure produces a non-negligible current during the search operation, especially for the FeFETs in LVT states ( $R_{FE}$  = R<sub>ON</sub>), leading to higher energy consumption for the search signals. We evaluate the average case in that half of the cells store '0' and half of the cells store '1'. Additionally, the early search termination scheme helps to save considerable search energy. We report both the single-step search energy and the total two-step search energy in Tab. IV. In real-world applications, typically more than 95% stored entries return mismatches in the first step but this depends on the search pattern [9]. Here we assume 90% 1-step mismatch rates for a pessimistic estimation and calculate the average search energy per cell. The proposed 1.5T1SG-Fe and 1.5T1DG-Fe TCAM designs achieve  $1.42 \times / 1.21 \times$  and  $4.42 \times / 3.79 \times$  search energy improvement compared to the 2SG-FeFET and 16T CMOS design, respectively. Due to the longer sensing time of the 2DG-FeFET and 1.5T1DG-Fe designs, their search energy is higher than the SG-FeFET counterpart.

TABLE IV FoM comparison of CMOS and FeFET TCAM designs

FoM	16T CMOS† [25]	2SG-FeFET	2DG-FeFET	1.5T1SG-Fe	1.5T1DG-Fe
Write voltage	0.9V	$\pm 4V$	$\pm 2V$	±4V, 3.2V	±2V, 1.6V
FE thickness	N.A.	10nm	5nm	10nm	5nm
Cell area $(um^2)$	0.286 (1×)	0.095 (3.01×)	$0.204~(1.40\times)$	$0.108~(2.65 \times)$	0.156 (1.83×)
Write energy/cell (fJ)	N.A.	1.63 (1×)	$0.81(2 \times)$	0.82 (2×)	$0.41~(4 \times)$
Search Latency (ps)	235 (1×)	582 (0.4×)	1147 (3.01×)	1 step: 159 2 steps: 351 (0.67×)	1 step: 231 2 steps: 481 (0.49×)
Search Energy/cell (fJ)	0.53 (1×)	0.17 (3.12×)	0.25 (2.12×)	1 step: 0.11 2 steps: 0.16 Average*: 0.12 (4.42×)	1 step: 0.13 2 steps: 0.21 Average*: 0.14 (3.79×)

\* The average search energy consumption per cell in real-world applications, assuming 90% step-1 miss rate.

† The 16T CMOS TCAM is implemented in 14nm SOI technology with 64-bit word length, and data is from simulated results.

## C. Design Space Exploration

Fig. 7(a) and (b) show the word length impact on the search latency and energy of the four SG-FeFET and DG-FeFET TCAM designs. The search latency and energy evaluation methods are consistent with Sec. V-B. As the word length increases, the associated ML capacitance increase, hence the search latency of the four TCAM designs increases accordingly. But the latency increase trends of the 1.5T1Fe design are slower than the 2FeFET design, which shows better performance scalability. The search energy per cell shows different trends of the 2FeFET and 1.5T1Fe TCAM designs. For the 2FeFET design, the search energy per cell decreases with word length increases, because the increased number of CAM cells per word amortizes the energy consumption of the SA. However, for the 1.5T1Fe TCAM designs, as the word length increases, the search latency increases, hence the voltage divider structure dominates the total energy consumption, which suppresses the energy amortization effects of SA.

## CONCLUSION

This paper introduces a novel 1.5T1Fe TCAM design based on DG-FeFETs that employs only one DG-FeFET per TCAM cell. We systematically analyze the advantages and challenges of DG-FeFETs design. The 1.5T1DG-Fe TCAM design alleviates the BG control overhead and achieves fast parallel search with high energy efficiency. A search early termination scheme is proposed to further reduce the search energy. A shared driver design is presented with device-circuit co-optimization to reduce the peripherals overhead. The proposed 1.5T1Fe TCAM can also be implemented by conventional SG-FeFET achieving superior search speed and energy efficiency compared to 2SG-FeFET.

## ACKNOWLEDGEMENT

This research was supported in part by the Semiconductor Research Corporation (SRC) Logic and Memory Devices Program (LMD), and by AI Chip Center for Emerging Smart Systems (ACCESS) sponsored by InnoHK funding, Hong Kong SAR.

#### REFERENCES

- [1] X. S. Hu *et al.*, "In-memory computing with associative memories: A cross-layer perspective," in *IEDM*, 2021, pp. 25.2.1–25.2.4.
- [2] A. F. Laguna *et al.*, "Seed-and-vote based in-memory accelerator for dna read mapping," in *ICCAD*, 2020.
  [3] L. Liu *et al.*, "A reconfigurable fefet content addressable memory for
- [3] L. Liu *et al.*, "A reconfigurable fefet content addressable memory for multi-state hamming distance," *IEEE TCAS-1*, pp. 1–14, 2023.
  [4] G. Pedretti *et al.*, "Tree-based machine learning performed in-memory
- [4] G. Pedretti *et al.*, "Tree-based machine learning performed in-memory with memristive analog CAM," *Nature Communication*, vol. 12, no. 1, pp. 1–10, Oct. 2021.
- [5] K. Ni *et al.*, "Ferroelectric ternary content-addressable memory for one-shot learning," *Nature Electronics*, vol. 2, no. 11, pp. 521–529, Nov. 2019.
  [6] H. Li *et al.*, "Sapiens: A 64-kb rram-based non-volatile associative
- [6] H. Li *et al.*, "Sapiens: A 64-kb rram-based non-volatile associative memory for one-shot learning and inference at the edge," *IEEE TED*, vol. 68, no. 12, pp. 6637–6643, 2021.

- [7] M. Imani *et al.*, "Searchd: A memory-centric hyperdimensional computing with stochastic training," *IEEE TCAD*, vol. 39, no. 10, pp. 2422–2433, 2020.
- [8] R. Karam *et al.*, "Emerging trends in design and applications of memorybased computing and content-addressable memories," *Proceedings of the IEEE*, vol. 103, no. 8, pp. 1311–1330, 2015.
- [9] C.-C. Lin et al., "7.4 a 256b-wordlength reram-based tcam with 1ns search-time and 14x improvement in wordlength-energyefficiency-density product using 2.5t1r cell," in *ISSCC*, 2016, pp. 136–137.
- [10] M.-F. Chang *et al.*, "17.5 a 3t1r nonvolatile tcam using mlc reram with sub-1ns search time," in *ISSCC*, 2015, pp. 1–3.
- [11] J. Li *et al.*, "1 mb 0.41 μm<sup>2</sup> 2t-2r cell nonvolatile tcam with two-bit encoding and clocked self-referenced sensing," *IEEE JSSC*, vol. 49, no. 4, pp. 896–907, 2014.
- [12] C. Wang *et al.*, "Design of magnetic non-volatile tcam with prioritydecision in memory technology for high speed, low power, and high reliability," *IEEE TCASI*, vol. 67, no. 2, pp. 464–474, 2020.
- [13] X. Yin *et al.*, "An ultra-dense 2fefet tcam design based on a multi-domain fefet model," *IEEE TCASII*, vol. 66, no. 9, pp. 1577–1581, 2019.
- [14] Y. Qian *et al.*, "Energy-aware designs of ferroelectric ternary content addressable memory," in *DATE*, 2021, pp. 1090–1095.
- [15] L. Liu *et al.*, "Eva-cam: A circuit/architecture-level evaluation tool for general content addressable memories," in *DATE*, 2022, pp. 1173–1176.
- [16] M. Trentzsch *et al.*, "A 28nm hkmg super low power embedded nvm technology based on ferroelectric fets," in *IEDM*, 2016, pp. 11.5.1–11.5.4.
   [17] Z. Jiang *et al.*, "Asymmetric double-gate ferroelectric fet to decouple the
- [17] Z. Jiang *et al.*, "Asymmetric double-gate ferroelectric fet to decouple the tradeoff between thickness scaling and memory window," in *VLSI*, 2022, pp. 395–396.
- [18] A. J. Tan *et al.*, "Ferroelectric hfo<sub>2</sub> memory transistors with high-κ interfacial layer and write endurance exceeding 10<sup>10</sup> cycles," *IEEE EDL*, vol. 42, no. 7, pp. 994–997, 2021.
- [19] S. Chatterjee *et al.*, "Comprehensive variability analysis in dual-port fefet for reliable multi-level-cell storage," *IEEE TED*, vol. 69, no. 9, pp. 5316– 5323, 2022.
- [20] S. Kumar et al., "Cross-layer fefet reliability modeling for robust hyperdimensional computing," in *IFIP/IEEE VLSI-SoC*, 2022, pp. 1–6.
- [21] H. Mulaosmanovic *et al.*, "Ferroelectric transistors with asymmetric double gate for memory window exceeding 12 v and disturb-free read," *Nanoscale*, vol. 13, no. 38, pp. 16258–16266, 2021.
- [22] S. Kumar et al., "Cross-Layer Reliability Modeling of Dual-Port FeFET: Device-Algorithm Interaction," *TechRxiv Preprint*, 2022. [Online]. Available: https://doi.org/10.36227/techrxiv.21230789.v1
- [23] J. Cai *et al.*, "Energy efficient data search design and optimization based on a compact ferroelectric fet content addressable memory," in *DAC*, 2022, p. 751–756.
- [24] R. Rajaei *et al.*, "Compact single-phase-search multistate contentaddressable memory design using one fefet/cell," *IEEE TED*, vol. 68, no. 1, pp. 109–117, 2021.
- [25] A. Fritsch et al., "A 4ghz, low latency tcam in 14nm soi finfet technology using a high performance current sense amplifier for ac current surge reduction," in ESSCIRC, 2015, pp. 343–346.
- [26] Q. Liu *et al.*, "High performance utbb fdsoi devices featuring 20nm gate length for 14nm node and beyond," in *IEDM*, 2013, pp. 9.2.1–9.2.4.
- [27] M. M. Dahan *et al.*, "C-and: Mixed writing scheme for disturb reduction in 1t ferroelectric fet memory," *IEEE TCASI*, vol. 69, no. 4, pp. 1595– 1605, 2022.