Hierarchical Characterization of Analog Integrated CMOS Circuits

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Abstract

This paper presents a new method for hierarchical characterization of analog integrated circuits. For each circuit class, a fundamental set of performances is defined and extracted topology-independently. A circuit being characterized is decomposed in general subcircuits. Sizing rules of these topology-independent subcircuits are included into the characterization by functional constraints. In this way, bad circuit sizing is detected and located.

1. Introduction

Comprehensive characterization is a very important issue in analog design. It is necessary to verify design quality in order to avoid cost-intensive redesigns. Because of the shortening of design cycles, there is a great need for fully-automated analog circuit characterization. Further, computer aided circuit characterization is required to efficiently use sophisticated design methods, for example in the area of circuit optimization [ANO95], circuit modeling or worst-case simulation [AGW93].

Principally, two ways of automated characterization of analog circuits can be distinguished: the symbolic [GWS89] and the numerical simulation-based characterization. By choosing the numerical approach, we are potentially able to topology-independently characterize the static circuit behavior as well as the small and large signal behavior in the frequency and time domain.

In recent years control languages for numerical analog-simulators [ANS95,SG94, ANA96] have been developed. Also whole characterization systems like Vice [GH96] or [CS92] exist. Today, there are still some drawbacks in using these systems. The designer has to do time consuming preparation work. For each characterization problem he has to write a control program [ANS95,SG94, ANA96] or define a control flow [GH96] to simulate and extract the circuit performances. In [CS92] test benches and performance extractions are predefined. With this system the effort for preparing a characterization is essentially reduced. But circuit performances like dc-gain, slewrate or unity gain bandwidth only describe the cell level behavior of analog circuits. In this way, the internal circuit behavior is not characterized.

It is the goal of our characterization concept to avoid these drawbacks. A pilot version of the proposed characterization environment is applied in industry for designing high-performance full-custom CMOS circuits.

2. Hierarchical decomposition of analog systems

Figure 1 shows the hierarchical decomposition of analog systems. On the lowest level there are the components like capacitors, resistors or transistors. In this decomposition we classified the cascode circuit as component, because its basic function is equivalent to the function of a transistor. On the next level there are the transistor pairs. For analog CMOS designs we distinguish four transistor pairs: simple current mirrors, differential pairs, level shifter, complementary pairs. The next hierarchy is formed by subcircuits like gain stages or the cacode current mirror. Cells like bias generators or operational amplifiers are built up from elements of the first three hierarchies. At last analog systems like phased locked loops or analog interfaces can be decomposed in functional blocks like amplifiers, comparators or filters.

In our characterization concept we take into account the hierarchical decomposition of analog CMOS systems according to *Figure 1*. On the hierarchy levels of components, transistor pairs and subcircuits general design rules are derived. In the characterization these design rules are formulated and extracted as so called functional constraints. On cell level and functional block level circuit performances are defined and extracted.

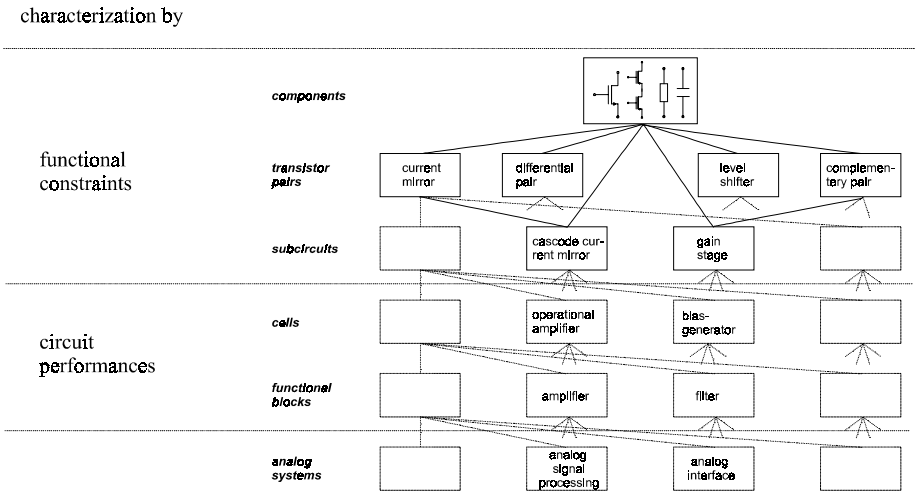

Figure 1: Hierarchical structure of analog systems

3. The hierarchical characterization environment

The characterization environment is based on numerical simulations. With the system we intend to characterize cells and functional blocks. It is created circuit class specific. All topologies of the same circuit class are pin-compatibel and their basic function is identical. For each analog circuit class a fundamental set of circuit performances is defined. These performances are potentially extractable for every representant of that circuit class. Further, each circuit being characterized is decomposed in principle components and subcircuits according to *Figure 1* and the corresponding functional constraints are included into the characterization. In this way, it is possible to control circuit sizing. Bad or even pathological sizing of the circuit is detected and located.

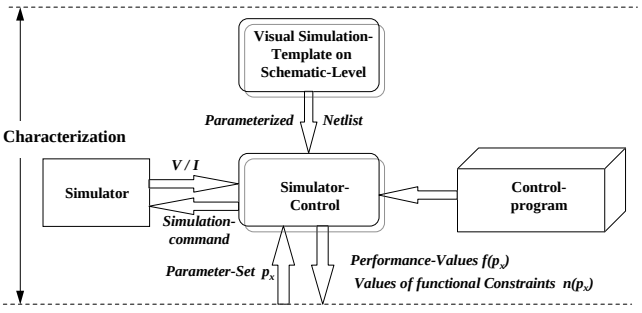

Figure 2: The components of the characterization environment

Figure 2 shows the components of our characterization environment. There is the circuit class specific simulation template on schematic level. The schematic of the circuit being characterized is included as a symbol into this simulation template. The simulator control, which communicates with the simulator, gets the parameterized netlist. The characterization process is controlled by the control program. By simulation and postprocessing of the simulated data the mapping of the parameter set $\mathbf{p}_x$ to the performance values $\mathbf{f}(\mathbf{p}_x)$ and the values of the functional constraints $\mathbf{n}(\mathbf{p}_x)$ is realized within the characterization environment. The results of such a nominal circuit characterization can also be used as input data of numerical design methods like circuit optimization [ANO95], response surface modeling or worst-case analysis [AGW93].

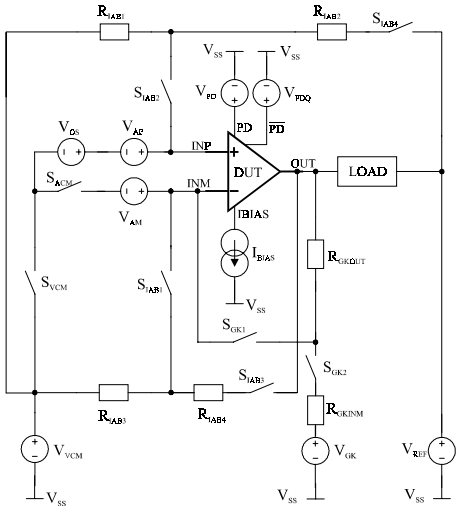

Figure 3: Simulation template of circuit class 'single-ended operational amplifier'

The most important cells in analog designs are operational amplifiers. Therefore, we created the characterization environment of the circuit classes 'single-ended operational amplifier' and 'fully-differential operational amplifier' at first. The simulation template on schematic level of the circuit class 'single-ended operational amplifier' is given in *Figure 3*. All necessary setups of performance simulation are realizable. They are adjusted by the control program (adapting the state of the switches, altering the sources). Any circuit load (resistor, diode, capacitor, ...) can be realized by setting up the general load at the output. The schematic of the circuit being characterized is included as a schematic symbol into the simulation template. With minimal effort, the environment is prepared to characterize each individual 'single-ended operational amplifier'.

The circuit class specific characterization environment is applied topology-independently. This is achieved by means of three general principles:

- flexible *parameterizing*
- *circuit performances* only describe the circuit behavior on cell or functional block level; therefore, each topology of the given circuit class is considered to be a „black box" for performance extraction
- sizing rules are derived from topology-independent elements of the first three hierarchies in *Figure 1*; the circuit being characterized is decomposed in these elements and the respective sizing rules are included as *functional constraints* into the characterization

In the following, the three principle ideas of our circuit class specific standard characterization environment are explained in detail.

3.1. Parameterizing

In the characterization environment four different types of parameters are distinguished. We consider three types of circuit parameters and the simulation parameters.

Circuit parameters p

Operating parameters $\boldsymbol{\Theta}$:

The operating parameters $\boldsymbol{\Theta} \in \Re^{n_\Theta}$ (V_{dd}, V_{ss}, Temperature) describe the operating conditions of the circuit. They are circuit class specific.

Statistical parameters **s**:

The process-inherent fluctuations are represented by statistical parameters $\mathbf{s} \in \Re^{n_s}$. They are process specific and described by correlated multivariate statistical distributions.

Design parameters **d**:

The design parameters $\mathbf{d} \in \Re^{n_d}$ are circuit specific and their values are explicitly determined by the designers (transistor geometries W; L, resistors R, capacitances C).

Simulation parameters $\boldsymbol{\zeta}$:

The simulation parameters $\boldsymbol{\zeta} \in \Re^{n_\zeta}$ are circuit class specific and define the values and ranges of physical parameters (e.g. voltage step of slewrate simulation or sweep range of time, frequency, voltage) of the simulation. Further, all parameters that configure the extraction of performances and functional constraints are called simulation parameters.

The simulation parameters are defined and initialized within the control program. Here, the so called extraction conditions are also defined. Extraction conditions check the possibility of extracting desired circuit performances from simulated data.

Moreover, the simulation parameters also tune the numerical algorithems of the circuit simulator.

3.2. Circuit class specific performances f

For each analog circuit class a fundamental set of circuit performances $\mathbf{f} \in \Re^{n_f}$ is defined. The performances must be defined topology-independently to enable their extraction for each structure of the circuit class without additional effort. Therefore, the cells and functional blocks being characterized are considered as „black boxes". All performances are extractable by postprocessing simulation data from external pins. In our environment circuit performances are always single values. Characteristic simulated curves (e.g. bode plot) are stored only for manually checking the simulation process. In order to avoid a higly redundant characterization result, curves are not defined as circuit performances.

To give a survey over the potential performances of analog circuits, the hierarchical performance tree is defined (*Figure 4*). In principle, the circuit performances describe the static and dynamic behavior of the circuit. The static behavior is calculated by dc or dc-transfer simulations. The dynamic behavior is calculated by ac (small signal) or transient (large signal) simulations. The first two hierarchies of the performance tree are general for all analog circuit classes. By going more into detail, the following hierarchies become circuit class specific. The performance tree of the circuit class 'single-ended operational amplifier' is shown in detail in *Figure 4*. At the end of each path of the performance tree, there is the name of an individual circuit performance (single value

performance). On the whole, for the circuit class 'single-ended operational amplifier' 29 different circuitperformances are defined. These 29 performances are extractable for each individual single-ended operational amplifier by numerical simulations.

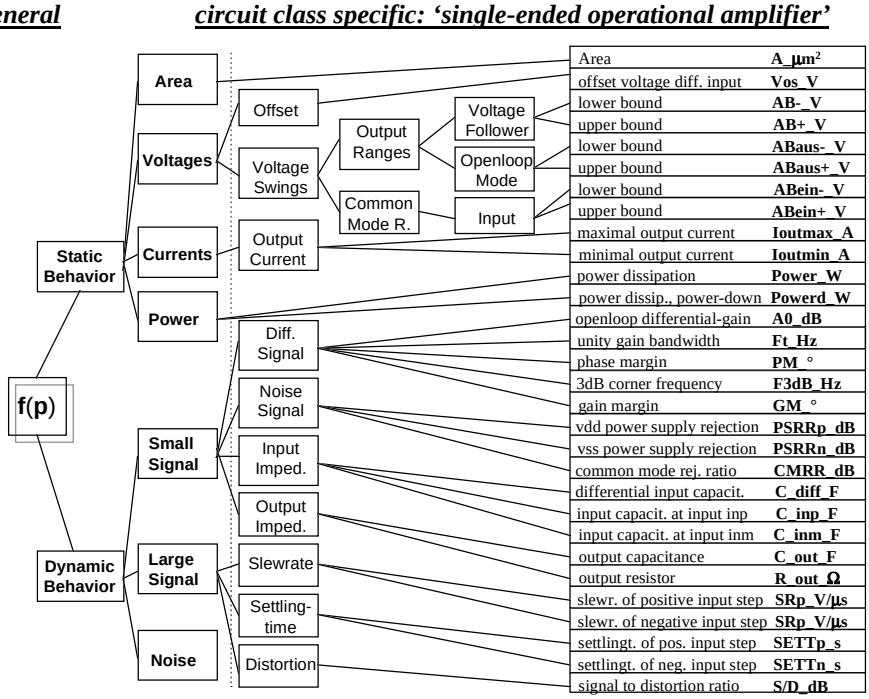

Figure 4: The general and 'single-ended operational amplifier' performance tree

3.3 Functional constraints

Performances only describe the circuit (class) behavior on cell respective functional block level. Circuit specifications define requirements on performances. Normally, circuit specifications are incomplete. Therefore, bad or pathological circuit sizing that is not indicated by the specified circuit performances can occur. To avoid this problem, we decompose the cell or functional block being characterized in the elements of the first three hierarchies in *Figure 1*. Sizing rules of these elements are derived and included as functional constraints into the characterization process. These sizing rules in essential express general function and matching conditions. In this way, circuit knowledge is taken into consideration during characterization. Thereby, the proper function of the circuit is guaranteed by fulfilling the functional constraints. Functional constraints are either equality or inequality constraints.

Figure 5 gives a short survey over potential functional constraints. Principally, functional constraints are devided into sizing rules of design parameters and sizing rules of properties that have to be calculated by simulation.

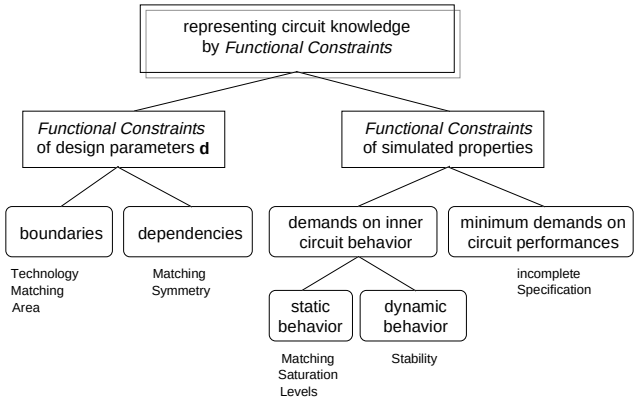

Figure 5: Potential functional constraints

To shorten this paper, the derivation of the functional constraints is only superficially presented for transistors and transistor pairs in the following section. The functional constraints of these elements cover the majority of all relevant functional constraints of cells and functional blocks.

4. Derivation of functional constraints

4.1. MOS Transistor

In CMOS analog designs there are three important regions of operation [SH68] of the MOS transistor:

- MOS transistor as voltage controlled current source (vccs)
- MOS transistor as voltage controlled resistor (vcr)
- MOS transistor as voltage controlled switch (vcs)

For the MOS transistor we defined three functional constraints that definitely separate the important regions of operation.

4.2. MOS transistor pairs

Transistor pairs play an important role in CMOS analog design. The following ones are relevant [LS94]:

- simple current mirror
- differential pair
- level shifter
- complementary pair

Transistor matching is a basic concept of analog CMOS design, especially concerning transistor pairs. We defined four general functional constraints for transistor matching [LHC86]. These functional constraints essentially represent sizing rules to minimize threshold voltage U_T mismatch, channel length modulation λ mismatch and transconductance factor k mismatch of transistor pairs. *Table 1* gives a short survey over the quality and quantity of the potential functional constraints we defined for transistor pairs. We referenced to the functional constraints of the MOS transistor and transistor matching to derive the functional constraints of the different transistor pairs.

To sum up, we are potentially able to check 7 functional constraints for the simple current mirror and the differential pair, 9 functional constraints for the level shifter and 2 for the complementary pair.

Transistor Pair	MOS Transistor	Transistor Matching	Additional Constraints
Simple Current Mirror	1	3	3
Differential Pair	1	4	2
Level Shifter	1	3	5
Complementary Pair	-	-	2

Table 1: Types and number of functional constraints of transistor pairs defined within our hierarchical characterization environment.

5. Example

5.1. Characterization of folded-cascode single-ended operational amplifier

The introduced hierarchical characterization environment has been used to size the folded-cascode [AH87] operational amplifier in *Figure 6*.

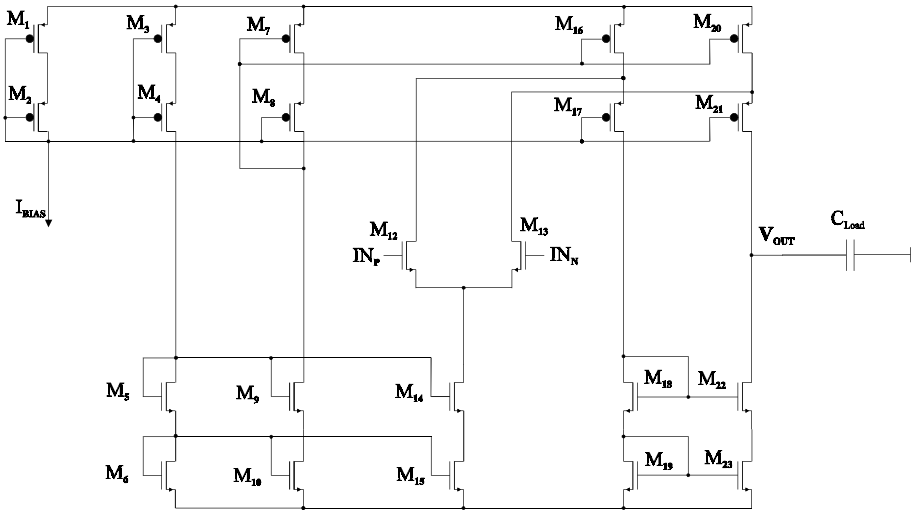

Figure 7: Folded-cascode operational amplifier

For this circuit the specification and the values of the specified circuit performances at the initial parameter point are given in *Table 2*. All specifications are met. Therefore, at the first glance everything seems to be ok.

Performance	A0_dB	Ft_Hz	PM_°	SRp_V/µs	SRn_V/µs	SETTp_s	SETTn_s
Specification	> 75dB	>15MHz	> 50°	> 7.5V/ms	> 7.5V/ms	< 150ns	< 150ns
Initial Sizing	79.1dB	16.8MHz	55.7°	8.4V/ms	8.1V/ms	95ns	99ns

Table 2 : Specified performances, specification and performance values at initial point

The folded-cascode circuit in *Figure 7* has been hierarchically decomposed. For the hierarchies in *Figure 1* we got:

components: 22 MOS transistors,
5 cascode circuits
transistor pairs: 5 simple current mirrors,
1 differential pair
subcircuits: 3 cascode current mirrors

From this decomposition and the defined general functional constraints of these elements, we got 73 functional constraints for the whole circuit: 32 parameter tracking relations (equality functional constraints) and 41 functional constraints of simulated properties (inequality functional constraints). The functional constraints were semi-automatically included into the characterization process.

For the evaluation of the functional constraints only an operating point simulation is necessary, which anyway must be done before each performance simulation. Therefore, we evaluated all functional constraints at the initial parameter point without additional simulation effort. All parameter tracking relations were fulfilled with the initial sizing. But through the evaluation of the 41 functional constraints of simulated properties, we noticed the violation (negative values) of 9 functional constraints.

Despite fulfilling the specification (see *Table 1*), the circuit has been bad designed, because transistor 7, 16, 20 did not work in saturation, the effective gate-source voltage of the transistors of the current mirrors 6/10, 6/15, 19/23 has been too small (high sensitivity of U_T mismatch) and the difference of the drain potentials of transistor 5 and transistor 9 (cascode current mirror) has been too big. The circuit has been mismatch sensitive and sensitive to noise signals with this sizing. But from the extracted values of the specified circuit performances in *Table 2* this could not be detected.

Then we manually designed the circuit to fulfill both, the specification and the functional constraints. With the improved sizing all 73 functional constraints are fulfilled and the circuit is well designed.

To analyze the differences of the two sizings, all extractable circuit performances are calculated in *Table 3*.

	Initial Sizing	**Imp. Sizing**	**Performance**	**Initial Sizing**	**Imp. Sizing**
A0_dB	**79.1dB**	**88.2dB**	Powerd_W	23.2pW	25.1pW
F3dB_Hz	1.97kHz	751Hz	C_in_diff_F	873fF	2.85pF
Ft_Hz	**16.8MHz**	**18.8MHz**	C_inp_F	551fF	554fF
PM_°	**55.7°**	**68.8°**	C_inm_F	544fF	550fF
G_marg_dB	12.7dB	18.8dB	C_out_F	135fF	615fF
Vos_V	84.7µV	21.4µV	R_out_ Ω	13.9MΩ	6.2MΩ
AB-_V	0.71V	0.79V	PSRRp_dB	72.2dB	79.3dB
AB+_V	4.4V	4.2V	PSRRn_dB	42.1dB	57.1dB
ABaus-_V	1.15V	1.38V	CMRR_dB	42.2dB	58.4dB
ABaus+_V	2.57V	2.71V	**SRp_V/µs**	**8.4V/µs**	**18.2V/µs**
ABein-_V	0.76V	0.929V	**SRn_V/µs**	**8.1V/µs**	**17.2V/µs**
ABein+V	5.0V	5.0V	**SETTp_s**	**94.6ns**	**114ns**
Ioutmax_A	46.7mA	194mA	**SETTn_s**	**99.4ns**	**49.8ns**
Ioutmin_A	-46.7mA	-194mA	S_zu_D_dB	104.2dB	113dB
Power_W	1.43mW	2.18mW			

Table 3: **All extractable circuit performances with the initial and improved sizing**

The specified performances are printed in bold letters. With both sizings all specifications are fulfilled in the nominal point. But with the impoved sizing the overall circuit performance is much better compared to the performance values with the initial sizing.

There are especially large differences in the offset voltage Vos_V, the noise rejection ratios PSRRp_dB, PSRRn_dB and the common mode rejection ratio CMRR_dB. This indicates that there is much more mismatch and mismatch sensitivity in the circuit with the initial sizing compared to the improved sizing. Further, the maximal (minimal) output current Ioutmax_A (Ioutmin_A) and therefore the slewrate SRp_V/µs (SRp_V/µs) is much bigger with the improved sizing. As the desired currents in the current pathes with both sizings are identical, this clearly indicates that with the initial sizing, current mirrors don't work in saturation. But there are also circuit performances with better values at the pathological initial point: AB-_V, AB+_V, ABaus-_V, ABein-_V, Power_W, Powerd_W, C_diff_F, C_out_F, R_out_Ω, SETTn_s. If only these performances would be specified, a numerical optimizer perhaps would size a pathological circuit. Therefore, for locating and avoiding bad or even pathological circuit sizing, it is necessary to check and fulfill the functional constraints.

A whole simulation and extraction of all 29 circuit performances in *Table 3* and the 41 defined functional constraints of simulated properties took 5 minutes and 35 seconds on a SUN Sparc 20.

6. Conclusion

In this paper a concept of hierarchical characterization of analog integrated circuits has been presented. The proposed characterization environment is based on numerical simulations and used for the characterization of analog cells and functional blocks.

A circuit being characterized is hierarchically decomposed in components, transistor pairs and subcircuits. General sizing rules of these elements are defined and extracted during characterization as functional constraints. In this way bad or even pathological circuit sizing is detected and located within the circuit. By satisfying the functional constraints, it is guaranteed to create well designed circuits.

On cell level and functional block level circuit performances are defined. Performances describe the static circuit behavior as well as the dynamic small and large signal behavior in the frequency and time domain. By extracting the circuit performances and the functional constraints comprehensive circuit characterization is possible. To evaluate the functional constraints only an operating point simulation has to be done. As this is also necessary for each performance simulation, the functional constraints can be extracted without extra simulation effort.

The proposed characterization concept is circuit class specific. All circuits of a circuit class are pin-compatible and their basic function is identical. With the presented characterization environment each topology of a given circuit class can be characterized. We achieved this by following three general principles:

- flexible *parameterizing* by including four different types of parameters
- *circuit performances* only define the circuit behavior on cell or functional block level; therefore, the circuit is considered to be a „black box“ for performance extraction
- deriving *functional constraints* from topology-independent basic elements

Our characterization system is intensively applied for the industrial design of high-performance full-custom CMOS circuits. It is used for

- automated characterization of analog circuits and
- providing characteristic circuit data for numerical design methods (optimization, response surface modeling, worst-case analysis).

The proposed characterization method has been applied to design a folded-cascode circuit. With the initial sizing the circuit already fulfilled the specification, but nevertheless it has been bad designed, because important sizing rules have been violated. This bad sizing has been detected and located by verifying the functional constraints. Then, we manually designed the circuit to fulfill both, the functional constraints and the circuit specifications. By means of that sizing, the overall circuit performances have been essentially improved.

Acknowledgment

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