Power and Timing Modeling for ASIC Designs

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This paper presents a unified power and timing modeling for ASIC libraries. This ASIC library is being standardized and targeted for a design flow, where timing analysis is complemented by power analysis. We show benchmark results from new industrial gate-level power analysis tools.

Design of digital integrated circuits has become an increasingly complex process. In addition to timing analysis, power analysis is becoming a part of the overall design flow. There are many commonalities between ASIC timing and power modeling. In order to avoid overlap and proliferation of tool-specific library formats, OVI[1] is proposing a standard model for ASIC cell libraries, containing functional, timing, power, and physical information of cells and large blocks. This paper focuses on characterization, modeling and design flow for power analysis.

CMOS circuitry has two dominant components of power consumption, charge-discharge of capacitance and short circuit consumption. High-level power estimation tools consider only charge discharge consumption, using estimations of capacitance and switching frequency[3, 4]. In deep submicron design, wire capacitance becomes dominant for global interconnect, as shown in figure 1. Therefore the estimation needs to be verified by more accurate analysis after layout.

Short-circuit power depends on both the slewrate of the driving input and the load capacitance at the output. Typically the characteristic of short circuit current is strictly increasing with slew rate and strictly decreasing with load [6]. As shown in figure 1, short-circuit power is dominant for small fanout. Although various analytical models have been proposed [5, 2], characterization over a matrix of slew rate and load values is the most general and practical approach. Since the slew rate of rising and falling transitions on the same pin may be quite different, it is important to distinguish between the slew rate for rise and fall also for characterization of the short circuit current. Internal cell currents, consisting of charge-discharge currents of internal capacitances as well as short-circuit currents, are state-dependent. In summary, accurate characterization for power requires a superset of characterization for timing, since both delay and power depend on load, slewrate and circuit state. There are circuit states without switching outputs that still exhibit internal power consumption. For sake of generality, state-dependent static power consumption may be considered a well.

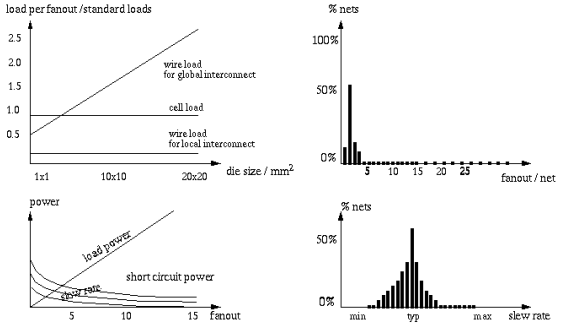

Figure 1. Deep sub-micron trends

With detailed power characterization data available, it is straightforward to predict the current consumption as a function of time during dynamic gate-level simulation with almost transistor-level accuracy. Even the transient behavior of the currents can be modeled, if the slew rates and event occurrence times are known. Static currents can be added to the model as constant currents during the time in between events.

ALF (Advanced Library Format) is an object-oriented language to describe characterization data for ASIC cells and functionality in a canonical way. In this paper, especially the power and timing data are of importance. For details see [1]. Figure 2 shows how the standard model fits into an ASIC design flow: timing, power and functional models come from the same primary library for cells. Models for megacells are created dynamically upon instantiation of a megacell in the design.

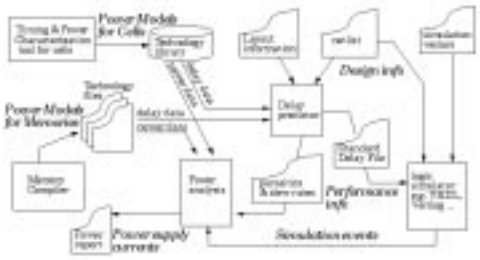

Figure 2. Integrated ASIC design flow

Module	lsipower	POET	vs. lsipower	Quickpower	vs. lsipower
accumulator	2.00	1.99	-0.4%	2.01	0.6%
multiplier	2.52	2.49	-1.3%	2.84	12.6%
shift	1.18	1.18	0.2%	0.877	-25.4%
controller	0.077	0.087	13.4%	0.101	31.2%
Total	5.77	5.75	-0.5%	5.83	1.0%

Table 1. Gate level power analysis tools

Capacitance and slew rates on all nets are calculated by a delay predictor Delays are backannotated to simulators and static timing analysis tools through Standard Delay Format (SDF) files, whereas the slew rate and capacitance back-annotation is reused for power analysis. A dynamic power analysis tool gets occurrence time and occurrence frequency of each characterization vector directly from simulation.

We show benchmark results for a sample design, a second order digital filter containing a $16x16$ bit multiplier and a 16 bit adder, some shift registers and control logic. We used the power analysis tool POET^{TM} from Advanced Development Group of Viewlogic and Quickpower^{TM} from Mentor Graphics, implemented the sample design in LSI Logic's $LCB500K$ library, and compared the results with LSI's internal power analysis tool, lsipower. All 3 tools use the same standard libraries and backannotated net capacitance. POET and lsipower match very close because slewrates were backannotated as well. Quickpower used estimated slewrates in this experiment. Standard slewrate annotation capability across tools, which is also pursued by standardization committees, will solve this problem.

A cell-by-cell comparison of the power consumption between lsipower and HSPICE shows the fine granularity of accuracy. lsipower is also capable of generating current waveforms, which match very close to HSPICE, as shown in figure 3.

As a conclusion, the accuracy of dynamic gate-level power analysis using vector-based models is mainly controlled by its inputs, i.e. the library and the backannotated design information. Very good correlation with transistor level analysis can be achieved.

Cell Name	Gate level(mA)	Transistor level(mA)	Error
eoa_1	0.010	0.010	0.00%
n1a_2	0.008	0.008	0.00%
n1a_1	0.008	0.007	14.29%
nd2a_1	0.007	0.006	16.67%
mux21ha_2	0.005	0.005	0.00%
n1a_3	0.005	0.004	25.00%
and2a_1	0.004	0.004	0.00%
and2a_2	0.004	0.004	0.00%
mux21ha_7	0.004	0.004	0.00%
n1a_6	0.003	0.003	0.00%
mux21ha_1	0.003	0.003	0.00%
mux21ha_3	0.003	0.003	0.00%
mux21ha_6	0.003	0.003	0.00%
mux21ha_5	0.003	0.003	0.00%
mux21ha_4	0.003	0.003	0.00%
n1a_4	0.003	0.003	0.00%
Control	0.077	0.076	3.50%

Table 2. Gate and transistor level power tools

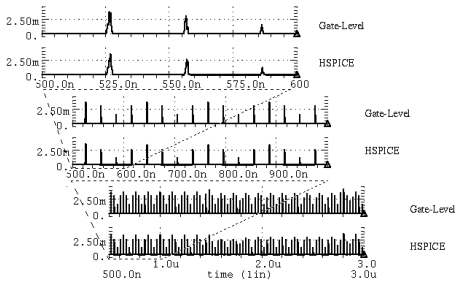

Figure 3. Gate level analysis versus SPICE

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References

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