Inductive and Capacitive Coupling Aware Routing Methodology Driven by a Higher Order RLCK Moment Metric

Amitava Bhaduri, Ranga Vemuri

HAL Id: hal-00181237
https://hal.science/hal-00181237

Submitted on 23 Oct 2007

Inductive and Capacitive Coupling Aware Routing Methodology Driven by a Higher Order RLCK Moment Metric

Amitava Bhaduri and Ranga Vemuri
Department of ECECS
University of Cincinnati, Cincinnati, OH 45221
{bhadhua, ranga}@ececs.uc.edu

Abstract

A new routing methodology, which accounts for inductive and capacitive coupling between neighboring wires is proposed. The inductive and capacitive coupling of the wires are introduced through a 'moment' based higher order RLCK cost function. The routing process guided by this costfunction ensures that the final solution has minimum ringing and delay.

1 Introduction

In the multi-GHz range, interconnect parasitics play crucial role in circuit performance. In traditional 'maze' routing it is difficult to introduce the effect of coupling parasitics. The maze router always finds the shortest path, which may lead to significant parallel runs between two neighboring wires giving rise to considerable amount of inductive and capacitive coupling. In this paper, we propose a routing methodology driven by a 'moment-based' cost function. This costfunction accounts for the higher order R,L,C,K parasitics between neighboring wires and converges to a routing solution that minimizes the overall delay of the nets and results in a better waveform response for all the nets.

2 Related Work

Crosstalk reduction (coupling capacitance) has been done in [1]. The authors in [2], developed various performance driven routing strategies using a simple Elmore (RC) delay model. Cong et al. [3], have used higher order RLC model in their MINOTAUR global router Though all of the above routing methodologies have their own merits, none of them considers complete R,L,C,K parasitics during routing.

3 Ringing and Central Moments

At high frequencies, the inductive effect of the interconnects gives rise to a T-line phenomenon called 'ringing', which can inadvertently cause the circuit to transit to a wrong state and cause logic failure. The repeated 'overshoots' and 'undershoots' also adversely affects the delay of the line as it increases the settling-time of the signal response. In addition

to the rise time (t_r) of the signal, the settling time (t_s) has to be accounted to obtain the actual wire delay (t_d) [4].

In order to account for the self and mutual inductive effects we resort to higher order moments of the impulse response. The concept of central moments is taken from probability theory and is used in delay characterization. The second and third central moments are as follows [5].

$$\mu_2 = 2m_2 - \frac{m_1^2}{m_0} \tag{1}$$

$$\mu_3 = -6m_3 + 6\frac{m_1 m_2}{m_0} - 2\frac{m_1^3}{m_0^2} \tag{2}$$

where, μ_2 is a measure of the spread and μ_3 the skewness of the impulse response. $\mu_3 = 0$ gives rise to a "critically-damped" signal response. On driving μ_3 closer to zero, 't_s' reduces to a negligible value. In addition to the minimum delay we also obtain a signal response that is less distorted and preserves signal quality. Hence, in our cost function we have chosen μ_3 minimization (closest to $\mu_{3ideal} = 0$) as the primary objective.

4 Proposed Methodology

We propose a routing methodology that uses the concepts of Section 3 to find the best possible overall routing solution that has the least parasitic interactions and the best waveform response for all the nets. We describe each of the steps used in our approach below.

Transfer Function and Template Generation: A simple example in Figure 1(A) demonstrates the transfer function generation of two interacting wires. Likewise, we pre-generate the symbolic transfer function of coupled interconnects as per the templates devised. In order to capture the parasitic interactions between the aggressor and the victim wires we have generated a few templates that covers the various ways in which 1-bend and 2-bend interconnects can couple with each other. The L-shaped route is a subset of Z-shaped route, hence we generate the templates with only Z-shaped nets in mind.

Route Cost Function: Let us consider that there are 'n' nets and at a particular instance the 'i'th net needs to be routed.
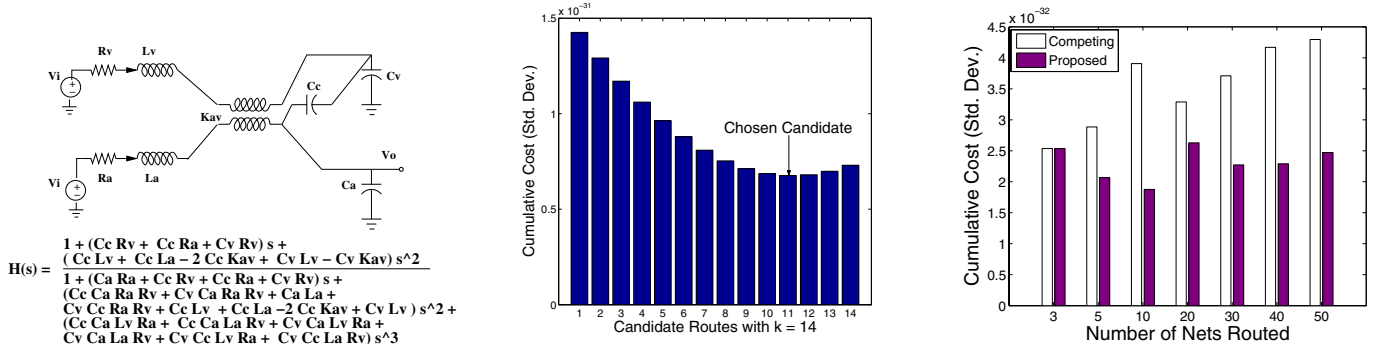
Figure 1. (A)Transfer function of 2 coupled wires (B) Possible Candidate Routes (C) Cumulative Cost comparison

1. For each of the 'k' candidates of net 'i' μ_3 is calculated.

2. The μ_3's of all the affected nets (victims) that have already been routed are re-evaluated.

3. For each candidate of net 'i', we compute the overall standard deviation of the routed and the current net as:

$$Cost = \sqrt{\frac{\sum_{n=1}^{i}(\mu_3^n - \mu_{3ideal})^2}{i}}$$

4. Store the values of the cumulative cost function for each candidate route.

5. Select the candidate route having the least cumulative cost and add to the list of routed nets.

The cost funtion thus gives a snapshot of the cumulative performance in terms of third-order central moments (μ_3) of all the nets up to the current net 'i'. Figure 1(B) illustrates an example with $k = 14$. Out of the 14 candidates, the cost function chooses candidate 11 as the routing solution.

Moment-driven Routing Technique: We have implemented the fundamental idea of a Mikami-Tabuchi line-search algorithm, which has been tailored to include our 'moment driven' cost function to sequentially route the nets. We have considered only 2-pin nets that can be connected using either a 1-bend or a 2-bend route. The inspiration of using L-shaped and Z-shaped technique find its origin in [1], [6]. As we inspect 'k' possible candidates for each of the 'n' nets in our sequential algorithm, the routing complexity is $\Theta(kn)$, in contrast to $\Theta(k^n)$ complexity in the method described in [1]. DRC violations are automatically eliminated by following the H-V routing technique. In addition, minimum spacing and width rules are accounted for during route generation.

5 Experimental Results

In our experiments we have randomly distributed pairs of pins and have routed the terminal pairs using our moment-driven line-search algorithm. We were able to find routes for each terminal pair such that the waveform response of the current net and the affected nets are best. As the individual signal response in terms of μ_3 is kept as close as possible to zero we find a routing solution that has a high signal quality and least settling time.

We compare our routing methodology to a standard line-search algorithm. For the competing approach, we picked the first route found by the router. We measured the cumulative cost (standard deviation) of the routing solution obtained, in separate instances of routing 3, 5, 10, 20, 30, 40 and 50 nets respectively. We see that the cumulative cost obtained using our method is significantly better than the competing approach as shown in Figure 1(C).

6 Conclusion

Interconnect parasitic consideration cannot remain restricted to a simple RC or a RLC model in performance-driven routing at multi-GHz frequencies. We have proposed a routing methodology that takes into account the inductive and capacitive coupling parasitics between neighboring wires during the routing process. The proposed approach ensures a routing solution for a number of randomly distributed pin-pairs, which has the least ringing and less settling time.

References

[1] R M. Smey, B. Swartz and P H. Madden. Crosstalk Reduction in Area Routing. In *DATE*, 2003.

[2] J. Lillis et.al. New Performance Driven Routing Techniques With Explicit Area/Delay Tradeoff and Simultaneous Wire Sizing. In *DAC*, 1996.

[3] J. Cong, C. Koh and P. Maddden. Interconnect Layout Optimization Under Higher Order RLC Model for MCM Designs. In *TCAD*, pages 1455 – 1463, 2001.

[4] H. B. Bakoglu. *Circuits, Interconnections, and Packaging for VLSI*. Addison-Wesley, 1990.

[5] R. Gupta, B. Krauter, L. T. Pileggi. Transmission Line Synthesis via Constrained Multivariable Optimization. In *TCAD*, pages 6 – 19, 1997.

[6] R. Kastner, E. Bozorgzadeh and M. Sarrafzadeh. Coupling Aware Routing. In *International ASIC/SOC Conference*, 2000.