A Triple-Mode Reconfigurable Sigma-Delta Modulator for Multi-Standard Wireless Applications

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Abstract

This paper presents the implementation and experimental characterization of a reconfigurable ΣΔ modulator intended for multi-mode wireless receivers that is capable to perform the analog-to-digital conversion for GSM, Bluetooth, and UMTS standards. The ΣΔ modulator reconfigures its cascade topology and building blocks in order to adapt the performance to the diverse standard specifications with optimized power consumption. The prototype has been implemented in a 130-nm CMOS technology and features dynamic ranges of 86.7/81.0/63.3dB and peak signal-to-(noise+distortion) ratios of 74.0/68.4/52.8dB at 400ksps/2Msps/8Msps, respectively. The modulator power consumption is 25.2/25.0/44.5mW, of which 11.0/10.5/24.8mW are dissipated in the analog circuitry.

1. Introduction

The next generation of wireless systems will require low-power multi-standard chipsets that are capable to operate over a number of different communication protocols, signal conditions, battery status, etc. [1] [2]. An efficient implementation of these chipsets demands for reconfigurable transceiver blocks that can adapt to the diverse specifications with minimum power consumption and at the lowest cost. One of the key blocks in multi-standard receivers is the ADC, because of the assorted signal bandwidths and dynamic ranges that can be required to properly handle the A/D conversion for several operation modes.

Compared to other data conversion techniques, sigma-delta modulators (ΣΔMs) are very suited for the implementation of multi-mode ADCs in highly integrated transceivers using digitally-oriented nanometer CMOS processes [3]-[9]. On the one hand, the key principles of ΣΔMs (oversampling and noise shaping) make them robust with respect to circuit errors. On the other, since both parameters determine the dynamic range of a ΣΔM, their variation can easily contribute to adapt the converter performance to different specifications with large hardware re-use. Indeed, changing the oversampling ratio of a ΣΔM from one standard of operation to another is a strategy commonly applied to adapt its dynamic range [3]-[9].

Also, the mandatory use of low oversampling in wideband applications typically forces the ΣΔM to achieve the required dynamic ranges by resorting to high-order shaping [3] [7] [9], to multi-bit embedded quantizers [4] [8], or both [6]. Thus, additional strategies to optimize the performance of a multi-mode ΣΔM for wideband standards can be found in the use of cascade architectures whose back-end stages can be switched on/off [6] or in the programming of notches within the signal band [3] [9].

Besides the former reconfiguration strategies at the architectural level of the ΣΔM, some others can be applied at the circuit level to adapt the power consumption of the analog blocks. For instance, if a multi-mode SC ΣΔM has to cope with a large spread of signal bandwidths, the sampling frequency, and thus the amplifier bias currents, can be also varied for the power consumption not to be determined by the standard with the largest bandwidth [9].

This work presents a triple-mode ΣΔM that combines architecture- and circuit-level reconfiguration strategies in order to adapt its performance to the requirements of GSM, Bluetooth, and UMTS standards. The modulator uses a cascade topology with a switchable multi-bit back-end stage, reconfigures its sampling frequency, and adapts the bias currents of the amplifiers to optimize the power consumption. The prototype has been implemented in a 130-nm CMOS process and operates with 1.2V/3.3V supplies. It features dynamic ranges of 86.7/81.0/63.3dB within signal bandwidths of 200kHz/1MHz/4MHz with 25.2/25.0/44.5mW power consumption, respectively.

This paper is organized as follows. Section 2 discusses the modulator architecture and its reconfiguration, whereas the circuit-level implementation is described in Section 3. Finally, Section 4 presents the experimental results of the prototype and compares its performance with reported multi-mode ΣΔMs.

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2. Modulator architecture

Fig.1 illustrates the architecture of the reconfigurable ΣΔM. It basically consists of a 4th-order cascade, built up with a 2nd-order front-end stage and two 1st-order stages (2-1-1 topology). The integrator coefficients maximize capacitor sharing and allow to progressively switch off the back-end stages (to obtain a 2-1 or a 2nd-order topology) while maintaining the modulator overload level [10]. Multi-bit operation can also be applied in the modulator last stage according to a dual-quantization scheme, with no need for calibration in the multi-bit DAC [11].

The oversampling ratio (OSR), the order of the noise shaping, and the resolution of the multi-bit last-stage quantizer in this reconfigurable ΣΔ architecture have been selected to fulfil the A/D conversion requirements of a direct-conversion receiver intended for GSM, Bluetooth, and UMTS standards. Table I summarizes the targeted dynamic ranges (DR) and bandwidths (BW) for each standard, together with the selected modulator architecture. For the standard with largest DR (GSM) a 3rd-order shaping and high oversampling are employed, whereas the modulator uses a 4th-order shaping and 2 bits in the last-stage for the standard with largest BW (UMTS) due to the limited oversampling. Note that the sampling frequency (Fs) is also increased for the UMTS standard.

The fully-differential SC implementation of the multi-mode ΣΔM is shown in Fig.2. The former reconfiguration strategies are handled at the circuit level with two signals (named GSM and SB), which switch on/off the last-stage of the cascade and control the division of the master clock frequency (80MHz) by a factor 2.

In addition to the configurations in Table I, either a 2-bit quantizer or a comparator can be selected in the last stage in order to give more flexibility to the prototype.

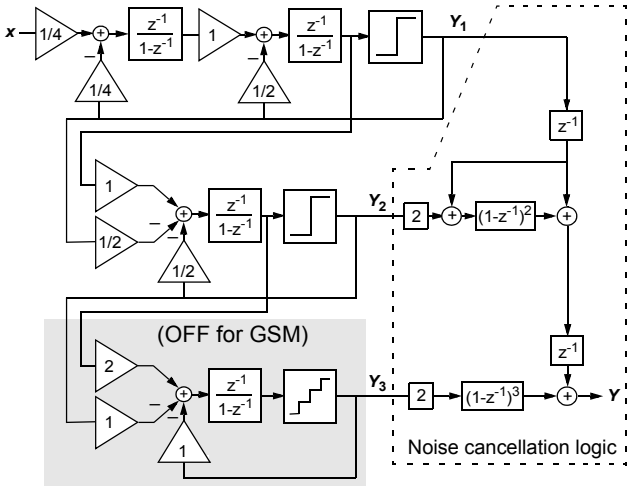


Fig. 1: Basic block diagram of the ΣΔM.

Table I: Specifications and ΣΔM architecture.

Standard	DR	BW	Architecture	OSR	Fs
GSM	13bit	200kHz	2-1	100	40MHz
Bluetooth	11bit	1MHz	2-1-1(2b)	20	40MHz
UMTS	9bit	4MHz	2-1-1(2b)	10	80MHz

The same sampling capacitor (0.25pF) is used for all standards, thus eliminating the need for switchable capacitor arrays at the modulator front-end. This value makes the dynamic range to be limited by kT/C noise for GSM, whereas it is limited by quantization noise for UMTS.

The modulator specifications in terms of DR and BW have been mapped onto electrical requirements of the building blocks (amplifiers, switches, comparators, etc.) using compiled equations capturing the non-ideal building-block behaviour and statistical optimization. This procedure is fine-tuned by behavioural simulation using SIMSIDES, a SIMULINK-based time-domain behavioural simulator for ΣΔMs [12]. These requirements define the

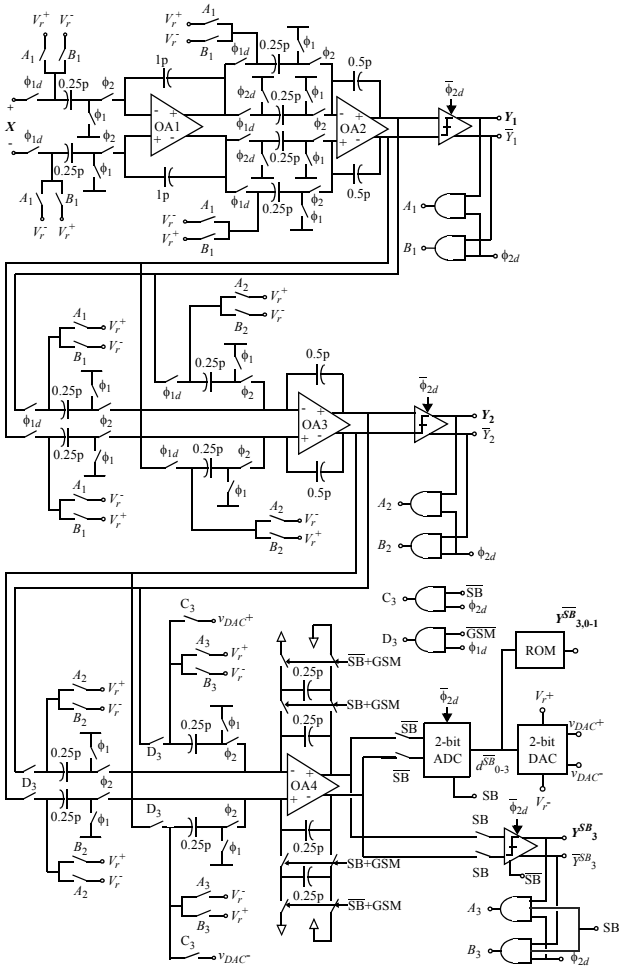


Fig. 2: Schematic of the reconfigurable ΣΔM.

starting point for the electrical sizing of the building blocks, which is described in the next section.

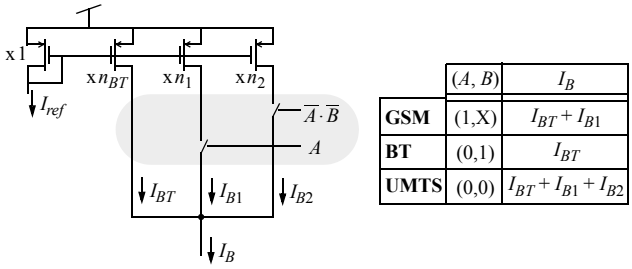
3. Circuit design

The four amplifiers in the reconfigurable ΣΔM (OA1 to OA4 in Fig.2) use a folded-cascode topology, since the required DC gains are not high, whereas the speed specifications are quite demanding for UMTS. The input pairs are pMOS, what affects power consumption but enables to cancel their body effect in order to reduce substrate noise coupling. The use of minimum-length transistors has been avoided in the input pair and in the current mirrors in order to limit 1/f noise and mismatching.

All amplifiers share the same transistor sizes, with the only difference being a larger differential input pair in the 2nd and 3rd amplifiers (OA2 and OA3) in order to obtain a faster response. The bias current of each amplifier is adapted from one standard to another according to the scheme illustrated in Fig.3. Depending on the amplifier and on the operation mode, the bias currents vary between 16uA and 80uA.

Table II summarizes the electrical parameters of the different amplifiers for each operation mode. Results correspond to the worst-case value of each individual parameter obtained from a corner analysis, considering fast and slow device models, ±10% variation in the 3.3-V analog supply and temperatures in the range [-40ºC, +85ºC].

All integrators in the ΣΔM use 0.25-pF sampling capacitors. This value has been fixed considering the trade-off between the modulator operation for GSM —in which thermal noise and capacitors mismatch can seriously limit the required resolution (13bit)— and that for UMTS —in which the required bandwidth (4MHz) in combination with large capacitive loads at the integrators can seriously impact power consumption. Metal-insulator-Metal (MiM) structures, which allow thin inter-metal oxide between the two top metal layers, were used. They exhibit a good matching (~0.1%) and small bottom-plate parasitics (<5%). Capacitor sharing allowed by the selected integrator coefficients reduces the number unit capacitors to only 2x17 in the complete differential implementation of the ΣΔM.



	(A, B)	I_B
GSM	(1,X)	$I_{BT} + I_{B1}$
BT	(0,1)	I_{BT}
UMTS	(0,0)	$I_{BT} + I_{B1} + I_{B2}$

Fig. 3: Adaptation of a bias current.

The design of the CMOS switches has been tackled with two main considerations in mind. First, the on-resistance heavily affects the integrator dynamic, slowing down its transient response [10]. Second, the non-linearity of the switch causes dynamic distortion at the modulator front-end, the more evident the larger the signal frequency. According to these considerations, resistances in the range of 260Ω can be tolerated in combination with the amplifier dynamics. In the process used, such a value can be obtained with standard-threshold CMOS transmission gates. The sizes of the pMOS and nMOS transistors have been selected to equalize their transconductances, keeping the resistance of the switch as linear as possible in the full-scale range (1.2V).

The first two stages of the modulator use comparators as single-bit quantizers. Their electrical requirements are not demanding; namely, less than 30-mV hysteresis and 40-mV offset. However, the maximum comparison time must be around a quarter of the clock period; i.e., 3ns for the 80-MHz clock frequency for UMTS. Therefore, the comparator uses the regenerative scheme illustrated in Fig.4 for speed reasons. It also includes an input amplifying stage to attenuate the impact of common-mode interferences on the comparator and of kick-back noise on the integrators.

The 2-bit embedded quantizer that is used in the modulator last stage for Bluetooth and UMTS consists of a flash ADC that compares the 4th integrator output with voltage taps provided by a resistive-ladder DAC. The ladder is built up with 6 unit resistors (400Ω, unsalicided p+ poly)

Table II: Worst-case amplifier performance (electrical simulation).

	GSM		Bluetooth			UMTS			
	OA1	OA2-OA3	OA1	OA4	OA2- OA3	OA1	OA4	OA2	OA3
DC gain (dB)	61.6	64.2	62.7		64.6	58.8		57.3	59.9
GBW (MHz)	244	143	183	105	130	326	102	251	232
Slew rate (V/us)	253	102	144	80	85	474	141	352	289
Equivalent load (pF)	0.6	1.3	0.6	1.1	1.3	0.6	2.2	1.3	
Output swing (V)	±1.8	±1.9	±2.1		±2.0	±1.4		±1.0	±1.2
Input eq. noise [nV/sqrt(Hz)]	11.8	10.4	13.6		11.0	10.5		7.8	8.2
Bias current (uA)	28	24	16		20	52		80	66
Power consumption (mW)	2.3	2.0	1.3		1.7	4.3		6.6	5.5

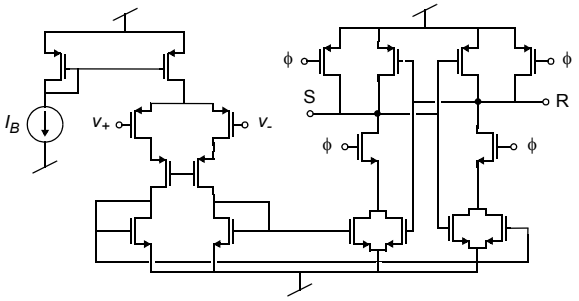


Fig. 4: Schematic of the comparator.

connected between voltage references of 2.25V and 1.05V. It provides a differential full scale of 1.2V with 0.5mA current consumption.

An on-chip voltage generator provides the reference voltages to the SC integrators and to the DACs. It consists of a band-gap reference and a resistive amplifier in inverting configuration. The main requirements for the references are a fast settling and a low output impedance in order to avoid dynamic distortion at the integrators. A 4-Ω maximum output impedance (required for GSM) is obtained within the signal bandwidth (up to 4MHz for UMTS).

4. Experimental results

The reconfigurable ΣΔ modulator has been implemented in a 130-nm 1-poly 8-metal digital CMOS process. Fig.5 shows the layout of the prototype (Fig.5a), highlighting its main parts, and a microphotograph of the chip (Fig.5b). The layout has been carefully planned to maximize the modulator performance in terms of robustness with respect to switching activity, including separate analog, mixed, and digital supplies, guard-rings surrounding each section of the circuit, etc. The complete modulator occupies 2.68mm^2 including bonding pads, whereas the core area is 1.40mm^2. The chip has been tested using the PCB shown in Fig.5c, which includes intensive filtering and decoupling strategies, as well as proper impedance termination to avoid signal reflections.

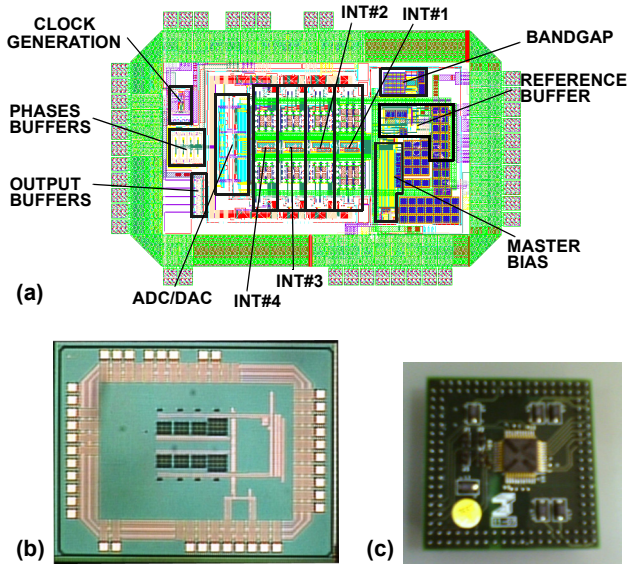


Fig. 5: Prototype implementation: (a) Layout, (b) Microphotograph, (c) Test PCB.

Fig. 6 illustrates the test set-up, in which an Agilent 93000 SOC test unit is used to generate the input, biasing, control, and clock signals, and to acquire the output bit streams of the modulator stages. After the bit-stream acquisition, data are transferred to a workstation, in which the noise cancellation logic is applied by software and the overall modulator output is post-processed.

Fig.7 shows the measured 65536-point Hanning-windowed FFTs of the modulator output, for the different standard configurations, considering a 58.6-kHz input sinewave with an amplitude of -9.5dBFS. Note that the reconfiguration of the noise shaping is clearly visible, together with the domination of white noise (for GSM) or quantization noise (for UMTS) within the corresponding bandwidths. However, a certain amount of offset and non-linearity is appreciable in the measured spectra, which is originated in the input signal conditioning at the PCB level (probably in the single-to-differential conversion and the common-mode setting, which is now under improvement).

The measured SNDR curves are depicted in Fig.8 for each operation mode. The prototype achieves a dynamic range of 86.7dB for GSM, 81.0dB for Bluetooth, and 63.3dB for UMTS, whereas the corresponding peak SNDRs are 74.0dB, 68.4dB, and 52.8dB. Note from Fig.8 that the SNDR drops prematurely due the harmonic content of the input signal to the prototype. The peak SNDRs are measured at -11.6dBFS for GSM and at -9.6dBFS for Bluetooth and UMTS (instead of at -5.6dBFS), what leads to a measured SNDR drop of 1.0bit for GSM and of 0.7bit for Bluetooth and UMTS.

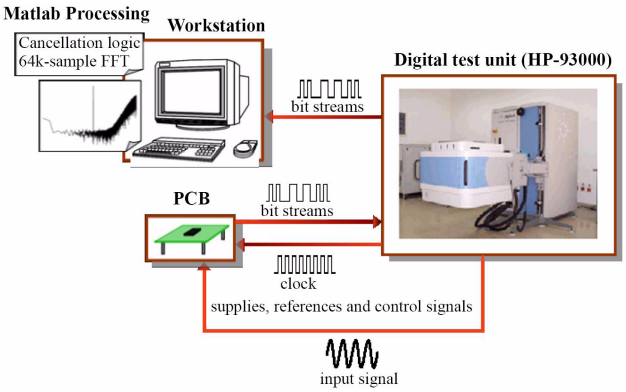


Fig. 6: Test set-up.

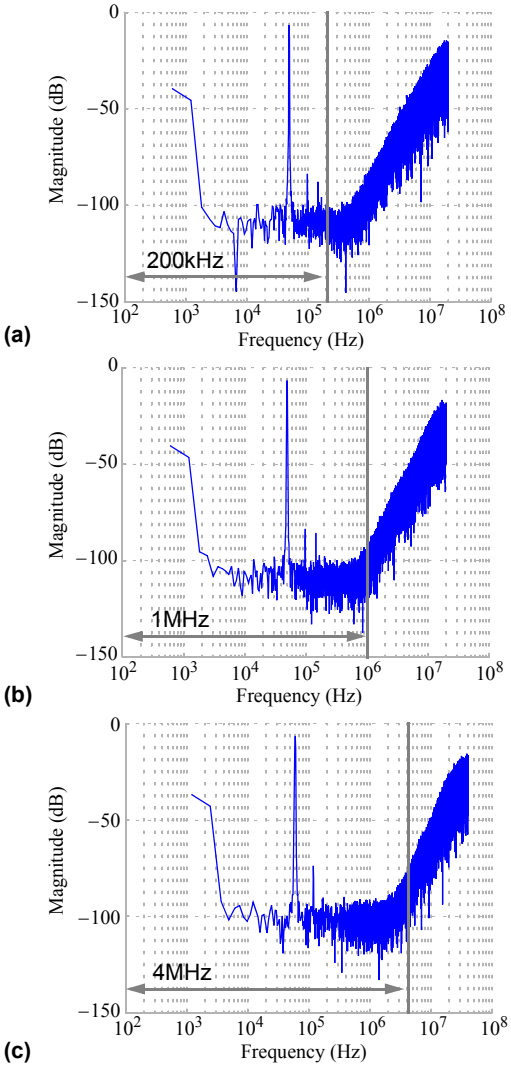


Fig. 7: Measured spectra for: (a) GSM, (b) Bluetooth, (c) UMTS.

Table III summarizes the most significant features of the measured performance for the reconfigurable ΣΔ modulator. The distribution of the power dissipation among the different modulator sections is also depicted in the table. The modulator power consumption is 25.2/25.0/44.5mW for GSM/Bluetooth/UMTS, of which 11.0/10.5/ 24.8mW are dissipated in the analog circuitry.

Table IV shows the state of the art in multi-mode low-pass SC ΣΔMs, extracted from ICs reported in open literature. The table contains the BWs, DRs, and power consumptions for each IC and standard of operation. For the sake of completeness, the employed modulator architecture, its OSR and Fs of operation, and the supply voltage and technological process of the implementation are presented as well. In addition, the two figures-of-merit (FOMs) commonly employed to evaluate the modulator

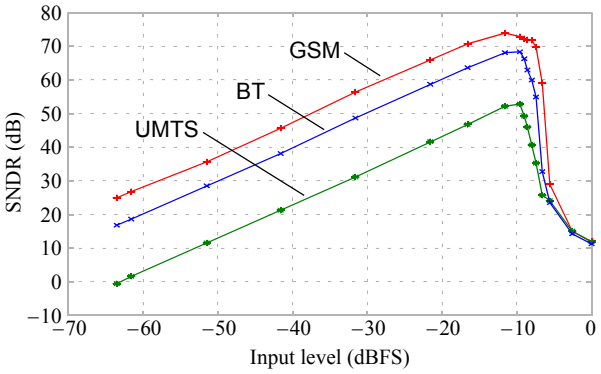


Fig. 8: Measured SNDR curves.

Table III: Summary of measured performance.

		GSM	BT	UMTS
Modulator architecture		2-1	2-1-1(2b)	
OSR		100	20	10
BW (MHz)		0.2	1	4
Fs (MHz)		40		80
DR (dB)		86.7	81.0	63.3
Peak SNDR (dB)		74.0	68.4	52.8
Process		130nm CMOS		
Core area		$1.4mm^2$		
Power consumption[a] (mW)		25.2	25.0	44.5
	Analog core @ 3.3V	11.0	10.5	24.8
	Ref. buffer @ 3.3V	19.0	18.9	20.0
	Mixed @ 3.3V	9.6	10.0	13.9
	Digital @ 3.3V	4.1	4.1	5.5
	Digital @ 1.2V	0.6	0.6	1.2

a. Digital output buffers and reference buffer are not included.

performance are also included; namely,

$$\mathrm{FOM}_1 = \frac{\mathrm{Power(W)}}{2^{\mathrm{DR(bit)}} \cdot 2\mathrm{BW(Hz)}} \cdot 10^{12} \quad (1)$$

$$\mathrm{FOM}_2 = 2kT \cdot \frac{3 \cdot 2^{2\mathrm{DR(bit)}} \cdot 2\mathrm{BW(Hz)}}{\mathrm{Power(W)}} \quad (2)$$

Note that FOM_1 specially accounts for the power consumption, whereas FOM_2 stresses on the modulator resolution. Therefore, the smaller FOM_1 and the larger FOM_2, the better performance of the ΣΔ modulator.

Since no specific FOMs have been yet proposed for the multi-standard scenario, the mean values of the FOMs obtained for each standard have also been included in Table IV as a way to evaluate the overall performance of the multi-mode ΣΔMs.

Note that the presented prototype compares favourably to the ICs reported in [4], [7], and [8], and it also achieves a performance comparable to that in [3], being thus competitive with the current state of the art.

Table IV: State of the art in low-pass multi-mode SC ΣΔMs.

	Burger, [3]			Miller, [4]				Gomez, [5]			Dezzani, [6]		Shim, [7]		Lim, [8]		Christen, [9]				This work		
Standard	GSM		UMTS	AMPS	GSM	CDMA	UMTS	GSM		UMTS	GPRS	UMTS	GSM	UMTS	CDMA-2k	UMTS	EDGE	UMTS		WLAN	GSM	BT	UMTS
BW (MHz)	0.2		3.84	0.018	0.2	0.625	1.92	0.2		2	0.1	1.92	0.1	2.5	0.615	1.92	0.1	1.92		10	0.2	1	4
Fs (MHz)	104		184	23			46	26		46	39	38.4	3.2	40	40	61	26	46.08	61.44	240	40		80
OSR	260		24	639	57.5	18.4	12	65		11.5	195	10	16	8	32.5	16	130	12	16	12	100	20	10
DR (bit)	14.0	13.0	8.7	15.2	13.7	13.0	12.2	12.8	12.0	8.0	13.3	11.3	12.3	8.8	12.3	11.0	14.3	11.3	12.8	10.8	14.1	13.2	10.2
Power (mW)	11.5	7.5	13.5	30.0			50.0	2.4	1.4	2.9	2.4	4.3	4.0		22.7		2.9	3.5	7.4	20.5	25.2	25.0	44.5
FOM_1	1.8	2.3	4.2	22.1	5.4	2.9	2.8	0.8	0.9	2.8	1.2	0.4	4.0	1.8	3.7	2.9	0.7	0.4	0.3	0.6	3.6	1.3	4.7
$FOM_2 \times 10^5$	23.3	8.4	0.2	4.2	6.3	7.0	4.2	21.2	12.0	0.2	21.2	14.2	3.2	0.6	3.4	1.8	73.0	18.4	68.7	8.2	12.2	17.7	0.6
$\overline{FOM}_1$	2.8			8.3				1.5			0.8		2.9		3.3		0.5				3.2		
$\overline{FOM}_2 \times 10^5$	10.8			5.4				11.1			17.7		1.9		2.6		42.1				10.2		
Architecture	3rd-order			2nd order (6bit)				2nd order (5level)			2nd order	2(5l) -1(5l)	3rd order		2nd order (11level)		2(3l)-2(3l)				2-1	2-1-1(2b)	
Supply (V)	2.5			2.7				1.2	1.5	1.2	1.2		1.8		2.8		1.2				1.2/3.3		
Process	0.25um CMOS			0.18um CMOS				130nm CMOS			130nm CMOS		0.18um CMOS		130nm CMOS		130nm CMOS				130nm CMOS		

Conclusions

A multi-mode ΣΔM has been presented that is capable to adapt its architecture- and circuit-level parameters to the required specifications for GSM, Bluetooth, and UMTS standards. The modulator uses a 4th-order cascade topology that is capable to power its last stage down and adapts the sampling frequency and the bias currents of the amplifiers in order to optimize power dissipation. The prototype has been integrated in a 130-nm CMOS process and features dynamic ranges of 86.7/81.0/63.3dB at 400ksps/ 2Msps/8Msps, respectively.

Thanks to the combined use of the diverse reconfiguration strategies, the presented prototype achieves a competitive performance, while covering a wide conversion region of the resolution-bandwidth plane.

Acknowledgements

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