Using Current to Drive Two SDC Memristors Connected in Series and in Anti-Series

Albert Cirera
Dept. of Electronic & Biomedical Eng.
Universitat de Barcelona Barcelona, Spain acirera@ub.edu

Blas Garrido
Dept. of Electronic & Biomedical Eng.
Universitat de Barcelona Barcelona, Spain blas.garrido@ub.edu

Pere Miribel-Catala
Dept. of Electronic & Biomedical Eng.
Universitat de Barcelona Barcelona, Spain peremiribelcatala@ub.edu

Jordi Colomer-Farrarons
Dept. of Electronic & Biomedical Eng.
Universitat de Barcelona Barcelona, Spain jcolomerf@ub.edu

Antonio Rubio
Dept. of Electronic Engineering Universitat Politècnica de Catalunya Barcelona, Spain antonio.rubio@upc.edu

Ioannis Vourkas
Dept. of Electronic Engineering Universidad Tecnica Federico Santa Maria (UTFSM)
Valparaiso, Chile ioannis.vourkas@usm.cl

***Abstract*— Networks of bipolar memristors have a rich collective switching behavior, which can be exploited in computing applications. Such a small network is formed by a pair of bipolar memristors connected in a series or anti-series configuration. The latter is known as complementary resistive switch (CRS), and has been studied for memory and for logic applications. While CRS structures have been investigated with voltage-based driving schemes, the collective behavior of current-driven networks of memristors has not yet been explored. To this end, here we present preliminary experimental results from two bipolar self-directed channel (SDC) memristors by *Knowm Inc.*, connected in series with the same or the opposite polarity, driven by current. The amplitude of the applied current pulses varied between |0.1 uA| and |1.0 uA|. The results demonstrate that current-based driving is effective for programming simultaneously memristors that are connected in series. Moreover, the devices in the CRS configuration respond in a complementary way to the applied input current. We observed a stable and uniform performance of the devices in all our experiments. Current pulses of |0.1 uA| did not affect the state of the memristors, so they can be used to perform READ operations in current-driven resistive memory modules.**

Keywords— memristor; resistive memory; complementary resistive switch; characterization; Knowm; SDC; current source;

I. INTRODUCTION

Memristor devices represent a very promising technology for future resistive memory chips [1], [2]. Memristors store information in the form of resistance and opposite polarities of the applied input signal are required to program the state of bipolar devices. A transition from a state of high resistance to a state of low resistance (HRS to LRS) is called a SET. The opposite transition is called a RESET. Memristors generally demonstrate a threshold-type switching behavior [3], thus their resistive state changes only when the applied signal exceeds the corresponding thresholds for SET and RESET.

Several works in the literature discuss the potential of networks of bipolar memristors for a variety of applications [4], [5]. Memristors connected in series have been explored for logic gate implementations [6], [7]. Likewise, the dynamic switching response of series of memristors with opposite polarities, has attracted considerable interest. One such example is the complementary resistive switch (CRS), proposed for memory [8], [9] and for logic tasks [10], [11].

The voltage thresholds V_{SET} and V_{RESET} of the memristors play an important role for their applicability in network-based structures. In [12] we find a detailed analysis of the way memristors connected in series behave under different biasing schemes, depending on the relation between the V_{SET} and V_{RESET} thresholds. Due to the dynamic redistribution of the voltage drop on each device while their resistance is changing, incomplete SET or RESET transitions can occur, which lead to gradual performance degradation of the CRS configuration [13]. Many works have focused on the impact of threshold variability in the global performance of the memristor network [14]. Such studies are greatly facilitated from the fact that most device models for simulation assume the existence of voltage thresholds for SET/RESET [15]. Moreover, whenever a conditional switching behavior is required; i.e., when a memristor should undergo a conditional state transition, depending on the state of the rest of the interconnected memristors [16], usually the feasibility of this depends on the relation between the V_{SET} and V_{RESET} values. This makes voltage-driven schemes challenging for networks of interconnected memristors, which still constitute a topic of interest from the modeling and the fabrication point of view

[17], [18]. However, lately different research groups have used current-driving schemes for memristor characterization, and reported interesting performance observed when the devices are submitted to constant current instead of constant voltage [19], [20], [21]. These works concentrate on the exploration of the response of discrete memristors. However, the collective behavior of networks of memristors under current-driven schemes has not been taken into consideration.

In this context, we present preliminary experimental results from the response of two bipolar memristors connected in series, driven with current. The devices were connected both with the same and with the opposite polarity (anti-series). We used a custom circuit for a voltage-controlled current source [22], [23] which allows the fine control of low levels of current. The devices under test were self-directed channel (SDC) memristors, commercially available in different packages and structures by *Knowm Inc*. [24], [25]. Our results demonstrate that current-based driving is effective to trigger simultaneous transitions in the resistive state of memristors that are connected in series. We used current pulses of Gaussian shape whose amplitude varied between |0.1 uA| and |1.0 uA|. We observed SET and RESET events for currents above 0.1 uA while the measured voltage drop on each device was always below 2 V. The collective response of two series

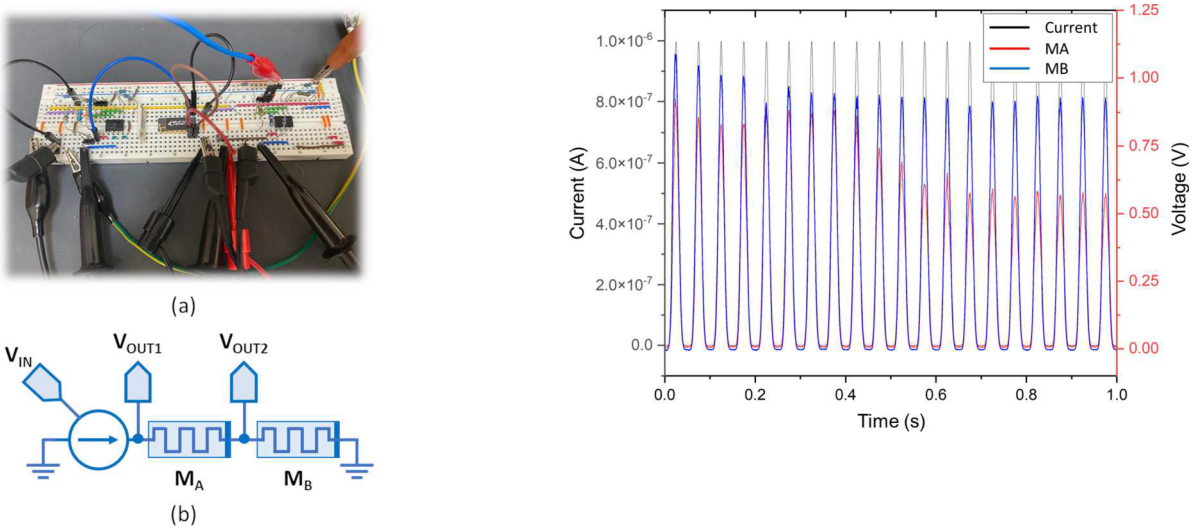


Fig. 1 Overview of the experimental setup. (a) Circuit implementation on a protoboard. (b) Compact schematic of the circuit showing a voltage-controlled current source driving two memristors connected in series.

memristors with the same polarity was found qualitatively equivalent with that of a single memristor. On the other hand, the memristors in anti-series configuration responded in a complementary way to the applied input current. We observed a uniform performance of the devices in all the experiments, where low current pulses of |0.1 uA| did not affect the state of the network. So, they are suitable for READ operations in current-based drivers of resistive memory (ReRAM) modules.

II. Experimental Setup

We show in Fig. 1(a) an overview of the experimentally implemented circuit. We distinguish the DIP16 package of 8 discrete self-directed channel (SDC) memristors by *Knowm Inc*. We used the ADP3450 instrument by Digilent, which has a digital oscilloscope and a function generator, controlled via the *WaveForms* software running on a PC. To drive the two memristors, we used two TL082 opamps in a custom circuit of a modified Howland current source, controlled by voltage. The use of such current pump was suggested in [23] and it was previously used in nanowire measurements [26]. The potential application of this circuit on memristors and its configuration have been thoroughly discussed elsewhere [21], [22], [27].

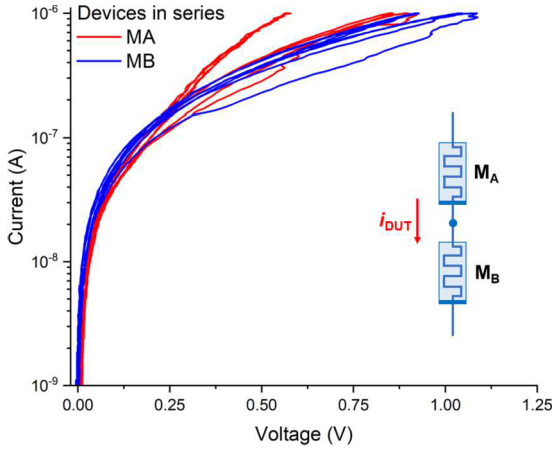
A compact schematic of the implemented circuit is shown in Fig. 1(b). The two series memristors M_A and M_B were connected to the output node of the current source. Through the control voltage V_{IN} we determine the common current flowing through both devices, which is independent of the resistance of M_A and M_B. The circuit permits monitoring the voltage drop on two different nodes using TL082 operational amplifiers in a voltage-follower (buffer) configuration. In all the conducted experiments, the current pulses we applied were *Gaussian-shaped* and had a 10-ms full width half maximum (FWHM) [21] with variable amplitude between |0.1 uA| and |1.0 uA|. Measurements were carried out at room temperature.

III. Results and Discussion

A. Forming process

In order to achieve a uniform SET/RESET switching, the forming process, which takes place on pristine memristors, is essential [27], [28]. Controlling the current through the devices is an effective way to realize the forming process.

(a)



(b)

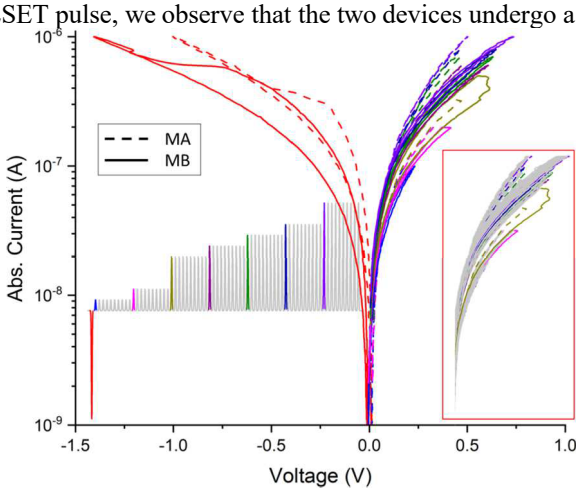
Fig. 2 The forming process of two memristors. (a) The evolution of the voltage on each device during the application of the current pulses to the two devices connected in series. (b) Semi-log representation of the current w.r.t. the voltage on every device, only for the two first and the two last pulses.

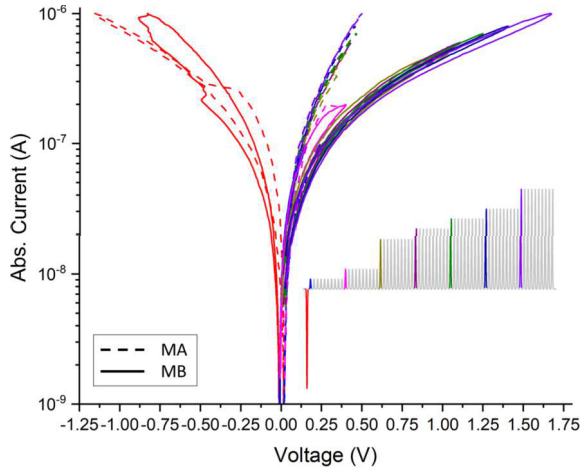
When two devices are connected in series with the same polarity and are driven with the same current, their forming can take place simultaneously. In our case, a sequence of 20 positive current pulses of 1.0 uA amplitude were applied. Fig. 2(a) shows the input current pulses and the evolution of the voltage drop on every device, whereas Fig. 2(b) shows the semi-log representation of the two *i-v* curves. We observe that the voltage gradually drops on both devices, which is indicative of the simultaneous reduction of their resistance. With the same current flowing through both devices, we would expect an identical response. However, we note that at the peak of the last current pulse, the voltage on M_B (V_{OUT2}) is nearly 2× the voltage on M_A (V_{OUT1} - V_{OUT2}). Therefore, both devices respond in a coherent way, even though they eventually reach different resistive values for their LRS state.

B. Memristors with the same polarity

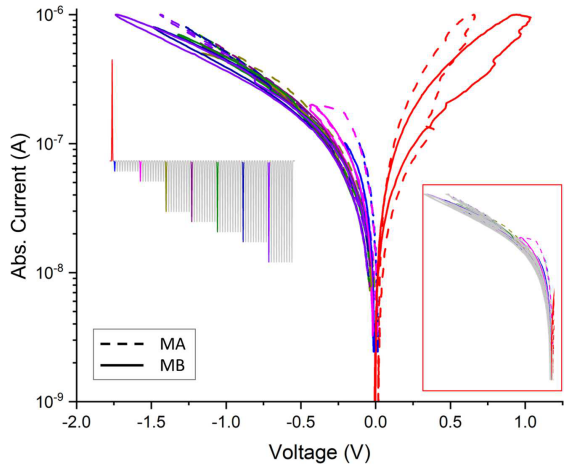
We studied the collective response of two memristors connected in series with the same polarity. We explored the effect of different current amplitudes during the SET process. To this end, the devices were first RESET to HRS using a negative pulse of -1.0 uA and then they were submitted to a sequence of positive pulse groups of gradually increasing amplitude. The amplitudes of the applied pulse groups were 0.1, 0.2, 0.5, 0.6, 0.7, 0.8, and 1.0 uA, respectively.

In Fig. 3(a) we show the response of the two memristors in a current-voltage representation. During the single RESET pulse, we observe that the two devices undergo a RESET





(a)



(b)

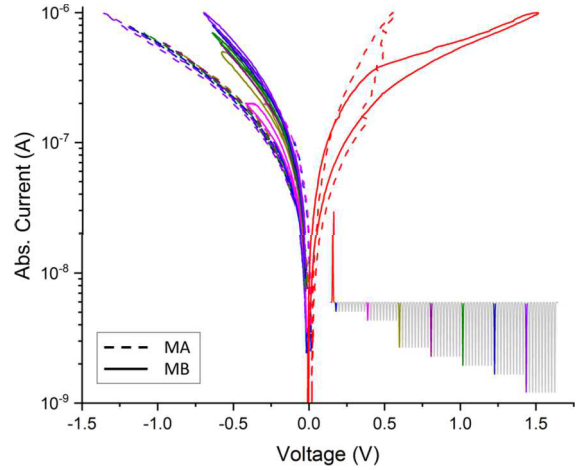
Fig. 3 Memristors in series. (a) The semi-log absolute current-voltage representation when a single RESET pulse was followed by a sequence of positive pulse groups. (b) The semi-log absolute current-voltage representation when a single SET pulse was followed by a sequence of negative pulse groups. We show the response only during the first pulse of every consecutive group. The timing of every pulse is shown with a different color in the inset. The rest of the pulses are shown in light gray color.

process in a sequential manner. At the peak of the negative current pulse, the voltage drop on M_B is nearly 40% higher than the voltage measured on M_A. By observing the curves in the first quadrant, we see that both devices undergo a SET process, where device M_A achieves a lower resistive state than M_B. The inset highlights the color correspondence with the timing of the pulses, and the remaining curves are shown in light gray color. There is no significant accumulative behavior during the application of consecutive pulses of the same amplitude. Nevertheless, higher current amplitudes drive the devices to lower resistive values. Similar observations can be made when studying the RESET behavior of the devices in Fig. 3(b), where the devices were first SET to LRS using a positive pulse of 1.0 uA and then were submitted to a sequence of negative pulse trains. No significant accumulative behavior is observed during RESET either. Both devices demonstrate a successful RESET behavior. The presented results confirm the initial hypothesis that both devices ought to behave in a "nearly" identical manner under the same inputcurrent.

C. Memristors with the opposite (anti-series) polarity

For the anti-series connection, we repeated the same experiments described in the previous section after connecting the device M_B with the opposite polarity. The objective is to

(a)



(b)

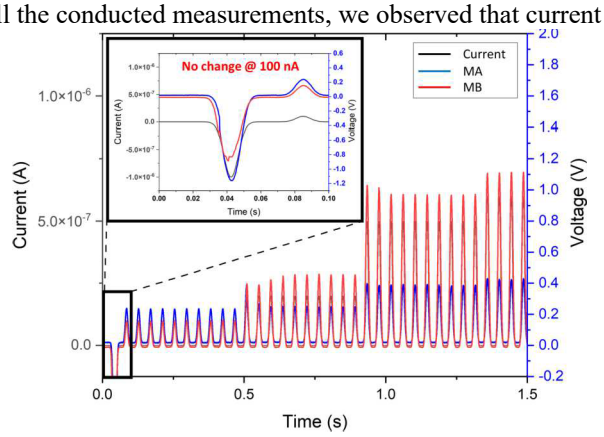
Fig. 4 Anti-series memristors. (a) The semi-log absolute current-voltage representation when a single negative pulse is followed by a sequence of positive pulse groups. (b) The semi-log absolute current-voltage representation when a single positive pulse is followed by a sequence of negative pulse groups. The timing of every pulse is shown with a different color in the inset. The rest of the pulses are shown in light gray color.

demonstrate that in a complementary resistive switch (RS) configuration (anti-series or simply "CRS"), the two memristors respond in a complementary manner to the applied input current. To better follow the response of each device, we examine the corresponding *i-v* curves separately.

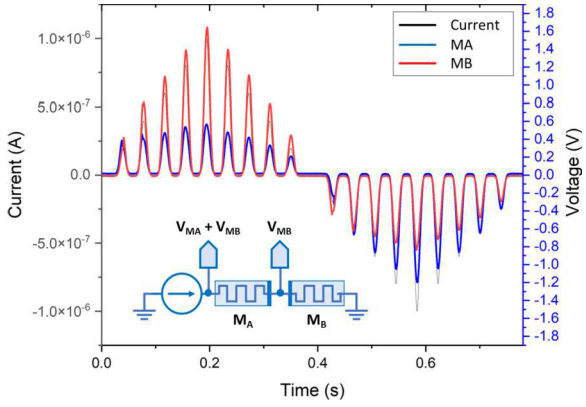
In Fig. 4(a) we show the response of the two anti-series memristors in a current-voltage representation. During the negative pulse of -1.0 uA, the device M_A is RESET to HRS whereas the device M_B is SET to LRS. The devices show the exact opposite behavior in the first quadrant, where positive pulses of 0.2 uA or higher trigger the RS event in the two devices. In Fig. 4(b) we observe a complementary switching response with the positive current pulse in the first quadrant, where the device M_A is SET to LRS and the device M_B is RESET to HRS. Next, the series of negative pulses trigger a complementary response. Therefore, both in Fig. 4(a) and in Fig. 4(b) we observe consistent switching behavior. We note the ability to control the LRS resistance by varying the maximum current through each memristor. It is worth noting that this observation is in line with the work reported in [29].

D. Modifying & reading the state of anti-series memristors

In all the conducted measurements, we observed that current pulses with amplitude |0.2 uA| or higher, alway



(a)



(b)

Fig. 5 Anti-series memristors. (a) A close-up view of experimental data presented in Fig. 4(a), showing the time-evolution of the voltage drop on the two anti-series devices during the first 1.5 s of the experiment. The inset focuses on the first pulse of 0.1 uA applied after the negative initialization pulse. (b) Experimental results from a series of incremental and decremental positive and negative current pulses, whose amplitudes were selected as 0.2, 0.4, 0.6, 0.8, and 1.0 uA, respectively. The curves correspond to the time- evolution of the voltage drop on the two devices.

induced a change in the state of the devices, regardless of their polarity, whereas |0.1 uA| amplitude did not affect their state. We highlight this observation revisiting the results shown in Fig. 4(a). Specifically, we show in Fig. 5(a) a close-up view of the response of the devices where we can observe what occurs when current pulses of 0.1 uA and 0.2 uA are applied. We focus on the first positive pulse groups, after a negative initialization pulse was applied. We do not observe any change in the state of the devices during the application of 0.1 uA current pulses, whereas a change occurs with the very first pulse of 0.2 uA, where the device M_B becomes more resistive than M_A. Likewise, we did not observe any change in the state of the devices during the application of -0.1 uA current pulses either (not shown here). Therefore, |0.1 uA| current pulses could be used to READ the state of the memristors, without disturbing the resistive combination of the CRS configuration.

We conclude this preliminary exploration of the behavior of series and anti-series memristors with the results presented in Fig. 5(b). We already observed the amplitude-dependence of the final state of the memristors in previous experiments. Here, we rather used a sequence of incremental and decremental positive and negative pulses to figure out the effect of smaller amplitude current pulses when they are applied immediately after pulses of higher amplitude have been applied first. The current pulse amplitudes were selected in the range of amplitudes which we verified that were able to

trigger a resistive switching (RS) event, namely: 0.2, 0.4, 0.6, 0.8, and 1.0 uA, respectively.

The results validate the complementary switching behavior claimed previously. The decreasing (increasing) measured voltage values are indicative of the simultaneous decrease (increase) of the resistance of each one of the two devices. During the first half of the positive pulses, the voltage on device M_B is increasing w.r.t. the voltage on device M_A, whereas the opposite behavior is noticed during the first half of the negative current pulses, since here the device M_A undergoes a RESET process whereas the device M_B undergoes a SET process. For both polarities of the input signal, any significant modification of the state of any device is noticed only until the application of the higher positive (lower negative) current pulse. Afterwards, we do not see any change induced by the application of the remaining pulses whose amplitude is lower than |1.0 uA|. The latter validates the amplitude-dependence of the final state of the memristors when current-based driving schemes are employed.

IV. Conclusions

The results presented in this work demonstrated the feasibility of current-based driving applied to networks of memristors connected in series, both with the same and with the opposite polarities. Our observations motivate the design and experimental implementation of solutions exploiting the CRS configuration in current-driven schemes for memory and computing applications, which could be tested using commercially available memristors, creating opportunities for new R&D tracks in this field. On-going work will focus on the key CRS operation proposed elsewhere for memory and logic applications, which is the case when the CRS is brought to the {LRS-LRS} intermediate combination; i.e., when only one device is forced to switch its state from HRS to LRS, while the other remains unaffected. This behavior was previously proposed for destructive READ out of the CRS state encoding binary information, as well as for logic XOR gates and for composite multi-level resistive switches [14], [30]. The current-based driving conditions required to achieve the intermediate CRS state combination, will be investigated next.

References

[1] D. Ielmini, "Resistive switching memories based on metal oxides: mechanisms, reliability and scaling," Semicond. Sci. Technol., vol. 31, no. 063002, 2016

[2] IntrinSic, "Revolutionary Embedded Memory," [Online]. Available: https://www.intrinsicsemi.com/

[3] J. Gomez, I. Vourkas, and A. Abusleme, "Exploring Memristor Multi- Level Tuning Dependencies on the Applied Pulse Properties via a Low Cost Instrumentation Setup", *IEEE Access*, vol. 7, pp. no. 1, pp. 59413 – 59421, 2019

[4] Y. V. Pershin and M. Di Ventra, "Self-organization and solution of shortest-path optimization problems with memristive networks," *Phys. Rev. E*, vol. 88, no. 1, p. 013305, Jul. 2013

[5] A. Madhavan, and M. D. Stiles, "Storing and Retrieving Wavefronts with Resistive Temporal Memory," 2020 *IEEE International Symposium on Circuits and Systems* (*ISCAS*), Seville, Spain, Oct. 12- 14

[6] I. Vourkas and G. Ch. Sirakoulis, "Emerging memristor-based logic circuit design approaches: A review," *IEEE Circuits Syst. Mag*., vol. 16, no. 3, pp. 15–30, Third Quarter 2016

[7] B. Hoffer, V. Rana, S. Menzel, R. Waser, and S. Kvatinsky, "Experimental Demonstration of Memristor-Aided Logic (MAGIC) Using Valence Change Memory (VCM)," *IEEE Trans. on Electron Devices*, vol. 67, no. 8, pp. 3115 - 3122, 2020

[8] J.-W. Ryu, and K.-W. Kwon, "A low power selector-less crossbar array with complementary resistive-switching memory," 2016 *IEEE Int. Conference on Electron Devices and Solid-State Circuits* (*EDSSC*), Hong Kong, China, Aug. 03-05

[9] I. Vourkas, and G. Ch. Sirakoulis, "Nano-Crossbar Memories Comprising Parallel/Serial Complementary Memristive Switches," *BioNanoSci*., vol. 4, no. 2, pp. 166-179, 2014

[10] G. Papandroulidakis, I. Vourkas, N. Vasileiadis, and G. Ch. Sirakoulis, "Boolean Logic Operations and Computing Circuits Based on Memristors," *IEEE Trans. Circ. Syst. II: Exp. Briefs*, vol. 61, no. 12, pp. 972-976, 2014

[11] A. Siemon, S. Menzel, R. Waser, and E. Linn, "A Complementary Resistive Switch-Based Crossbar Array Adder," *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 5, no. 1, pp. 64-74, 2015

[12] I. Vourkas, and G. Ch. Sirakoulis, "Study of Memristive Elements Networks," *J. Nano Research*, vol. 27, pp. 5-14, Mar 2014

[13] A. Ascoli, *et al*., "History Erase Effect in a Non-Volatile Memristor," *IEEE Transactions on Circuits and Systems—I: Regular Papers*, vol. 63, no. 3, March 2016

[14] C. Fernandez, I. Vourkas, and A. Rubio "Shortest Path Computing in Directed Graphs with Weighted Edges Mapped on Random Networks of Memristors", *Parallel Processing Letters*., vol. 30, no. 1, pp. 2050002, Mar. 2020

[15] I. Vourkas, A. Batsos, and G. Ch. Sirakoulis, "SPICE modeling of nonlinear memristive behavior," *Int. J. Circ. Theor. Appl*., vol. 43, no. 5, pp. 553–565, May 2015

[16] I. Vourkas, and G. Ch. Sirakoulis, "On the Generalization of Composite Memristive Network Structures for Computational Analog/Digital Circuits and Systems" *Microelectronics J*., vol. 45, no. 11, pp. 1380-1391, Nov. 2014

[17] F. Di Francesco, G. A. Sanca, and C. P. Quinteros, "Spatiotemporal evolution of resistance state in simulated memristive networks," *Appl. Phys. Lett*. 119, 193502, 2021

[18] M. A. Nugent, T. W. Molter, "Thermodynamic-RAM technology stack," *Int. Journal of Parallel, Emergent and Distributed Systems*, vol. 33, no. 4, pp. 430-444, 2018

[19] H. Lv, *et al*., "Voltage driving or current driving: Which is preferred for RRAM programming?," 2011 *Int. Symposium on VLSI Technology, Systems and Applications*, Hsinchu, Taiwan, Apr. 25-27

[20] H. Garcia, S. Dueñas, O. G. Óssorio, H. Castán, "Current Pulses to Control the Conductance in RRAM Devices," *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 291–296, 2020

[21] A. Cirera, B. Garrido, A. Rubio, and I. Vourkas, "Effective Current- Driven Memory Operations for Low-Power ReRAM Applications", *IEEE Access*, vol. 11, pp. 51260 – 51269, 2023

[22] A. Cirera, I. Vourkas, A. Rubio, and M. Perez, "Stochastic Resonance Exploration in Current-driven ReRAM Devices," 2022 *IEEE Int. Conf. on Nanotechnology* (*NANO*), Palma de Mallorca, Spain

[23] E. Pescio, A. Ridi, A. Gliozzi, "A picoampere current generator for membrane electroporation," *Rev. Sci. Instrum*., vol.71, no. 4, pp. 1740, 2000

[24] K. A. Campbell, “Self-directed channel memristor for high temperature operation,” *Microelectron. J*., vol. 59, pp. 10-14, Jan. 2017

[25] Knowm Inc., [Online]. Available: https://knowm.org

[26] J. D. Prades, *et al*., “Ultralow power consumption gas sensors based on self-heated individual nanowires,” *Appl. Phys. Lett*., vol. 93, no. 12, pp. 123110, 2008

[27] A. Cirera, C. Fernandez, I. Vourkas, and A. Rubio, “Exploring Different Circuit-level Approaches to the Forming of Resistive Random Access Memories,” 2022 *Int. Conf. on Modern Circuits and Syst. Technol.* (*MOCAST*), Bremen, Germany

[28] T. Wang *et al*. “Electroforming in Metal-Oxide Memristive Synapses”, *ACS Appl. Mater. Interfaces*, vol. 12, pp. 11806-11814, Feb. 2020

[29] M. H. Li, *et al*., "Self-compliance SET switching and multilevel TaOx resistive memory by current-sweep operation," 2014 *Annual Non-Volatile Memory Technology Symposium* (*NVMTS*), Jeju, Korea (South), Oct. 27-29

[30] I. Vourkas, A. Abusleme, G. Ch. Sirakoulis, and A. Rubio, “1-D Memristor Networks as Ternary Storage Cells,” 2016 *Int. Workshop on Cellular Nanoscale Networks and their Applications* (*CNNA*), Dresden, Germany, Aug. 23-25