

EKV MOS Transistor Model For Ultra Low-Voltage Bulk-Driven IC Design

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Abstract—The paper addresses a development and evaluation of well-known EKV MOS transistor model with focus on the ultra low-voltage / ultra low-power analog IC design employing rather “exotic” *bulk-driven* technique. The presented contribution can be viewed as an extension of already established compact simulation model with modifications to the original parameter extraction flow. The article contains a brief description of EKV model fundamentals, a novel parameter extraction flow and most importantly, the comparison of developed EKV model with the foundry-provided BSIM model (v3.3) and the experimental measurement data obtained from prototype chip samples fabricated in 130 nm CMOS technology.

Index Terms—Bulk-Driven, Ultra Low-Voltage, Low-Power, EKV Model, Analog IC Design

I. INTRODUCTION

The current scaling of MOS transistors is governed by very well-known Moore’s law [1]. The emerging FinFET and GAAFET CMOS technologies are exceptional in terms of power efficiency per area, the scale of integration and the maximum operating frequency [2]. However, they also introduce numerous issues for the designers and process engineers. First of all, the process variations and aging effects are becoming more and more substantial and in the current mass-production technology node (5 nm FinFET, as of 2021), the behavior of transistors is gradually becoming stochastic rather than deterministic. This undesired effect will be even more pronounced in the following process nodes, such as 3 nm, in the near future. From the circuit designer’s point of view, the transistors produced by the cutting-edge technologies are optimized for switching purposes and are therefore, predestined mainly for high-performance (and expensive) digital systems.

Analog / Mixed signal ICs are still being designed in rather mature CMOS processes using planar transistors, such as 65 nm and (much) higher. This is caused by significantly lower cost, lower fabrication process dispersion, voltage levels used and the overall transistor properties, in general. Moreover, the mature process nodes contain high quality circuit components vital for analog design, such as resistors, capacitors, varactors, inductors, etc.

The current trend of employing very low power supply voltages and lowering the overall power consumption is also supported by the recent boom of battery-powered electronic

devices on the market. Furthermore, the requirements for minimized power consumption are more pronounced by the onset of on-demand IoT technology [3].

Any electronic circuit working with lowered power supply voltage or working in low-current regime, cannot be designed without accurate device models needed for simulations. There have been developed numerous compact MOS transistor models describing the properties and behavior using different description approaches. The model with most impact and success in the industry can be divided into three basic groups. The industry standard *Berkeley Short Insulated-Gate Model* (BSIM) model that has been used by the foundries for decades, is based on the threshold voltage definition (up to BSIM4 version) and has been primarily developed for strong inversion description (so-called *Quadratic model*) [4].

The second group is comprised of so-called *surface potential* transistor models, which describe the behavior based on the potential present on the Si-SiO₂ interface. Models like SP, PSP or MM belong into this family [5].

The third model group is based on the *inversion sheet charge* (ISC) present in the device’s channel. The best known MOS transistor models falling into this category are BSIM5 and higher, ACM and finally EKV [6]–[11]. Since the second and third model groups are newer, they are also more appropriate for nanoscale transistor modeling, which requires the description of rather complicated quantum effects, non-quasi static behavior, layout related effects, and so on. Their main advantage, however, lies in continuous modeling across the whole range of the input / output voltages and currents, as well as providing continuous derivatives of mentioned parameters. Thanks to this property, these models accurately describe the transistor behavior not only in the strong inversion but also in the sub-threshold region (weak inversion) and also in the area of smooth transition between these two regimes (also called *moderate inversion*).

The motivation for creating EKV model calibrated for weak and moderate inversion combined with the bulk-driven (BD) capability lies within the trend of lowering the voltage headroom in modern deep sub-micron technologies, as well as the necessity of inherently accurate compact model for ultra low-voltage / low-power analog IC design [12], [13].

II. EKV TRANSISTOR MODEL FOR BD CIRCUITS

A. EKV model fundamentals

The theoretical background of EKV transistor model has been extensively published in numerous scientific works in the past and it is not the scope of this article to describe the modeling approach in depth. Let us just briefly summarize the most important fundamentals, which are depicted in Fig. 1.

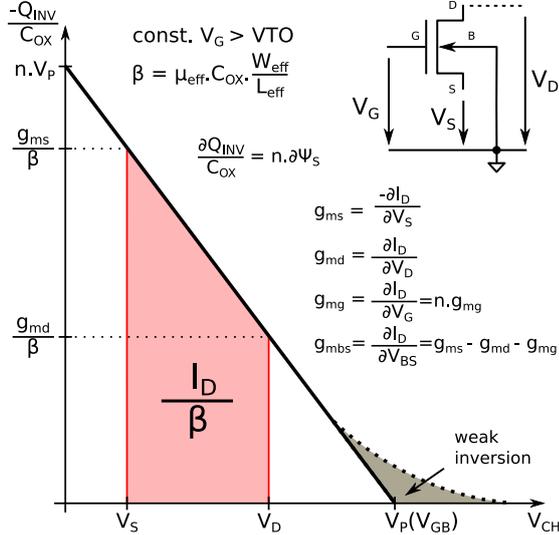


Fig. 1. The fundamental background of EKV MOS transistor model.

As one can observe, the drain current is determined as a definite integral of ISC across the MOS device channel. The crucial parameter, in this case, is so-called *pinch-off voltage* – V_P , which is in fact a function of voltage between the gate and *bulk* terminal. It denotes a value of V_{GB} when the ISC is zero in a non-equilibrium state.

Another crucial parameter is a normalization current, which is used for calculating the forward and reverse current, as well. Its name is *specific current* and it is defined by Eq. 1. The definition is comprised of a constant *technology current* and the scaling factor defined by MOS device geometry. The specific current also represents a condition when the current flow through the MOS device is consist of equal portions of drift and diffusion current.

$$I_{SP} = 2n \cdot \mu \cdot C_{OX} \cdot U_T^2 \cdot \left(\frac{W}{L} \right) = I_{TECH} \cdot \left(\frac{W}{L} \right) \quad (1)$$

The continuous modeling of ISC across the whole voltage range is expressed by so-called *inversion coefficient* (IC). One of its analytical definitions is shown in Eq. 2

$$IC = \frac{I_D}{I_{SP}} = \frac{I_D}{I_{TECH} \cdot \left(\frac{W}{L} \right)} = \ln^2 \left[1 + \exp \left(\frac{V_G - V_{TH}}{2n \cdot U_T} \right) \right] \quad (2)$$

In combination with g_m/I_D methodology, it represents the benchmark characteristics of EKV model for analog IC design as it depicts a continuous curve containing values of the drain

current combined with its derivative across the whole inversion range.

The value of threshold voltage (and V_P , as well) is dependent on V_{BS} , which in return, modifies the drain current. The simulation models and analytical formulas governing this phenomenon are usually focused on so-called *body-effect*, which is represented by increasing the threshold voltage due to increasing reverse voltage across the source-bulk diode. The opposite side of the body-effect is forward-biasing of the mentioned PN junction, which lowers the threshold voltage and therefore, increases the drain current. The drawback of this approach is two-fold. The bulk-driven transistor exhibits an input current draw, which is linearly dependent on device's area. However, its dependency on input voltage, as well as the temperature is exponential. The second disadvantage is the risk of catastrophic latch-up effect, which will occur when the forward voltage across the PN junction exceeds the turn-on level. The latter is the main reason, why the application field of bulk-driven design techniques is quite limited and still represents an attractive research topic. As mentioned before, $V_{DD} = 0.4$ V effectively eliminates the risk of latch-up effect even at high operating temperatures.

B. The proposed extraction flow

EKV model (v2.63) contains only about 30 internal parameters, which govern the modeled electrical behavior. In order to obtain the values for each parameter, the extraction from manufactured stand-alone transistor samples needs to be carried out [14], [15]. The original extraction sequence has been modified, in order to incorporate the effects of forward-bias of the source-bulk diode on MOS transistor properties. The proposed extraction flow is depicted in Fig. 2. First of all, we completely omit the narrow / short device modeling, since these are rarely used in *analog* IC design due to high dispersion of their electrical properties. The second proposed modification is formed by omitting the *impact ionization* parameters extraction. With $V_{DD} = 0.4$ V, the discussed effect will not occur, hence we can leave the according model parameters at their default values. The third modification is introduced by extracting the model parameters for narrow / long MOS device after the wide / long one. This way, we will obtain a complete set of model parameters for long-channeled devices, which are predominantly used in ultra low-voltage and/or low-power analog circuit design. Furthermore, we can fine-tune their values by iterating between measured and simulated results of output and transfer characteristics of given MOS devices. The parameters modeling the short-channel and temperature effects can be extracted afterwards.

The fourth update to the original extraction sequence is introduced by measuring classic transfer characteristics of the transistor with stepped V_D . The fifth and the final change is the introduction of stepping the bulk voltage in *both* directions from the substrate in extraction setups SETUP2 and SETUP3. Naturally, this requires a twin-well fabrication process, to be able to bulk-drive both types of MOS transistors.

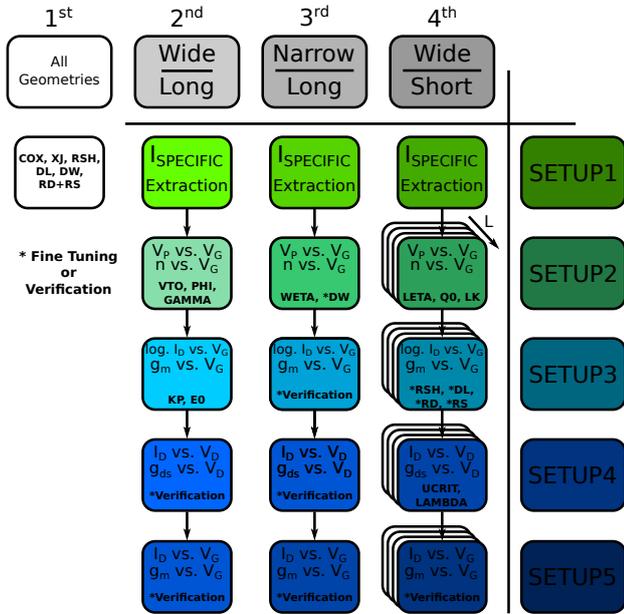


Fig. 2. The proposed extraction flow of EKV model parameters for BD design.

After the I_{SP} extraction, one would proceed to pinch-off voltage measurement (SETUP2 in Fig. 2) and extract the parameters responsible for sub-threshold current slope modeling and the threshold voltage itself [16]. However, we propose a novel measurement setup shown in Fig. 3. The transistor is biased into a moderate inversion, while being kept in saturation. The bulk voltage is stepped from the maximum body-effect towards the maximum forward-bias, which in our case was $V_B \in \langle -0.4 \text{ V}, +0.4 \text{ V} \rangle$. The gate voltage V_G is swept between 0 V and 0.4 V.

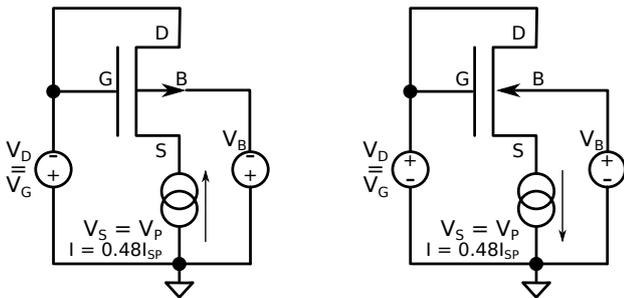


Fig. 3. The proposed pinch-off voltage measurement setup for bulk-driven transistor model.

This way, we can still extract the parameter values as in the original experiment ($V_B = 0 \text{ V}$), but we also can directly verify the accuracy of all extracted model parameters and re-iterate, if needed.

The measurement setup for extracting the parameters governing the maximum transconductance and velocity saturation – SETUP3 is shown in Fig. 4. The device is biased

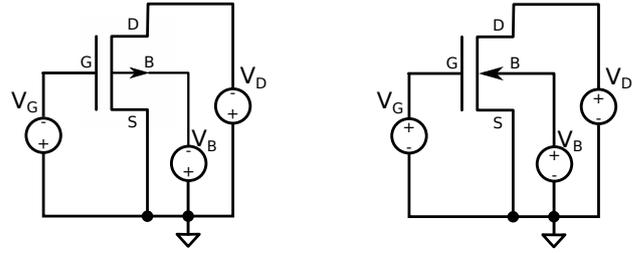


Fig. 4. The proposed extraction of transconductance and velocity saturation for bulk-driven transistor model.

into the linear regime and V_G is swept, while the bulk voltage is, again, stepped in both directions.

The experimental measurements named SETUP4 and SETUP5 represent the means to obtain classic output and transfer characteristics, respectively. Output characteristics will be used to obtain model parameters responsible for the saturation region and channel modulation. The data from SETUP5 will not be used for extraction, but are invaluable for overall fine-tuning and testing of the model as a whole.

The proposed extraction flow ensures correct modeling of bulk-driven transistor in ultra low-voltage conditions and also simplifies the original sequence thanks to discussed approximations. The re-ordering of the steps in the original extraction flow is a matter of personal preference, but we believe that the proposed extraction sequence is more logical and reduces the overall time required for convergence to the final model parameter values.

III. EXPERIMENTAL RESULTS

The measurements have been carried out on 25 individual prototype chips fabricated in general purpose 130 nm CMOS twin-well process containing both types of MOS transistors with 7 different $\frac{W}{L}$ ratios (7x NMOS and 7x PMOS) with their bulk terminals isolated from the substrate. The experimental measurement were set up according to Fig. 2, the silicon temperature was kept at constant value of $T = 27^\circ \text{ C}$. The experimental data have been processed by statistical analysis, which yielded characteristics of fast, slow and typical transistors, as well as basic Pelgrom's plots [17].

Fig. 5 depicts the comparison of the measured data of so-called *transconductance efficiency factor*, developed EKV model and the original BSIM model provided by the foundry. As expected, the EKV model exhibits superior accuracy across the whole inversion range, in this benchmark graph.

The results of the proposed extraction method named SETUP2 are depicted in Fig. 6. As expected, the stepped V_B causes shifting of the threshold voltage, as well as the pinch-off voltage slope. The black symbols and lines denote the conditions when $V_B = 0 \text{ V}$. The presented simulation results confirm the robustness of EKV model itself, but most importantly, a correct extraction procedure of respective model parameters. The worst-case discrepancy of this experiment is below 1%. Fig. 7 shows a direct comparison of the developed EKV model, foundry-provided BSIM model and experimental data

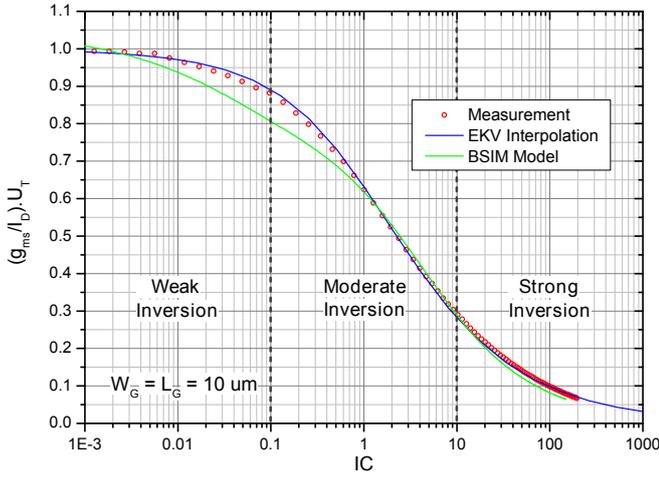


Fig. 5. Transconductance efficiency factor versus inversion coefficient.

of SETUP3 gathered from the nominal MOS transistor. Again, the black symbols and lines determine the conditions, when the bulk is shorted to the source terminal. At first glance, we observe significantly better correlation of EKV model, especially with bulk being in forward-bias conditions and weak inversion. The worst-case discrepancies have been calculated at -10.64 % and -60.27 % for EKV and BSIM model, respectively. It should be noted, that the agreement of EKV model could be improved, but it was sacrificed for the overall accuracy of the model within the specified $\frac{W}{L}$ ranges. The output characteristics of the nominal MOS transistor are shown in Fig. 8, in semi-logarithmic scale, in order to display the agreement across the whole gate voltage range. Namely, we stepped the gate voltage from zero to $V_G = 0.4$ V. One can observe better accuracy of EKV model, especially with V_G set close to the range of moderate inversion. The worst-case discrepancy has been calculated at -12.51 % for EKV model and -22.61 % for BSIM model.

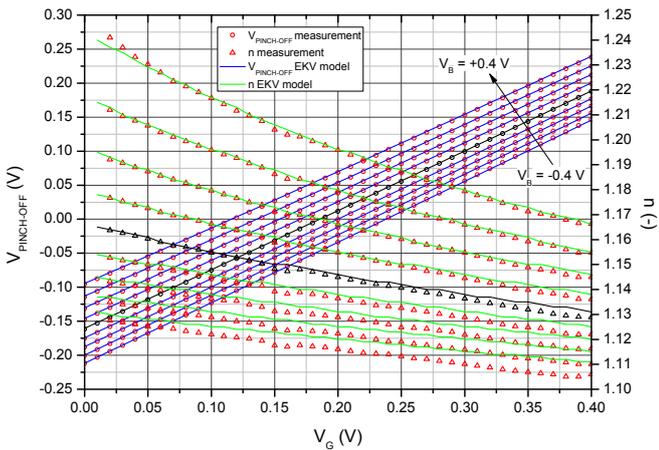


Fig. 6. Measurement and simulation results of BD pinch-off voltage and substrate factor n .

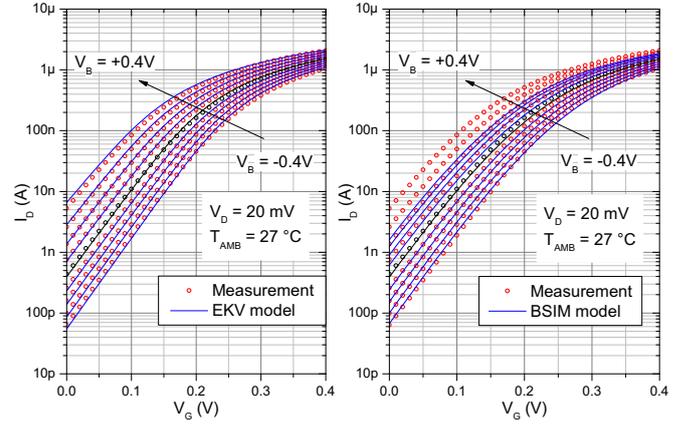


Fig. 7. Measurement and simulations of the proposed "bulk-driven" SETUP3.

The results of the last experiment, classic transfer characteristics – SETUP5 are depicted in Fig. 9. Again, it contains curves for both simulation models, as well as the measured data. We swept the gate voltage, while the drain voltage was stepped from $V_D = 50$ mV up to $V_D = 0.4$ V. The agreement of both models is quite satisfactory. However, EKV model exhibits better correlation in moderate inversion, again. The worst-case discrepancy in this case is 12.7 % for EKV model, while BSIM model exhibits deviation of -19.17 %.

The derivatives of all presented characteristics have been used for fine-tuning of the extracted parameters and were also analyzed for accuracy in each extraction step. The using of bulk-driven circuit design methodology also implies an update to the selection of relevant derivatives. The EKV model exhibits superior agreement with measured data, based on preliminary analysis. The discussed results should be published shortly. The displayed results prove a successful EKV model development with focus on BD circuits and low-voltage / low-power application area.

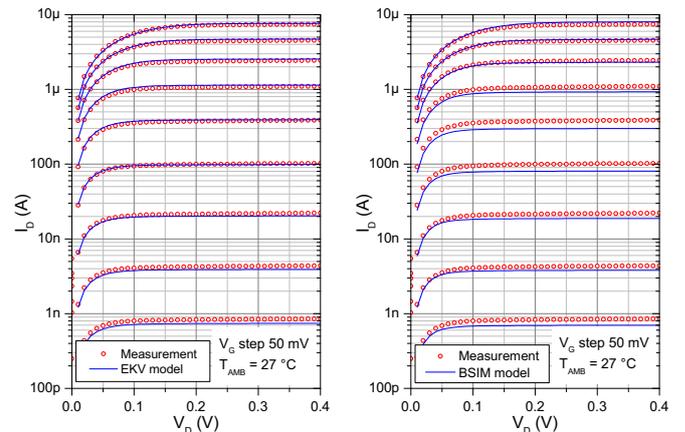


Fig. 8. Measured and simulated results of the output characteristics.

ACKNOWLEDGMENT

This work was supported in part by the Slovak Research and Development Agency under grant APPV 19-0392, Ministry of Education, Science, Research and Sport of the Slovak Republic under grant VEGA 1/0731/20, and by ECSEL JU under project PROGRESSUS (876868).

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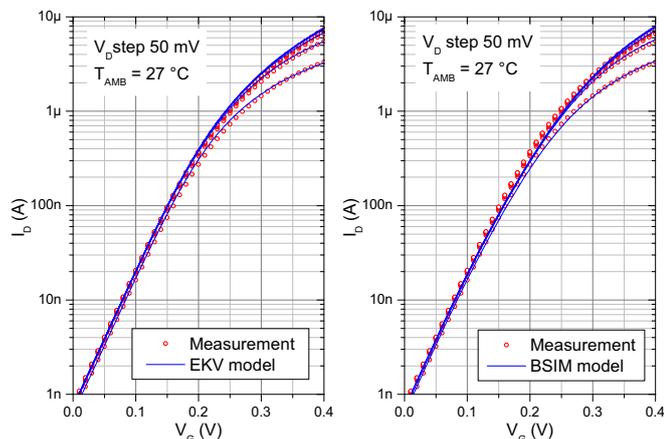


Fig. 9. Measured and simulated results of MOSFET transfer characteristics.

IV. CONCLUSION

We have developed a compact simulation model calibrated for ultra low-voltage / low-power analog IC design using the bulk-driven methodology. In order to achieve this, we have developed a novel extraction flow of EKV model internal parameters. The extraction sequence has been carried out on 25 prototype chip samples, each containing 7 different geometries (ranging from $L = 120 \text{ nm}$ to $L = 10 \text{ }\mu\text{m}$) of both transistor types (14 transistors per chip). The presented model exhibits superior accuracy to the foundry-provided BSIM (v3.3) model, in all relevant aspects of bulk-driven, as well as gate-driven analog IC design. Namely, the achieved refinement of model accuracy ranges from 6.47 to 49.63 percentage points. This promises a significant improvement in correlation between the simulation results and the measurement performed on fabricated ICs, in our future projects.

The developed EKV model, extracted and verified by the novel extraction flow, confirms the robustness and precision of EKV model itself, but most importantly, it expands its application into almost-uncharted area of ultra low-voltage / low-power analog IC design. The proposed extraction sequence itself introduces several approximations, which simplify and shorten the extraction process. It also modifies two key measurement setups with regard to bulk-driven design.

Our future plans include performing the extraction flow on another 25 chip samples. Naturally, we also plan to measure and extract the parameters responsible for modeling of the temperature-related effects. With the extraction flow in place and 50 analyzed chip samples, we intend to develop models for fast and slow transistors, as well. This will enable us to perform the Corner analysis and Monte-Carlo analysis, thus investigate the overall robustness of a IC during the design process. We will also develop EKV model calibrated for transistors designed with minimal channel length in given technology for accurate simulations of digital, pulsed or switching circuits, as well.