Testability Issues in Superconductor Electronics

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Abstract

An emerging technology for solutions in high-end applications in computing and telecommunication is Superconductor Electronics. A system-level study has been carried out to verify the feasibility of DfT in superconductor electronics. In this paper, we present how this can be realized to monitor so-called single-flux quantum pulses. As a part of our research, test structures have been developed to detect structural defects in this technology. We also show detailed test results of those structures. It proves that it is possible to detect possible random defects and provide defect statistics for the Niobium-based fabrication process.

1. Introduction

High-speed electronic devices in telecommunication and computing take the present semiconductor technologies beyond their limits. At this relatively immature stage, superconductor electronics is capable of handling these tasks as demonstrated by superconductor ADCs and microprocessor chips. As the complexity of the circuits has been increasing to about 5000 gates per chip [1], realization of the design as well as testing becomes a difficult task. Very little information is available on the methodology for achieving high yield as well as testing methodologies for superconductor electronics.

In electronic systems consisting of several thousands of gates, the trend is to introduce certain testability options at the design phase. Main goal of this DfT approach is to make the system testable at lower costs, and reducing the test time by increasing the ease of testing. This is desirable, as the system under study is complex; hence it is not possible to test all components directly with in the system. A DfT-based approach is essential for commercial production of complex reliable systems in SCE. As the complexity of the superconductor electronics (SCE) circuits has increased beyond 63,000 Josephson junctions (JJ) per chip as in the case of a Flux microprocessor chip [2], realization of a working design becomes an extremely difficult task. Very little information is available in literature on the methodology for achieving high yield for superconductor electronics. The yield levels turn out to be much lower than in the semiconductor industry due to the fact that little information is available on superconductor process defects.

We have developed special test structures to be realized along with the ICs for the JeSEF Nb process [3, 4]. These test structures were developed as a part of our Defect-Oriented Testing (DOT) approach on SCE [5]. The information gathered using these test structures are primarily used for yield analysis and DOT [6]. Fault models are being developed after studying the behaviour of the test structures. These fault models are then used for fault simulation of the circuit. From the data, potential defect-prone areas can be detected within the circuit and DfT structures can be introduced to monitor the status while employing the DOT approach.

In this paper, the possibilities of DfT for SCE circuits are discussed in view of the DOT approach. We also present measurement results from test structures that have been designed to detect the top-ranking defects that can occur in the JeSEF Niobium process.

The organization of the paper is as follows. The next section briefly explains IC testing followed by general DfT strategies in section 3. In section 4, the applicability of DfT to SCE is described followed by the proposed DfT structure for monitoring SFQ pulses. Measurement results on test structures are presented in the last section.

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2. Integrated Circuit Testing

Testing is the experimental analysis of a system. Along with the progress of IC technology, associated testing methodologies were developed to verify the realised design [7]. Detection of the nature and cause of the fault in the realised circuits is important for the commercial release of a product. The tests performed on an IC can be divided into two main categories: functional and structural. Introduction of additional circuitry is often required while performing structural testing. Functional testing is often simple and straightforward. But the generation of the correct test vectors for various faults is a difficult task and the faults are often indistinguishable while employing functional tests. Additionally, it is impractical for the ATE manufacturers to keep-up with the operating frequencies of the devices, making them unsuitable for at-speed testing as the operating frequencies of the devices are rapidly increasing.

On the other hand, for structural testing to be carried out, a systematic methodology has to be developed. Information about possible defects in the technology is gathered and fault models are developed for different probable faults. Specific test patterns are developed after a careful study of the structure of the circuit. Tests are carried out for a specific set of faults using the available fault models. Hence, the nature and cause of the detected fault is known. Another major advantage of structural testing is that expensive ATE can be sometimes replaced with less expensive ones. Knowledge about probable defects and their statistics is an essential factor in carrying out structural tests. Information about random defects, occurring random in nature, is important because they contribute to the majority of the defects in a mature process. The most common defects that occur are shorts and opens in wiring layers, via defects and pinholes in oxide layers. Cracking of metal layers is another issue, which, in the worst case, can become an open in the layer.

The effective detection of these defects in a manufacturing process are carried out using specially designed test modules also called Process Defect Monitors (PDM), which consist of a number of test structures. Of the different kinds of PDMs, those used for the determination of the structural-defect distribution (short, breaks etc.) is useful for the current study on structural testing. The information gathered using this structure is the basis for DOT. A defect ranking is used to create a realistic fault list. Faults are resulting from defects that cause malfunctioning of the realised circuit in the technology under study. Fault models are then developed to translate the defect information into the circuit under study for simulation.

3. Design for Testability

A fault is said to be testable if there exists a well-specified procedure to expose the fault. Similarly a circuit is testable with respect to a fault set when each and every fault in this set is testable. Design for Testability (DfT) refers to those design methodologies which put constraints on the design process to make test generation and application cost-effective.

In general, by means of DfT, controllability and observability of the design is improved. There are two classes of DfT techniques – ad-hoc techniques and structured techniques. Most approaches require circuit modifications and factors such as chip area, IO pins and delay are affected. Usually these factors increase when DfT techniques are applied.

Hence a critical balance exists between the attainable gain and the applicable DfT.

4. Design for Testability for SCE

Design for testability is a desirable option for SCE due to the fact that the circuits work at ultra-high frequencies and very low temperatures. Because of these operating conditions, the set-ups required for testing the realised circuits are bulky and expensive. After realising this drawback, researchers have started working on testability of SCE circuits [2, 9], but a DfT approach in SCE is still in its infancy. Until now, tests carried out in SCE are mostly *functional* in nature. But details of the defect that caused the fault in the device are not trivial using functional approaches. At this point a DOT approach becomes attractive.

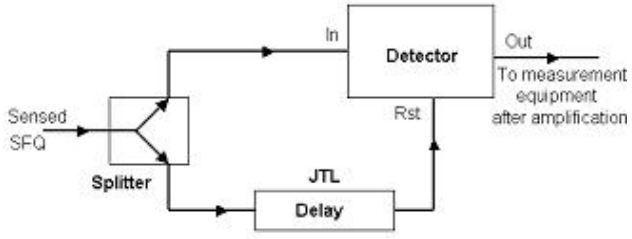

Figure 1. Block diagram of a structure for monitoring SFQ pulses in an RSFQ circuit.

Monitoring nodes, which are having a high probability of being faulty, in a circuit, is desirable while conducting DOT. It is extremely difficult to monitor an SFQ pulse in a circuit due to its basic properties. In this paper, we

propose a new scheme by which detection of an SFQ pulse inside a circuit is possible.

Figure 1 shows the block diagram of the proposed scheme. It consists of simple SCE circuit elements like splitter, JTL delay line and a specially designed detector for the SFQ pulse. This structure is attractive in finding faults within a circuit where direct pulse monitoring is not possible. The SFQ pulse to be sensed is split and one part is applied directly to the input of the special detector circuit. The other pulse is applied to the reset input of the detector via a delay segment. By measuring the voltage at the output of the detector, the presence of an SFQ pulse can be detected.

The delay segment determines the duration of the voltage level at the output of the detector. The delay can de made sufficiently long before the reset of the voltage state. As a result, less expensive external test equipment can be triggered using the amplified signal from the output of the detector. A JTL is used in the design to construct a delay line for this purpose. The output of the detector has to be amplified to be able for the external equipment to detect the signal. The circuit diagram of our designed pulse detector is given in Fig. 2.

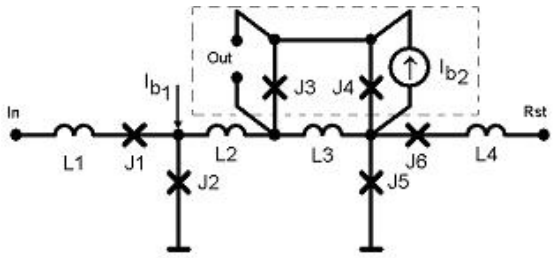

Figure 2. Circuit diagram of the detector used in the SFQ pulse monitor.

It is a modified form of a readout SQUID connected to a Set-Reset Flip-flop (SRFF). Arrival of an SFQ pulse on the "In" terminal will set the FF by trapping a fluxon in the J2-L2-L3-J5 loop. This in turn set the JJs, J3 and J4 into a sequential switching mode. The average voltage across the junction can be measured after necessary amplification. This can be implemented on-chip or off-chip according to design specifications. Arrival of an SFQ pulse at the "Rst" terminal will reset the SRFF and the fluxon that is trapped escapes out of the loop. This in turn reset the sequential switching of J3 and J4s reducing the average voltage across them to zero.

Fig. 3 shows the operation of the detector circuit.

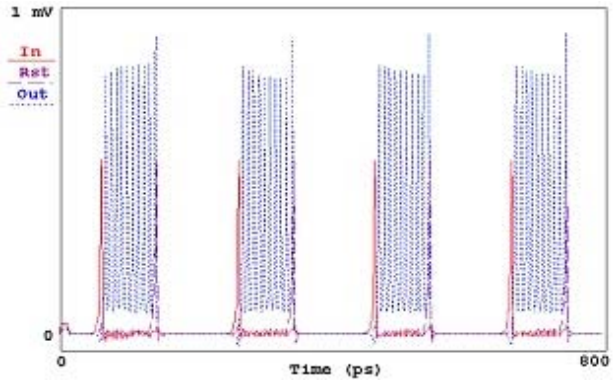

Figure 3. Operation of the detector circuit designed for monitoring SFQ pulses.

To illustrate the insertion of the DfT structure into a circuit, we take a part of an RSFQ circuit as example CUT. This is shown in figure 4.

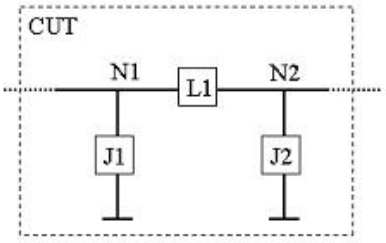

Figure 4. Schematic diagram showing part of the example CUT.

The part under study consists of two JJs, J1 and J2 at nodes N1 and N2 respectively and an inductance L1 between the nodes N1 and N2. In this case, the node that is to be observed is taken as N1. This can be approached in two ways. The first method is to use a splitter to insert the DfT structure into the CUT. The implementation is as shown in Fig. 5, the additional structure is shown shaded.

The SFQ pulse arriving at N1 is split into two – one is fed back into the remaining part of the original CUT and the other to the input of the DfT structure.

This method introduces a delay, which is equivalent to that of the splitter into the original CUT. This has to be taken into account if the system has a critical delay in the path in which the structure is inserted. This can be overcome by using the second technique.

Here, an inductance is used to couple L1 to the DfT structure to sense the current flowing through it as shown in Fig. 6.

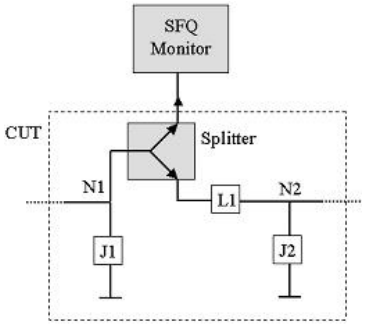

Figure 5. Schematic diagram showing the insertion of the monitor into the circuit-under-test (CUT) using a splitter.

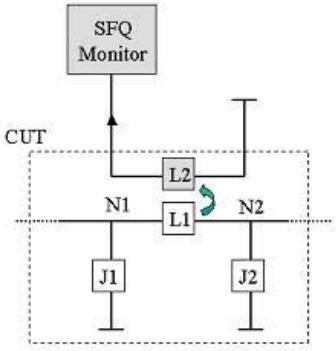

Figure 6. Schematic diagram showing the insertion of the monitor into the circuit-under-test (CUT) by coupling inductance.

Special measures have to be taken so that no external current from the DfT structure flows back into the CUT through the coupling inductance L2. A unidirectional JTL can be used if necessary in the design. All delays of the original CUT will remain unchanged.

The proposed DfT structure was inserted into an XOR gate as CUT. The circuit was then tested using JSIM simulations. Various nodes were monitored and the results showed that the scheme is feasible. Fig. 7 shows the simulation result of the monitor while using it to monitor the input node of the XOR gate. In this case, input A was monitored. This scheme is useful, especially while conducting DOT for verification of fault models. Furthermore the area overhead is less while implementing the design as only a few JJs are added by the structure. Built-in-self-test (BIST) will probably the ultimate test solution for complex RSFQ circuits [10].

5. Test structures and Defect Analysis

Until now, most research has been carried out to detect and reduce parametric defects in superconductor processes and the functional verification of devices. As the processes have become more matured, the importance of detecting structural defects has increased. This is due to the fact that the occurrence of gross manufacturing errors and deviation of parametric values are decreasing due to the maturity of the process. However, random defects can still occur due to various reasons like the presence of impurities, local wafer defects and human errors.

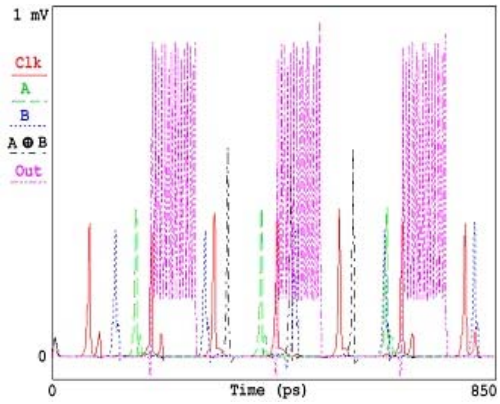

Figure 7. Output of the monitor connected to one of the inputs (A) in an XOR.

As a result of our earlier research on structural defects in the JeSEF RSFQ process [4], a test chip has been realised for a detailed process analysis. Two types of structures were designed, one set for low temperature (LT), 4 K testing and the other for room temperature (RT), 294 K testing. More detailed information about the test structures is available in Ref. [6]. The results from these structures serve two purposes:

1. Statistical information on defects for DOT and Yield analysis.
2. The determination of potential defect-prone areas for monitoring using a DfT structure in DOT.

Twenty-seven possible defects were theoretically predicted for this process. These defects have been grouped and ranked into a list of probable defect locations. Classification of the structural defects for the LTS RSFQ process is given in Table 1. The list has been prepared by considering the following facts: the frequency of occurrence of the weak-spots and the topology of the defects. The junction defects are primarily due to the thin oxide barrier of the JJ. Metal layer defects occur due to step-coverage problems, critical dimensions and large pinholes in the isolation layers. Metal-layer defects cause intra-layer shorts due to extra material or inter-layer shorts due to isolation-layer problems. Cracks occur due to step-coverage problems in the under-lying layers. Metal-to-resistor contact problems are the primary

cause in case of resistor layers. Both opens and shorts occur in this layer.

TABLE I. Classification Of Structural Defects in an LTS Tri-layer process

No.	DEFECT TYPE	Nature of the defect
1.	Junction defects	Shorts, opens, excessive size and number of pin holes in the thin oxide layer.
2.	Metal layer defects	OPENS OR NEAR OPENS, CRACKS AND SHORTS IN THE METAL LAYER
3.	Resistor defects	Contact resistance problems, opens or near opens and shorts in the resistor layer.
4.	Isolation defects	Shorts and opens between layers, defects in vias.

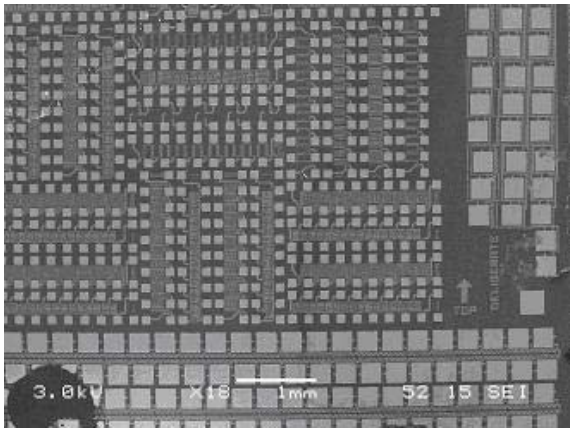

Figure 8. SEM photograph of part of the test chip; location of the RT structures are in the centre and LT structures at the periphery for easy access for testing.

A SEM photograph of a part of the test chip that has been realised in the JeSEF process is shown in Fig. 8.

The two types of structures, LT and RT, reduce the unnecessary complexity in the testing phase and test-running costs. The 4 K structures can be seen at the edge of the chip. They have been placed for easy bonding access. The RT structures are positioned at the centre of the chip, which can be accessed by the contacts of an automatic probing machine.

Low temperature measurements are carried out at 4.2 K. The designed test structure is a modification of the long-chain I-V curve measurements in JJs. Originally they were proposed [11, 12, 13] for detecting parametric variations in a process. A model has been developed that has helped to create a method for detecting and pinpointing possible junction defects down to a chain of 20 JJs. The detection method has been developed to reduce the number of thermal cycles needed, thus reducing test cost and test time [4].

The basis for the RT measurements is forcing a current and measuring the voltage at fixed power dissipation. A semi-automatic probe station is used for this purpose. A four-point scheme is being used so that more accurate measurements can be carried out. The chip is placed in the probe station and appropriate test routines are loaded. The measurement data is stored in an output file for analysis. This file is then subjected to analysis, resulting in a list of locations of structures that are defective. The subsequent location in the chip is further optically analysed to confirm the defect.

Metal-layer defects are detected using a structure in which the metal runs over repeated steps of the underlying layers [14]. At room temperature, the resistance of this path is measured and compared with the resistance of a reference path, called “v/d Pol structure” [15], with the same layout, though without the steps of the underlying layers. Deviations from the average measured resistance ratio will reveal opens or near opens in any of the test structures.

To illustrate the analysis, we are presenting the details of one structure in this paper. It is the one that has been designed to test for the second metal wiring layer (M2) defects over a via to the first metal layer (M1). The layout of the structure is given in Fig. 9.

The step as result of the via was emulated by removing the corresponding isolation layers to form the test structure. This prevents detecting multiple defects in the structure. More details of the structure is given in Ref. [16].

One of the detected defects is shown in Fig. 10. A crack in M2 resulted in a high resistance of the segment. A database is being prepared with the results from these test structures. Chips from different process runs are being measured for this purpose. An extensive analysis is required after the preparation of the database to bring out a ranking list for the defects and creation of a fault list for the SCE process under study. Translation of the defect behaviour from RT to LT is the next step in our fault-model development.

The defect statistics obtained from the above test structures will be used for IFA. Depending upon the type of defect occurring in the processed circuit, it can be classified as semiconductor-like defects and special

defects that apply to superconductor circuits only.

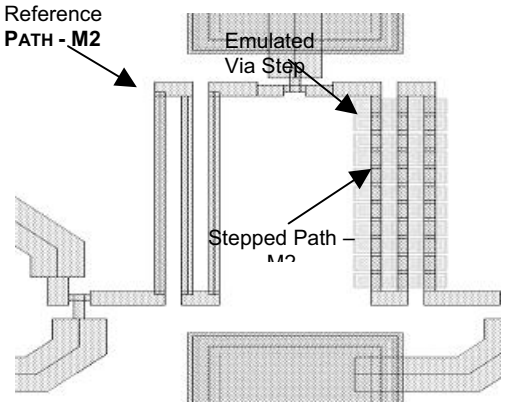

Figure 9. Part of the layout of the structure for the detection of defects in M2 layer for step-coverage problem over a via.

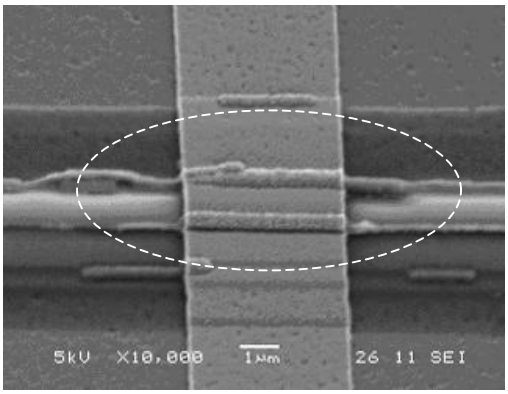

Figure 10. SEM photograph of a detected defect using the designed test structure for the detection of defects in the JeSEF process; location of the defect is the Niobium wiring layer over a step as result of the via.

Resistive bridges and shorts are examples of semiconductor-like defects that can occur in the circuit. Shorts in a JJ are an example of the second kind. Our early study on this subject was published in reference [5]. Some faults were especially induced in the developed test structures and will be used to validate the results of those studies.

6. Conclusions

In this paper a possible DfT scheme for monitoring SFQ pulses within an RSFQ circuit has been discussed. A DfT scheme is inevitable for RSFQ circuits because of their very high frequency of operation and extremely low operating temperature (4 degrees Kelvin). We have demonstrated how SFQ pulses can be monitored at an internal node of an SCE circuit. The available features in the proposed design for customising the detector make it attractive for a detailed DOT of RSFQ circuits. Analysis on the test structures that have been developed for DOT of the JeSEF process proves that our structures are capable of detecting the probable defects. The defect statistics obtained from the above test structures will be used for IFA, a DOT methodology, of SCE circuits. Fault models will be verified using the DOT methodology. Generation of the required test vectors for carrying out the structural test will be available after the time-consuming IFA.

Much work is still remaining regarding this part of DOT for superconductor electronics, which is essential for a structural testing methodology for RSFQ circuits.

7. References

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