

# (Some) Open Problems To Incorporate BIST In Complex Heterogeneous Integrated Systems

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**Abstract**-- This paper presents an overview of test techniques that offer promising features when Built-In-Self-Test (BIST) must be applied to complex integrated systems including analog, mixed-signal and RF parts. Emphasis is on techniques exhibiting a good trade-off between test requirements (basically in terms of signal accuracy and frequency) and test quality.

## I. INTRODUCTION

Testing is an activity strongly constrained by the evolution of both design techniques and technology changes. Then, in order to foresee future challenges in testing non-digital integrated circuits and systems, it is essential to consider these in connection with what may be forecast in design and technology. There are two main driving forces when considering a futuristic view of non-digital test. First of all, the way technology is scaling down and its impact on analog and RF design techniques. Second, the main application fields where circuits will play a significant role. Regarding the latter, RF transceivers, single-chip Microsystems, re-configurable subsystems, are examples of different categories recognized nowadays as important. Regarding the former, problems related to non-ideal effects, to the use of non-conventional devices or to nano-devices are among the most significant ones.

Nowadays complete and very complex systems are integrated on one single die. By far the largest portion of that is in the digital part of the system, which usually contains Multi-core GHz Processors, multiple Mbytes of memory, Media Access Controllers (MAC) and several dedicated Digital Signal Processors (DSP). Examples can be found in consumer applications like Cellular phones, DVD players, Multi-media players and so on. A general conceptual scheme for the architectures of these present and future systems can be that in Figure 1, where any wireless-based application is conceptually covered. As shown in the typical example of Figure 1, these systems usually contain one or multiple Analog Front-Ends (AFE), Analog Back-Ends (ABE), as well as RF Receive and Transmit functions. One of these SoCs is a combination of the so-called "More Moore" and "More-than-Moore" technologies.

This paper aims to give a glimpse on the problems arising when BIST (Built-In-Self-Test) is to be used in systems like that in Figure 1. Besides the digital components, there are two main focus of attention: a) the baseband analog components, and b) the RF parts. Every one has each own specificity; however, it should be essential to combine them if effectiveness is looked for.

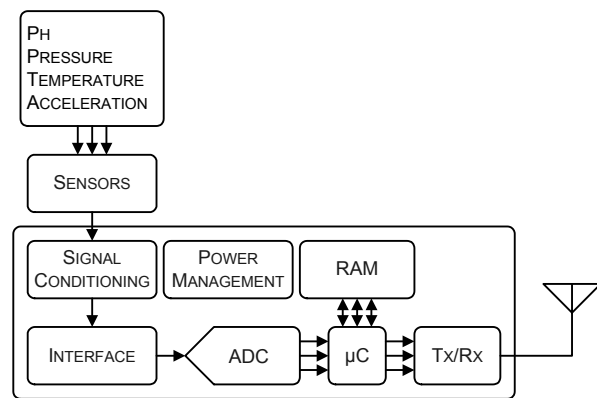


Fig. 1: Generic SoC View

## II. TESTING SOC'S: NON-DIGITAL BIST PROBLEMS

Applying BIST to the digital part of a SoC is not difficult as we have available many alternatives broadly proven in practice, all of them based on defect test. On the other hand, when analogue BIST has been considered, it is from a theoretical perspective a simple extension of its digital counterpart. In that sense, a general scheme for testing a complex SoC will be as the one shown in Figure 2. Converting such a scheme to provide BIST functions just require to move generators and digitizers into the chip. However, this is in practice almost unfeasible due to the strict requirements imposed by the analogue circuitry.

From the point of view of structure, re-using and re-routing are essential for BIST. For example, in the case of DACs the situation is very nice if Direct Digital Frequency Synthesizer (DDFS) is available to generate the

tones needed for testing. Then, only a test-pin is needed for the analog output signal as well as a Spectrum Analyzer to process the output signal. When a DDFS is not already available in the digital system, that function is often integrated additionally for test-purposes only. In modern CMOS processes the size of a DDFS is so small that cost is no longer a reason not to do this. In the case of the ADC, memory can be placed on chip to capture a certain amount of data that, subsequently, can be read out at a much slower pace, through test-pins. However, this cannot always be done due to the constraints imposed by the accuracy and speed of the ADC.

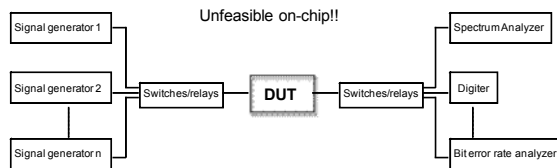


Fig. 2: Test set-up

However, in real life the situation is not so simple. Analog (and consequently mixed-signal) circuits are usually tested by measuring their functional specifications. This means the need for many different measurements with severe accuracy constraints. The heterogeneity of the analog blocks in terms of testing their specs affects in terms of frequency, accuracy, signal integrity, extra power, etc.

Taking this in mind, the conceptual view in Figure 2 is not feasible to be applied on-chip with the typical requirements imposed by analog and RF components since it would be necessary to combine signal generators ranging from the baseband frequency up to the radio frequency. Furthermore, some (if not all) generators do need an accuracy similar or higher than the ADCs and DACs available within the SoC.

In order to be able to apply the BIST concept, there are some ideas worth exploring:

- adapting the existing test techniques by paying the price of a reduced test accuracy.
- developing new techniques relaxing the accuracy constraints imposed by the analog circuits.
- introducing techniques not relying on spec testing and thus not requiring specific stimuli (or even any stimuli at all).

In what follows we try to consider the potential usefulness of these ideas keeping in mind the interest of combining them for RF and baseband signals.

### III. TESTING THE BASEBAND COMPONENTS

Going back to Fig. 1, the trend is to keep the analog circuitry to a minimum, pushing to the digital domain whatever is possible. The minimum required mixed-signal function is an ADC (typically, more than one). Usually a Track & Hold or a Sample & Hold

Amplifier (SHA) is preceding the ADC. For anti-aliasing or noise reduction purposes some form of Low-Pass Filtering (LPF) is implemented, although often just the natural poles of the other blocks are deemed sufficient. Active filtering is usually avoided as it is often simpler (as well as lower power and cost) to increase the sampling speed a bit to allow simple first-order filtering. A Programmable-Gain Amplifier (PGA) adjusts the incoming signal to optimally fit to the reference voltage of the ADC. Nevertheless, most testing requirements for the complete AFE rely on testing the ADC, since this is the crucial component. Depending on the system, it may be just one or even many, and the efficient test of this component is normally an important complement to any system-level technique. Testing ADCs is a topic broadly covered in past years. However, in connection with BIST, several new methods worth attention due to their potential to overcome the above-mentioned problems. In essence, among those new methods, it is worthwhile to mention:

- those relaxing input requirements.
- those reducing test time.
- those compacting the test process.
- those not using specific test signals

In what follows, these techniques are summarized, describing their principles and benefits.

#### A. Relaxing input requirements

Traditional ADC test methods (either histogram or spectral analysis) rely on the generation of highly linear ramp signals or extremely pure sinusoidal tones. Translating these constraints into accuracy figures, both mean at least two more resolution bits than that of the ADC to be tested. Some authors have been dealing either with the implementation of high resolution signals for on-chip testing [1-4] or with devising simpler measurement procedures [5].

Instead, new techniques are reported based on finite resolution stimuli and new computational algorithms. Among them, [6] and [7] are interesting as they implement traditional test methods using two signals which do not require either high linearity [6] or high signal purity [7].

Another line of progress relies in the use of exponential waveforms. In [8-9], one exponential obtained by the discharge of a capacitor is proposed as a modification of the classical histogram technique. On the other hand, [10] uses a staircase-like exponential instead of a linear ramp and, through a polynomial fitting algorithm, provides a test method adequate for BIST.

The use of a noise signal as the test input stimuli is worked out in [11]. The interesting feature in this case is the need of many less output samples as compared to the histogram technique. This method paved the way for the use of specific signals of interest for concrete circuits, for instance for using pseudorandom signals to test

sigma-delta modulators. Another interesting approach has been recently reported based on a simplified double histogram [12].

#### B. Reducing test time

Another category of new methods is the one we can call model-based [13-18]. Among them, there are techniques relying on the development of a linear model using a reduced set of variables [13,14]. Strictly speaking, this does not relax the tester requirements but the number of specifications to be measured. On the other hand, in [15,16], tester resources are alleviated by measuring  $N$  devices and, from them, building an empirical model by resorting to a non-linear regression method. Finally, within this group we have to mention to methods that develop a behavioral model, like [17-19]. The main idea in this case is to translate complex performance specifications into some parameters which can be tested with a lower effort.

#### C. Compacting the test process

Recently, a new idea has emerged for the efficient testing of systems where several DACs and ADCs exist, no matter the relative accuracy of these converters [20]. A sequential procedure, involving every converter, is scheduled with the SoC to allow for the testing of all of them. It is proven that a trade-off between test time and measurement accuracy can be obtained.

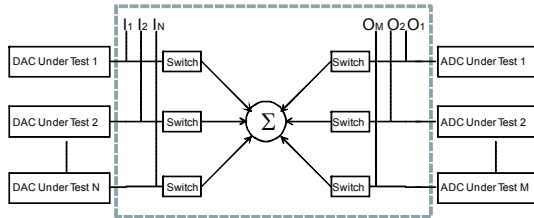


Fig. 3: On-chip Multi-converter Testing

#### D. Eliminating test stimuli

Finally, there are techniques that do not rely on even using a test stimulus. They are quite appealing from the point of view of BIST since generators are not needed at all. However, these techniques are not directly giving information of the specs and are much more useful for structural test. The most popular is the so-called Oscillation-based Test [21,22], relying in forcing oscillations either in a circuit or in a full system. Due to the fact that no generators are needed and that a purely-digital evaluation can be made [23,24], this technique worth interest mostly as a complement of other techniques. It has to be noticed that an interesting modification has been recently published [25,26]. Figure 5 shows a conceptual scheme for OBT. As seen in the upper part of this Figure, the SUT (System Under Test) is converted by any means into an oscillator. Then, an evaluation module reads a digital information regarding frequency, amplitude, DC level, etc. Finally, a digital

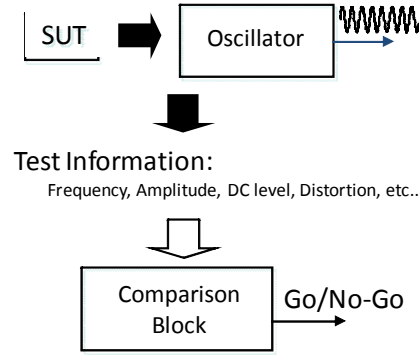


Fig. 4: OBT conceptual scheme

discrimination is performed to make a decision on accepting or rejecting the SUT.

### IV. TESTING THE RF PART

As we have discussed above, most SoCs incorporate a receive- as well as a transmit-function, which means that both a DAC as well as an ADC are present. From a test engineer point of view, testing RF subsystems embedded in a complex, tightly-integrated SoC represents a challenging task. The difficulty stems from the fact that each RF block has a specific set of diverse specifications that usually require a custom test strategy.

It can be said that RF testing has inherited all the difficulties of analog testing, but adding also the problem of having to handle high frequency signals. This framework leads to the same fundamental problem for analog and RF testing: these blocks are tested based on the functional measurement of a set of specifications, while fault-model-based test, very successful in the digital test domain, are impossible to standardize in the RF field, since each circuit type demands its own custom fault model.

The direct test and diagnosis of an RF device are based on the application of a high-frequency stimulus to the DUT, and the observation of its response. This requires the use of high-speed external test equipment and, for embedded RF devices, the provision of an adequate test access. However, the increase in operation frequency and integration capabilities turns the latter two requirements quite difficult. Test access to internal nodes is usually impossible, and even in the case these nodes are reachable, there may be electrical losses in the transport of the signals from the chip to the external tester due to their inherent high-frequency. This is why BIST should be so interesting if made feasible. Manipulations would remain internal, thus eliminating transport problems. However, the internal generation of RF signals makes difficult this alternative; only if we can devise a trick to avoid the generation of RF signals this approach can be used.

Some authors [27,28] replicate traditional RF test equipment such as spectrum analyzers on a load board.

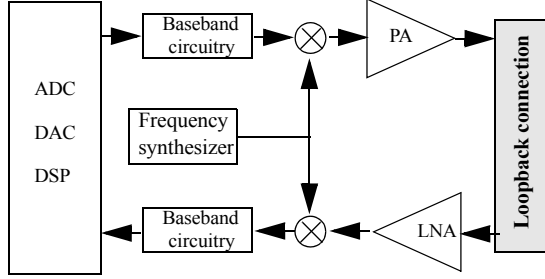


Fig. 5: Loopback Testing

These approaches employ complex circuitry (mixers, frequency synthesizer, etc.) for up- and down-conversion of the test stimulus and its response, respectively. The need of RF testers is eliminated and multiple RF test specifications can be extracted. However, the load board circuitry is too complex for its direct BIST implementation, and hence this approach is limited to the test of discrete RF circuits.

The approaches in [29-31] focus on failure diagnosis of RF circuits. The work in [29] considers the detection of catastrophic faults, while those in [30,31] also attempt to isolate parametric ones. Although behavioral simulations demonstrate high fault coverage, they lack a general fault model, and it is necessary the use of standard RF test equipment and techniques to enable failure diagnosis.

Loop-back test and diagnosis of transceivers have also been widely explored [32-36]. They follow the general scheme depicted in Figure 5. The signal coming from the transmitter part of a transceiver is re-injected into the receiver facilitating a global test for the transceiver signal chain. This enables the DAC to drive the ADC, allowing the implementation of a fully digital test as a very powerful and cost-effective test-scenario. The main advantage is that only-digital signals are involved as well as that both the receiver and the transmitter are tested at once. This concept leads to DFT implementations, although it relies on removing and switching some components, increasing complexity and disturbing the normal system operation. Furthermore, an on-chip implementation is not so simple since, in practice, some components need to be removed for testing [36] (namely the band-pass filter, close to the antenna, and the power amplifier in the transmission path), or a signal attenuator has to be introduced in the loopback connection to accommodate the PA output signal to the LNA input signal range [34].

The use of test sensors embedded into the RF system has also been proposed [34-41]. A number of sensors are usually located along the RF signal path, as it is depicted in Figure 6. Several built-in test schemes have been reported that use integrated peak, root-mean-square (RMS), and power detectors for testing discrete RF modules or complete transceivers. However, these sensors deliver a DC signal. To extract the test

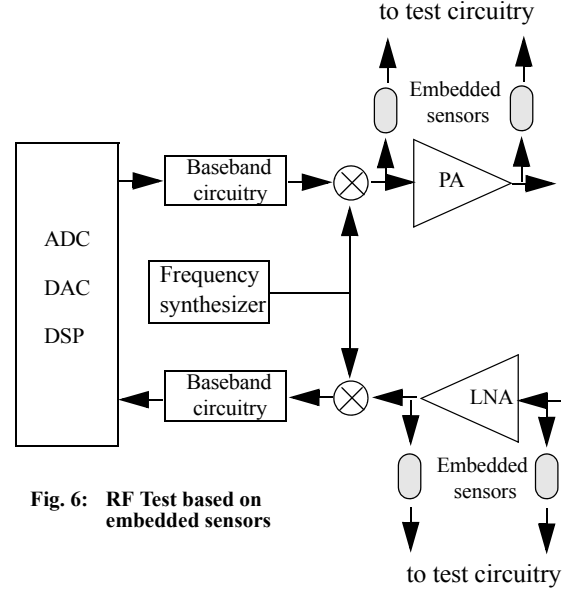


Fig. 6: RF Test based on embedded sensors

specifications from the limited information of a DC magnitude, multiple detectors and/or test configurations have to be used, thus increasing the complexity of the test as well as the required area overhead. Likewise, the design of these detectors is not always straightforward.

Another technique recently reported which can also be employed for testing of RF-based SoCs is the envelope response analysis, based on the generation of a particular, optimized stimulus and a complex post-processing after using one or several ADCs to convert the envelop of the system outcome to digital for interpretation. Some references exist differing in the kind of stimulus as well as in the way to make an interpretation of the response. Thus the work in [42] proposes an optimization algorithm to find the optimum multitone test stimulus, complemented with the use of a multivariate-adaptive regression spline mapping for extracting the target specifications from the digitized envelope response.

On the other hand, references [43, 44] extend the idea of testing by an envelope response characterization, but unlike [42], they are based on analytical results obtained by applying an arbitrary two-tone test stimulus to the device under test. The pre-processing stage for stimulus optimization is then eliminated. Furthermore, it uses simple first-order  $\Sigma\Delta$ -modulation for acquiring the response envelope, avoiding the need of a complete A/D

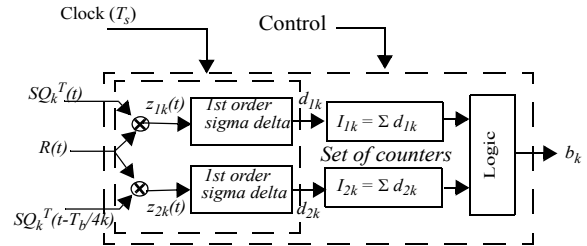


Fig. 7: Test core for the characterization of periodic signals

converter for signal acquisition, and simplifying the post-processing of the signal. This technique is also interesting from the viewpoint of incorporating BIST because the input test signal can be easily generated and the envelope detector itself is also simple. In Figure 7 the components of an evaluator for the envelope detector response are detailed, while A general BIST structure is shown in Figure 8.

## V. CONCLUSIONS

An overview of test techniques for analog, mixed-signal and RF integrated parts has been given. Emphasis has been put on those techniques which exhibit a promising trade-off between the test requirements (basically in terms of signal accuracy and frequency) and the test quality. A combined use of some of these methods is probably the best solution when BIST must be provided to a complex SoC.

## ACKNOWLEDGEMENTS

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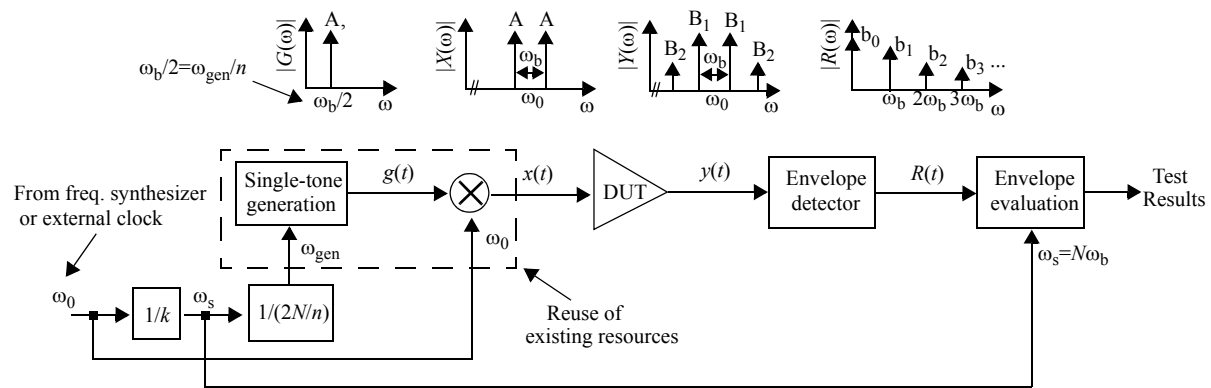


Fig. 8: Proposal for a full-BIST implementation

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