Efficient Utilization of Hierarchical iJTAG Networks for Interrupts Management

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***Abstract*—Modern systems-on-chips rely on embedded instruments for testing and debugging, the same instruments could be used for managing the lifetime dependability of the chips. The IEEE 1687 (iJTAG) standard introduces an access network to the instruments based on reconfigurable scan paths. During lifetime, instruments could be required to initiate communication with a system-level dependability manager for different reasons. For example, fault/event occurrences or measurement read-out requests; however iJTAG networks are inherently master/slave networks, where the instruments are the network slaves. In this work, a scalable interrupts-management methodology is presented for allowing instruments-initiated communication using hierarchical iJTAG networks. The presented method allows for an efficient access of the network according to the required use-case by allowing the network to be configured into a corresponding optimized mode. In addition, a novel on-chip localization methodology is presented, which significantly reduces the localization time of interrupting instruments as compared to previous works.**

***Keywords*—IEEE 1687, iJTAG, embedded instruments, fault management, dependability.**

I. Introduction

Following the increased complexity of System-on-Chips (SoCs) along with the decreased reliability of modern technology nodes, an increasing number of embedded instruments are now becoming integrated for testing, debugging and monitoring. The IEEE 1687 (iJTAG) [1] standard introduces standardized and scalable access networks to those instruments.

Many embedded instruments are used in maintaining the lifetime dependability of the chip, for example, temperature, voltage and current (iddt/q) sensors, delay monitors, Built-in-Self-Test (BIST) engines, error detectors, trace buffers, and many others. They allow executing dependability procedures, such as Dynamic Frequency and Voltage Scaling (DFVS) [2], online Built-In-Self-Test (BIST) [3] [4], operating conditions monitoring [5], fault diagnosis [6], and others.

Since embedded instruments became integrated into the iJTAG networks for off-chip access, reusing the networks for dependability on-chip access is an obvious solution for a standardized, scalable and low overhead access mechanism. During lifetime, an instrument could require to initiate the communication with an on-chip Dependability Manager (DM) for different purposes. Examples are the occurrence of a monitored event (triggers, errors, timeouts, ...), data/configurations request or to request a data readout. However iJTAG networks are inherently master/slave networks, where an iJTAG controller is the network master which initiates the communication with all the instruments acting as network slaves.

Instrument-initiated communication could be enabled by means of interrupts, however for a large number of instruments a huge routing overhead will be required for a separate interrupt signal per instrument. In [6] the authors utilized hierarchical iJTAG networks in delivering a global interrupt signal along with its diagnostics information following a fault occurrence to an on-chip fault manager, which then localizes the interrupting instrument. This method provides a simple and scalable interrupts delivery and localization solution.

The large number of dependability instruments found in modern SoCs, could generate different types of interrupts with different handling priorities. For example, a "measurements ready" interrupt raised by one of the on-chip sensors has a lower handling priority than a fault interrupt from a fault detector. The same idea as discussed in [6] for fault management, could be generalized for delivering different types of global asynchronous instruments interrupts along with any corresponding information, for dependability procedures that use iJTAG-integrated embedded instruments.

In [7], Segment Insertion Bits (SIBs) were extended to include in-line fault-diagnostics registers. Although this approach allows for a quick diagnosis, it adds an unnecessary overhead to the access time in case of normal instrument access. Access time could become critical in production testing, and for debugging in case of instruments that deliver runtime data. Adding additional in-line registers for different types of instruments interrupts will further increase both the normal instruments access time and the localization time.

In addition, the used iterative localization procedure in [6] is limited by the nature of the iJTAG standard where an access to a register requires a sequence of scan accesses to iteratively open an active path to that register. This affects the interrupt response, fault diagnosis and recovery times.

In this paper we introduce a methodology for the delivery and localization of instruments interrupts without any access time overhead on the normal instruments access, which enables more than one type/priority of interrupts. We also introduce a faster solution for on-chip localization as compared to [6] while keeping the possibility for off-chip (iJTAG compliant) interrupts management.

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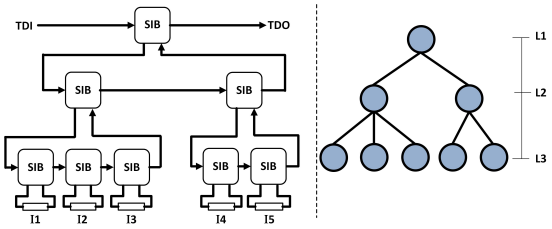

Figure 1: An example of a hierarchical iJTAG network.

II. Background and Terminologies

iJTAG networks are based on reconfigurable scan paths which consist of both scan registers and scan multiplexers. The reconfiguration of the network is performed via updatable network registers which serve as the source of the ScanMuxs' address signals named as the ScanMux Control Bits ($SCBs$). A register in the network is considered to be $selected$ when the network is configured such that this register becomes included in the active scan path. In case a register is selected, all its scan control signals (Shift Enable (SE), Capture Enable (CE) and Update Enable (UE)) become enabled.

A Segment Insertion Bit (SIB) is a main iJTAG network component which allows for a hierarchical organization of the iJTAG network. It consists of a Scan Multiplexer (ScanMux) and a corresponding SCB. When updated with a '1', a SIB is said to be $opened$, and the attached scan segment is included to the active scan path. In the case a '0' is updated to the SIB, it is said to be $closed$ and the attached segment is excluded.

Hierarchical iJTAG networks with one SIB in its top level can be viewed as a $directed\ rooted\ tree$ where the top level SIB is its $root$, and the instruments registers are connected to the $leaves$. Figure 1 shows an example of a hierarchical SIBs network. A SIB has one $parent$ in the higher level (except for the root), one or more $children$ in the lower level (except for the leaves), and could have one or more $siblings$ in the same level sharing the same parent. A SIB is selected when its parent is both selected and opened, in this case, scan control signals are also propagated from the parent SIB to its children. The root SIB is selected by the TAP controller.

We denote the scan path formed by opening only the parents of a network register (SIB or TDR) as the $minimum\ access\ path$ to this register.

In [6], hierarchical iJTAG networks were used for fault diagnosis. The SIB design was extended in [7] to accommodate for three diagnostic registers (F, C and X) in-line with the SIB register (S) for holding the diagnostic flags of the child subnetwork. In general, we refer to the in-line registers in the SIBs as the $hierarchical\ flags$. Hierarchical flags are used to hold binary information regarding the lower level subnetwork which helps in localizing an interrupting instrument as in the fault (F) flag, or for a quick propagation of additional interrupt information as in the corrected (C) flag.

A propagated fault signal to the root SIB, corresponds to the logical disjunction of all instruments fault flags, and it serves as the capture source of the top level fault diagnostic register. Once a '1' is found in the fault register, an Operating System (OS) interrupt is issued and localization is performed by iteratively opening SIBs with a '1' captured in its fault flag.

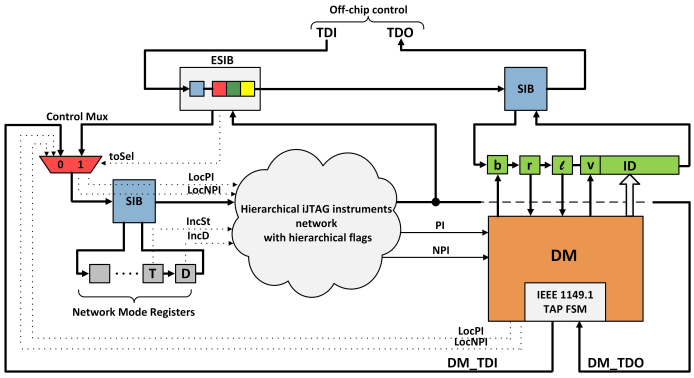

Figure 2: System level organization.

III. System-Level Organization

An on-chip Dependability Manager (DM) is incorporated in a SoC in order to manage its lifetime dependability by executing procedures using the distributed on-chip instruments. It uses the iJTAG network as an access mechanism to the instruments. Figure 2 shows the system-level iJTAG network organization of a SoC with a DM. The DM is considered as a top-level embedded instrument with a set of off-chip accessible Test Data Registers (TDRs). They are used for organizing the network control, where a busy (b) flag indicates that the DM is currently accessing the network, and a request (r) flag indicates a network access request from the off-chip controller.

A control Multiplexer selected by the 'toSel' signal of the top-level Extended SIB (ESIB), ensures that the DM's signals are physically disconnected whenever the top-level ESIB is opened by an off-chip controller. The hierarchical instruments network could be configured into several modes using either scan-updatable SCBs (Network mode registers) or using DM-generated on-chip modes signals.

The iJTAG network hierarchy is utilized to deliver different interrupt types with different priorities to the DM and to localize their sources. The different interrupts are propagated via hierarchical asynchronous OR networks where their outputs are the disjunction of all of the corresponding instruments interrupts. The design of the SIB to allow for the systematic formation of such network was discussed in [7] for faults interrupts. Figure 3 shows the corresponding OR network to the iJTAG network organization shown in Figure 1. The capture source of the in-line flag register is the disjunction of all the flags in the children subnetwork.

Two general types of interrupts are defined in dependability management, being Preemptive Interrupt (PI) and Non-Preemptive Interrupt (NPI). A PI usually corresponds to the occurrence of a critical fault. When a DM receives a PI, it immediately stops any ongoing access and starts a localization process and then notifies the OS with the location of the fault. On the other hand, an NPI does not require the DM to stop its ongoing operation, in this case interrupt handling occurs afterwards. Sources of NPIs could be instruments requesting

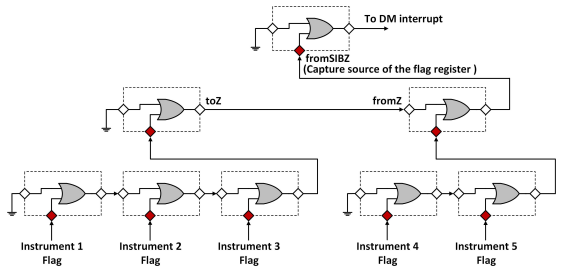

Figure 3: Flag Propagation network.

for configurations or for data read-out like the status bits in the instruments with non-deterministic execution times as presented in [8]. In addition to the included fault (F) hierarchical flag register in the SIB design for fault flag-propagation, a status (St) register is added to hold the propagated instruments status flags. The F register is used in localizing a PI, while an St register is used in localizing an NPI. Other flags could also be included for different PI or NPI interrupts priorities.

IV. Multi-Mode iJTAG Networks

The iJTAG network can be configured into several modes, each optimized for a different use-case. In this work we present three main modes for efficient interrupts management:

1) Normal instruments access (mode A).
2) Access with hierarchical flags (mode B).
3) On-chip localization (mode C).

In mode A, the hierarchical flags are not required to be accessed, therefore they are bypassed while accessing a SIB. A network is configured to Mode B in case one or more hierarchical flags are required to be accessed. For example, when it is required to perform diagnosis in parallel with the normal instrument access or in case of off-chip fault localization. Finally mode C allows for an optimized network configuration in case of localizing an interrupting instrument. In this mode the network is configured such that a scan path is formed to include only the interrupt flag registers of the ESIBs found in the minimum access path to the interrupting instrument. This path will be referred to as the $localization\ path$.

Figure 4(a) shows the hierarchical network shown in Figure 1 configured to mode A while accessing the second instrument (I2), and with the SIBs extended to accommodate for the diagnostic and the status registers. In this mode, only the (S) registers of the ESIBs are included in the active scan path. In Figure 4(b) the same network is configured to mode B where the diagnostic registers are included in the active scan path along with the S register. Figure 4(c) shows the localization path of I2 while configuring the network to mode C. Here only the PI flag registers of the ESIBs in the minimum access path to I2 are included.

Initially the network is configured in mode A. For configuring the network into mode B, a set of global SCBs are updated to '1' in order to include corresponding hierarchical flags into the scan path inside the extended SIB. Those SCBs are shown in Figure 2 as the network mode registers. They generate the include (IncZ) control signals from their update stages to the network (where Z refers to any hierarchical flag register).

The required time in clock cycles (t_{acc}) for accessing an instrument in level L, starting with a fully closed network configured in either modes A or B, is given in equation (1). Here R denotes the number of selected registers in the ESIB, E is the number of clock cycles in the Capture-Shift-Update (CSU) cycle [6], and b_i is the number of sibling ESIBs at the i^{th} level. For example in Figure 4, b_1 = 1, b_2 = 2, b_3 = 3. The accessing is performed by iteratively opening the parents ESIBs until the instrument's TDR is reached.

$$t_{acc} = \sum_{i=1}^{L} \Big((L - i + 1) b_i \times R \Big) + L \times E \qquad (1)$$

The formed scan path in mode C is dependent on the propagated flag values from the OR network, therefore mode C does not follow the specifications of the iJTAG standard which limits the sources of the ScanMux select signals to either updatable registers or to the primary inputs of the chip. For this reason mode C was only allowed as an on-chip mode. In Figure 2, two localize (LocZ) signals are generated by the DM to configure the network to the localization path of either a PI or an NPI interrupt. Whenever an off-chip controller accesses the network, they are pulled down to '0' via the control mux.

In case of off-chip localization, the off-chip controller could either configure the network in mode B with the corresponding interrupt flag included and perform the localization as discussed in [6] which uses the slow off-chip test clock (TCK), or it can use the DM for a fast on-chip localization by closing the top-level ESIB and setting the localize (l) TDR of the DM to '1'. The DM then configures the network into mode C and performs the localization using the chip's clock then reports the ID of the localized instrument by setting the valid (v) TDR to '1' and writing the instrument's ID in the 'ID' TDR.

A. Performing On-chip Localization

When the network is configured for on-chip localization (mode C), the localization path is automatically formed as the active scan path. The ESIBs are designed such that the flag registers are shifted-out before the contents of the inserted subnetwork. The localization procedure is performed as follows: the DM applies a CSU cycle via the embedded TAP FSM, such that the interrupt flag registers capture the propagated flag values first; then a continuous $hierarchy\text{-}aware$ shift-out is performed until the whole localization path is processed. The interrupting instrument(s) is/are localized by analyzing the contents of the interrupt flag registers of leaf ESIBs and identify the one(s) containing a '1'.

The hierarchy-aware shift-out is essential in determining the correspondence between a shifted-out bit with the hierarchical flag registers and consequently the length of the localization path. The DM stores the network hierarchy information. Starting from the first shifted-out bit (which always corresponds to the right-most top-level ESIB's flag register), the DM analyzes the value of each shifted-out bit. If it is a '0' then the next bit would correspond to the left sibling flag register, and if it is a '1' then the next bit would correspond to the right most ESIB flag register in the child subnetwork. For the leaf ESIBs

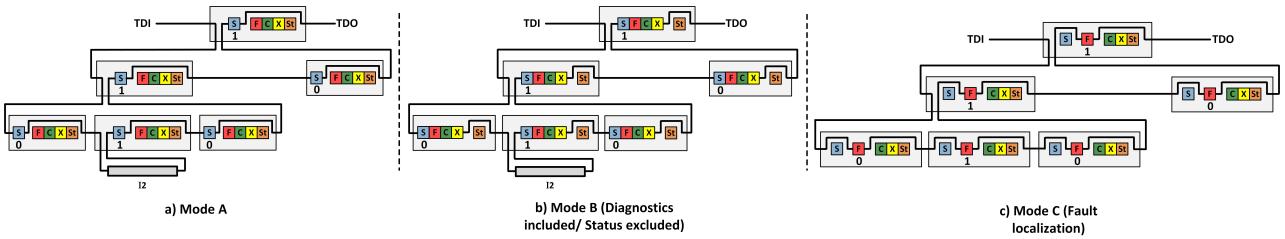

Figure 4: Network modes for accessing/localizing I2.

the next bit is always the left sibling flag bit. For the left-most ESIB in any level, a '0' indicates that the next bit would be the flag register of the left sibling of the first non-left-most parent ESIB among the parents of this ESIB. The hierarchy-aware shift-out ends when all the parents of a left-most ESIB are also left-most ESIBs. The processing time required for each shifted-out bit is a constant and referred to as the bit-processing time (c).

The number of clock cycles required to perform the localization using mode C (t_{loc}) is given in Equation (2). The localization occurs during the shift cycle, which takes 2 clock cycles from the beginning of the CSU cycle.

$$t_{loc} = 2 + c + \sum_{i=1}^{L} b_i \tag{2}$$

B. Optimum Network Organization for On-chip Localization

The iJTAG network hierarchy could be optimally organized for minimizing the localization time [6]. Assuming a single interrupt type for all the instruments, a balanced tree is proposed such that the localization path length of all instruments is either the same or differ by 1. For example, if a binary tree is used to connect 17 instruments, the number of ESIBs in each level will be 1, 2, 4, 8, 17 respectively, with the same sibling group size (b) of 2 in each level, except for the first level (only one ESIB), and for the leaf one (7 groups with 2 siblings and one group with 3). The length of the instruments localization path in this organization will be either 9 or 10.

The organization problem could be formulated as follows: Given a number (N) of instruments, find the balanced tree organization which results in the minimum localization time for the instrument with the longest localization path in this organization. This problem could be solved by a constrained exhaustive search of all the valid balanced network organizations for the given number of instruments and calculating t_{loc} for each, then choosing the one with the minimum t_{loc} as the optimum organization for this number of instruments.

A number of constraints are provided based on the properties of balanced trees. The maximum depth (L_{max}) of a balanced tree with N leaves is in the case of a binary tree:

$$L_{max} = \lfloor log_2(N) \rfloor + 1 \tag{3}$$

For a given network depth (L), the maximum number of nodes (S) in a certain level (n) occurs if the lower network is binary. Note that for the first level S_1 is equivalent to b_1.

$$S_{n_{max}} = \left\lfloor \frac{N}{2^{L-n}} \right\rfloor \tag{4}$$

The total number of nodes in a certain level (S_n) can be recursively calculated as: $S_n = b_n * S_{n-1}$, therefore:

$$b_n = \frac{S_n}{\prod_{i=1}^{n-1}(b_i)}, \quad 1 < n < L \tag{5}$$

For a certain level (n), given the sibling group sizes of the higher levels (b_1 ... b_{n-1}), the upper bound of a sibling group size at this level could be calculated by substituting (4) in (5):

$$b_{n_{max}} = \left\lfloor \frac{N}{2^{L-n}} \Big/ \prod_{i=1}^{n-1}(b_i) \right\rfloor, \quad 1 < n < L \tag{6}$$

After constraining both the network depth in (3) and the sibling group size for each level in (6), finding the organization with the minimum t_{loc} could be done as follows:

1) Choose a network depth (L), where $1 \leq L \leq L_{max}$.
2) Start with the binary organization of depth (L). Calculate the corresponding b_L from eq. (7), and each of the level constraints $b_{n_{max}}$ from eq. (6) for this organization.
3) Calculate t_{loc} of this organization according to eq. (2).
4) Increment b_{L-1} and calculate the corresponding b_L, then calculate t_{loc}. Repeat until $b_{(L-1)} = b_{(L-1)_{max}}$.
5) Increment (b_n) in the next higher level with $b_n < b_{n_{max}}$.
6) Set the lower levels to a binary organization and update the corresponding $b_{n_{max}}$ for each lower level, then repeat 3-6 until all levels reach its maximum values.
7) Increase L and repeat 2-7.

$$b_L = \left\lceil N \Big/ \prod_{i=1}^{L-1}(b_i) \right\rceil \tag{7}$$

After exhaustively searching the space of valid organizations and calculating the corresponding t_{loc}, the organization with the lowest t_{loc} value is chosen as the optimum one.

For multiple interrupt types, the instruments are divided into groups, where each group generates the same type of interrupt. The same optimized construction procedure could be applied for each group with $N = N_{group}$. In this way all instruments with similar interrupt type will have the minimum possible localization time. The optimally organized networks could be connected together at the first level starting from the group with the most critical interrupt connected to the right. In this configuration, the localization time of the most critical interrupts will not be affected by the other instruments as all the interrupting instruments' flag registers will be shifted out before shifting any registers from the other groups. The next

Table I: Extended SIB ports

Signal	Mode	Src/Dest	Description
SI	In	Sibling/Parent	Scan input
fromSO	In	Child	Scan output of child subnetwork
CE	In	Parent	Capture enable
SE	In	Parent	Shift enable
UE	In	Parent	Update enable
Sel	In	Parent	Select for modes A and B
IncZ*	In	Parent	Include Z register
LocZ*	In	Parent	Localize Z register
fromSIBZ*	In	Sibling	Sibling Z flag
fromZ*	In	Child	Children Z flag
SO	Out	Sibling/Parent	Scan output
toSI	Out	Child	Scan input of child subnetwork
toSel	Out	Child	Child select for modes A and B
toCE	Out	Child	Child capture enable
toSE	Out	Child	Child shift enable
toUE	Out	Child	Child update enable
toIncZ*	Out	Child	Child include Z register
toLocZ*	Out	Child	Child localize Z register
toZ *	Out	Sibling/Parent	Propagated Z flag

[1](*) indicates possible multiple signals from the same type according to the included flag registers in the ESIB.

group's localization time will be increased with the number of ESIBs in the first level of the rightmost group.

V. Architecture of the Extended SIBs

The different network modes presented in section IV requires re-designing the Extended SIB (ESIB) to allow for bypassing certain registers in each mode, and to insert/exclude children segments based on the propagated flag in case of mode C. This design not only should cover the scan path reconfiguration but also should resolve the conditions of hierarchically propagating the control signals (CE, SE, UE, Sel) and the mode signals (Include and Localize). Resolving those conditions should be performed while adhering to the iJTAG standard for modes A and B. The ESIB design should maintain the modularity of a SIB as a building block of hierarchical iJTAG networks, and should also be scalable with regard to adding further interrupt types with different handling priorities.

In order to have a simple ESIB design two conditions are defined for a DM during mode C:

1) Only one type of interrupt localization is allowed at a given time. (Only one LocZ signal is active)
2) The DM 'Sel' signal is set to '0' whenever mode C is entered.

A DM generates the control signals along with one or more localize (LocZ) signals to the second-level ESIBs through the control Mux. Then the control, 'Loc' and the SCBs-generated include (IncZ) signals are propagated down the hierarchy to the selected ESIBs.

Figure 5 shows the internal organization of the ESIB. It consists of a mandatory S register which is updated to '1' to include the child segment in case of modes A or B, followed by one or more flag registers. Each represents either a captured propagated interrupt flag or a flag for additional interrupt information. Each register in the ESIB can be excluded from the scan path via a bypass Mux. A segment insertion Mux is included directly after the scan input. If a register is selected in the scan path via the bypass Mux, the scan control signals (CE, SE, UE) are also enabled to it. The ports of the ESIB along with their sources are shown in Table I.

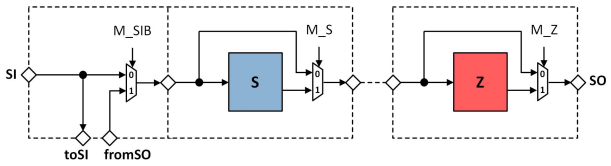

Figure 5: Extended SIB scan path organization.

The scan-path configuration conditions for the S and the flags (Z) registers are shown in equations (8) and (9). Equation (8) follows the same scan-path configuration condition of the original SIB register. Note that in mode C the DM forces the top level 'Sel' to '0' which consequently sets all the 'Sel' signals to '0'. In (9) a flag register becomes selected either in mode B where the corresponding include signal = '1', or in mode C where the corresponding localize signal = '1'.

$$M\_S = Sel \tag{8}$$

$$M\_Z = (Sel \wedge IncZ) \vee (LocZ) \tag{9}$$

The child segment insertion condition is shown in equation (10). The child segment is inserted either when the S register is updated with a '1' in mode A or B, or when one of the interrupt flags is propagated from the subnetwork with its corresponding localize signal enabled (except for the leaf ESIBs). This equation implies that the interrupting instrument should hold its interrupt flag until the localization procedure ends (indicated by setting LocZ to '0') in order to keep the localization path configured properly.

$$M\_SIB = (Sel \wedge S_{update}) \vee (\bigvee_{\forall Z}(LocZ \wedge fromZ)) \tag{10}$$

Equations (11-13) show the conditions for the hierarchical propagation of the Sel and mode signals. The Sel signal in equation (11) is propagated to the child subnetwork when the S register is updated with a '1'. In equation (11) the 'IncZ' signal is propagated whenever the ESIB is selected. Note that equation (9) indicates that the propagated Inc signal to a child ESIB will not become effective except when this ESIB is also selected. This conforms with the propagation of the scan controls as presented in the standard.

Equation (13) indicates that the 'LocZ' signal is asynchronously propagated to all the ESIBs in the localization path whenever the DM sets the top level 'LocZ' signal to '1'.

$$toSel = Sel \wedge S_{update} \tag{11}$$

$$toIncZ = IncZ \wedge Sel \tag{12}$$

$$toLocZ = LocZ \wedge fromZ \tag{13}$$

The conditions for propagating the scan control signals are shown in equations (14-16). Similar to the 'IncZ' signal, the scan control signals are propagated when the ESIB is selected in modes A or B. The Capture and Shift enables are also propagated when the ESIB is configured to mode C and one of the Loc signals is active. The update enable signal is not used in mode C.

Table II: Localization time reduction

N	b	t_{loc} [6]	Off-chip		On-chip		On-chip (optimized hierarchy)			
			t_{loc} (Mode B)	Rd	t_{loc} (Mode C)	Rd	# Valid Networks	b_{new}	t_{loc} (Mode C)	Rd
25	3,9	90	54	40%	14	84.4%	55	3,3,3	11	87.8%
50	4,13	118	68	42.4%	19	83.9%	179	2,3,3,3	13	89%
100	5,20	158	88	44.3%	27	82.9%	581	3,3,3,4	15	90.5%
200	3,4,17	206	118	42.7%	26	87.4%	1897	2,3,3,3,4	17	91.7%
500	4,6,21	266	148	44.4%	33	87.6%	8837	3,3,3,4,5	20	92.5%
1000	5,8,25	326	178	45.4%	40	87.5%	29303	2,3,3,3,4,5	22	93.1%

$$toCE = CE \wedge (Sel \vee (\bigvee_{\forall Z} LocZ)) \quad (14)$$

$$toSE = SE \wedge (Sel \vee (\bigvee_{\forall Z} LocZ)) \quad (15)$$

$$toUE = UE \wedge Sel \quad (16)$$

It should be noted that when the ESIB is configured to mode C, the content of the S register is preserved, since no shift, capture or update operations are allowed to the S register. A DM could interrupt the ongoing accesses on receiving a PI interrupt, configure the network to mode C and perform localization. When the network is set back to either mode A or B, it will be configured to its last configuration, and the halted instruments accesses would start immediately.

VI. Experimental Results

The reduction in both the access and the localization times for the multi-mode iJTAG networks are analyzed in this section compared to the diagnostics networks in [6]. In order to quantitatively evaluate the access time reduction, the evaluation on balanced diagnostics network organizations is performed with the minimum access time for identical instruments. This organization could be achieved using the same analysis in section IV, while minimizing the access time in equation (1) (with R=4) instead of the localization time.

Given the resulting balanced network organization for N identical instruments, we calculate the access time (t_{acc}) for both the diagnostics network in [6] with all the diagnosis flags attached (R=4), and the multi-mode network proposed in this work configured to mode A (R=1). Figure 6 shows the values of the instrument access time in each network for N = 1 to 1000. The mean reduction value of the instrument access time achieved by a multi-mode network in mode A is 66.3% .

Table II shows the localization time reduction (Rd) compared to the previous work, in the following three cases: 1) Off-chip localization with reduced hierarchical flags count (mode B with only 'F' included). 2) On-chip localization (mode C) using the network organization in the previous work, 3) On-chip localization (mode C) using the optimized network organization discussed in section IV. The bit processing time is ignored in all three cases. It can be shown that when using mode B with reduced flags for off-chip localization, t_{loc} is reduced by an average of 43.2%. While using mode C t_{loc} is reduced by an average of 85.6% for the same network and 90.8% for the optimized one. For mode C, the proposed

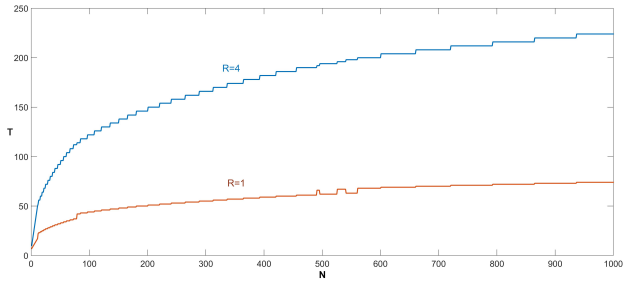

Figure 6: Instrument access times.

network optimization reduced the localization time by an average of 36.1% compared to the networks proposed in [6].

VII. Conclusions

Considering the current increasing trend of integrating embedded instruments for debugging and monitoring, a System-on-Chip is expected to experience a growing number of lifetime instruments interrupts of different types and handling priorities. In this work an efficient scalable-methodology for the delivery and localization of interrupts is presented based on hierarchical, multi-mode iJTAG networks. System-level and network-level organizations were discussed along with the required architectural modifications to the basic network component. It was shown that using multi-mode networks, both the access and localization times are decreased by 66% and 91% respectively compared to previous works.

References

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