GaN Nanowire Field Emitters with a Self-Aligned Gate Process

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Introduction: Electron devices based on field emitters (FE) are promising for harsh-environments and high-frequency electronics thanks to their radiation hardness and scattering-free electron transport. Si field emitters with a sub-10 nm tip radius and self-aligned gates have demonstrated sub-20 V turn-on operation [1,2]. However, stability and operating voltage still need further improvement to enable circuit applications. III-Nitrides are excellent candidates to overcome these issues because of their strong bonding energies [3] and tunable electron affinities [4]. So far, there are few demonstrations of III-Nitride field emitters with self-aligned gates, which are critical to reduce the gate-emitter voltage (V_{GE}). In this work, a novel GaN nanowire (NW) field emitter based on self-aligned gates is demonstrated to reduce the gate-emitter turn-on voltage ($V_{GE,\,ON}$) below 30 V. To the best of our knowledge, this represents the lowest control voltage in any GaN field emitter device, opening an opportunity for using III-N in integrated field emitters.

Device fabrication: The epitaxial stack was grown by Enkris Semiconductor, Inc. on a 1-mm thick Si (111) substrate. The structure is as follows: 100 nm n^{++}-GaN (Si: 1×10^{19} cm^{-3}), 1 μm n^{-}-GaN (Si: 1×10^{17} cm^{-3}), 2 μm n^{++}-GaN (Si: 1×10^{19} cm^{-3}), buffer, and Si substrate (Fig. 1). Fig. 2 (a) shows the device geometry, and Fig. 2 (b) summarizes the process flow for fabricating these self-aligned gate GaN field emitters. The fabrication starts with (1) nanowire (NW) formation using e-beam lithography, Ni lift-off, Cl_2/BCl_3-based dry etching, and sidewall-healing with TMAH treatment (Fig. 3 (a)). Then the Ni mask is removed. After the NW formation, (2) a TEOS layer of 160-nm thickness and then 100 nm Cr are conformally deposited. The gate-emitter distance (d_{ge}) is determined by the thickness of the deposited TEOS layer. After deposition, (3) devices are planarized by thick TEOS deposition followed by a blank dry etching. (4) The exposed top Cr regions are then dry etched with Cl_2/O_2-based chemistry. (5) Metal contact to the n-GaN layer is then formed by Ni/Au lift-off process. Finally, (6) CF_4/O_2-based dry etching is used to remove TEOS to expose GaN tips (Fig. 3 (b)).

Results and Discussion: Transfer characteristics and corresponding Fowler-Nordheim (F-N) plot of self-aligned gate GaN NW field emitters are shown in Fig. 4. The anode is a suspended W ball with 0.5-mm diameter biased at +500 V (Fig. 4(a)). The gate aperture diameter is 400 nm, and the pitch between emitters is 1.2 μm. The lowest obtained turn-on V_{GE} is 27 V and ON-state current is about 500 nA at V_{GE} = 60 V with a 50 × 50 60-nm width and 300-nm height NWs field emitter array (FEA) (Fig. 4 (a)). The slope of F-N plot in Fig. 4 (b) is about -578, leading to a field factor (β) of 8.76×10^5 cm^{-1}, assuming the work function of n^{++}-GaN is 3.8 eV [5]. Similar to Si devices [1,2], the turn-on voltage and ON-state current are expected to be improved by increasing the number of NWs and reducing NWs' tip radius. Moreover, it should be noted that the epitaxial structure has an n^{-}-GaN (Si:1×10^{17} cm^{-3}) layer in the stack, which should be removed in future structures to reduce the series resistance of NWs. The output characteristics and lifetime of the devices were also measured (Fig. 5 (a) and (b)). The relatively large noise in these plots might be the result from the charging/discharging events during measurement since the electric field from the anode ball is not horizontally uniform. Moreover, a large gate leakage increase occurs after about 10 min in the lifetime test (Fig. 5 (b)). Although more work needs to be done to improve device stability, these devices show the lowest turn-on voltage and high current density among reported GaN filed emitters (Fig. 5 (c)). We are currently developing an integrated anode for integrated circuit applications, which we expect will improve the performance further.

Conclusion: GaN NW field emitters with self-aligned gates are fabricated with a TEOS planarization technology. This new technology reduces the turn-on V_{GE} below 30 V for a 50 × 50 NW arrays with NW width of 60 nm and height of 300 nm. The d_{ge} is about 160 nm and can be precisely controlled by TEOS deposition. With optimization and an integrated anode, integrated circuit applications are possible with III-Nitrides field emitters in the future.

Acknowledgment

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Reference

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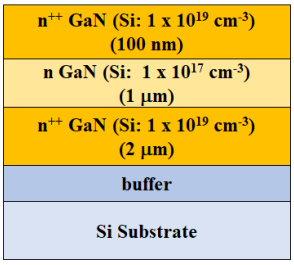

Fig. 1. Epitaxial structure of the wafer used in this work.

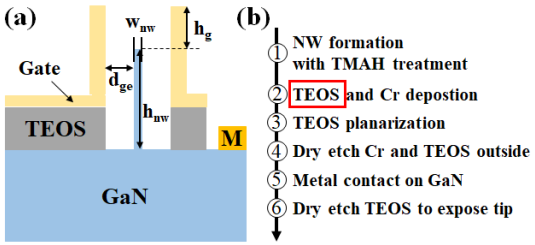

Fig. 2. (a) The device geometry and (b) the process flow of GaN NW field emitters with self-aligned gate. The gate-emitter distance (d_{ge}) is determined by the TEOS deposition highlighted by a red rectangle in (b).

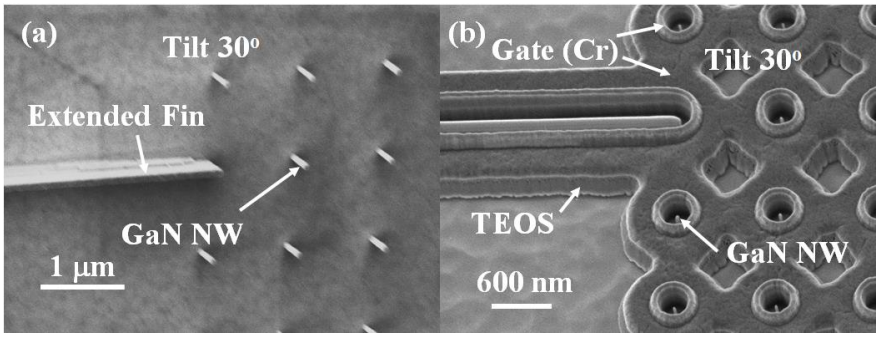

Fig. 3. Scanning electron microscope (SEM) images of (a) GaN NWs with extended fin and (b) finished self-aligned gate FEs. The "extended fin" is used to extend out the gate metal to a large metal pad.

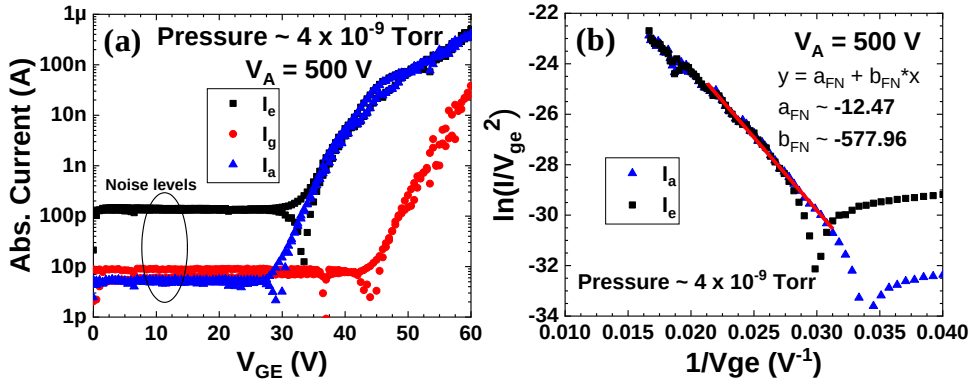

Fig. 4. (a) Transfer characteristics and (b) corresponding F-N plot of GaN NW field emitters in Fig. 3 (b) with a 50 × 50 NW arrays with NW width (w_{nw}) of 60 nm and NW height (h_{nw}) of 300 nm.

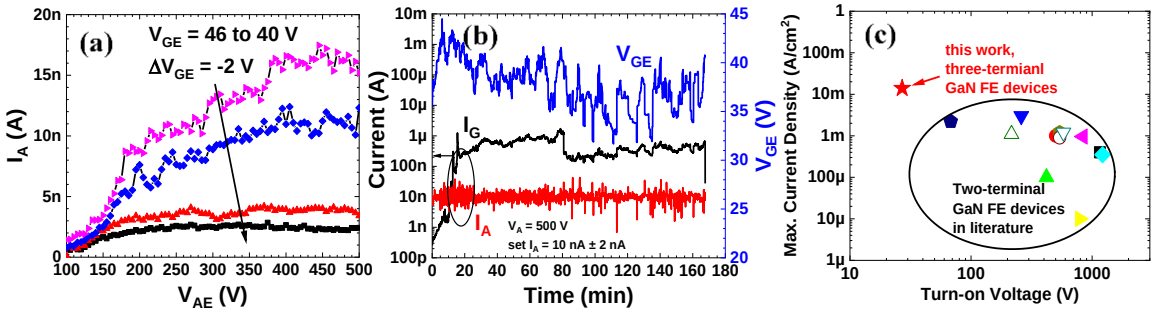

Fig. 5. The (a) output characteristics and (b) lifetime test of this GaN FEA, and (c) benchmark of different GaN FE devices. The device failed after 160 mins due to the formation of leakage path between gate and emitter. To the best of the authors' knowledge, this work is the first one demonstrating sub-30 V turn-on voltage in GaN FE devices.